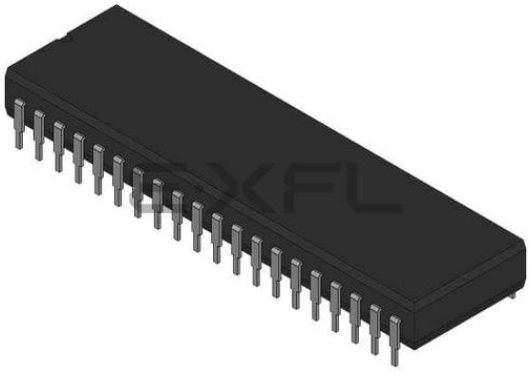

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at89lp3240-20pu

There is no difference in counting rate between Timer 2's Auto-Reload/Capture and Baud Rate/Clock Out modes. All modes increment the timer once per clock cycle. Timer 2 in Auto-Reload/Capture mode increments at 12 times the rate of standard 8051s. Setting TPS_{3-0} = 1101B will force Timer 2 to count every twelve clocks. Timer 2 in Baud Rate or Clock Out mode increments at twice the rate of standard 8051s. Setting TPS_{3-0} = 0001B will force Timer 2 to count every two clocks.

2.3.6 Serial Port

The baud rate of the UART in Mode 0 defaults to 1/4 the clock frequency, compared to 1/12 the clock frequency in the standard 8051. In should also be noted that when using Timer 1 to generate the baud rate in UART Modes 1 or 3, the timer counts at the clock frequency and not at 1/12 the clock frequency. To maintain the same baud rate in the AT89LP3240/6440 while running at the same frequency as a standard 8051, the time-out period must be 12 times longer. Mode 1 of Timer 1 supports 16-bit auto-reload to facilitate longer time-out periods for generating low baud rates.

Timer 2 generated baud rates are twice as fast in the AT89LP3240/6440 than on standard 8051s when operating at the same frequency. The Timer Prescaler can also scale the baud rate to match an existing application.

2.3.7 SPI

The Serial Peripheral Interface (SPI) has a dedicated interrupt vector. The ESPI (IE2.2) bit replaces SPIE (SPCR.7). SPCR.7 (TSCK) now enables timer-generated baud rate.

The SPI includes Mode Fault detection. If multiple-master capabilities are not required, SSIG (SPSR.2) must be set to one for master mode to function correctly when $\overline{SS}$ (P1.4) is a general purpose I/O.

2.3.8 Watchdog Timer

The Watchdog Timer in AT89LP3240/6440 counts at a rate of once per clock cycle. This compares to once every 12 clocks in the standard 8051. A common prescaler is available to divide the time base for all timers and reduce the counting rate.

2.3.9 I/O Ports

The I/O ports of the AT89LP3240/6440 may be configured in four different modes. By default all the I/O ports revert to input-only (tristated) mode at power-up or reset. In the standard 8051, all ports are weakly pulled high during power-up or reset. To enable 8051-like ports, the ports must be put into quasi-bidirectional mode by clearing the P1M0, P2M0, P3M0 and P4M0 SFRs. The user can also configure the ports to start in quasi-bidirectional mode by disabling the Tristate-Port User Fuse. When this fuse is disabled, P1M0, P2M0, P3M0 and P4M0 will reset to 00h instead of FFh and the ports will be weakly pulled high. Port 0 and the upper nibble of Port 2 always power up tristated regardless of the fuse setting due to their analog functions.

2.3.10 External Memory Interface

The AT89LP3240/6440 does not support external program memory. The $\overline{PSEN}$ and $\overline{EA}$ functions are not supported and those pins are replaced with general purpose I/O. The ALE strobe does not toggle continuously and cannot be used as a board-level clock.

automatically tristated when inputting data regardless of the Port 0 configuration. The Port 0 configuration will determine the idle state of Port 0 when not accessing the external memory.

Figure 3-9 and Figure 3-10 show examples of external data memory write and read cycles, respectively. The address on P0 and P2 is stable at the falling edge of ALE. The idle polarity of ALE is controlled by ALES (AUXR.0). When ALES = 0 the idle polarity of ALE is high (active). When ALES = 1 the idle polarity of ALE is low (inactive). The ALE strobe pulse is always active high. Unlike standard 8051s, ALE will not toggle continuously when not accessing external memory. ALES must be zero in order to use P4.4 as a general-purpose I/O. The WS bits in AUXR can extended the $\overline{RD}$ and $\overline{WR}$ strobes by 1, 2 or 3 cycles as shown in Figures 3-11, 3-12 and 3-13. If a longer strobe is required, the application can scale the system clock with the clock divider to meet the requirements (See Section 6.5 on page 32).

Figure 3-9. External Data Memory Write Cycle (WS = 00B)

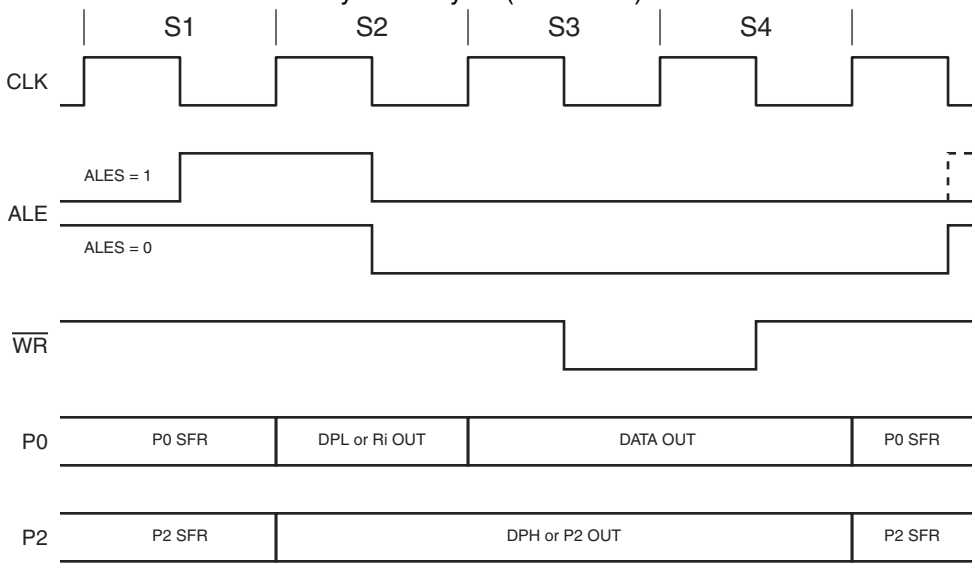


Figure 3-10. External Data Memory Read Cycle (WS = 00B)

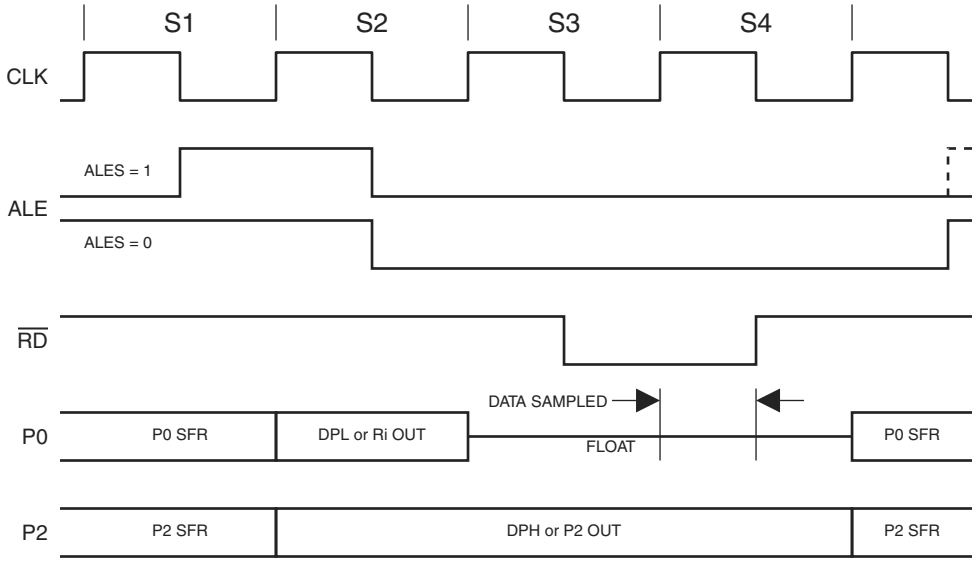


Table 5-5. DPCF – Data Pointer Configuration Register

DPCF = A2H — Reset Value = 0000 00X0B

Not Bit Addressable

	DPU1	DPU0	DPD1	DPD0	SIGEN	0	–	DPS
Bit	7	6	5	4	3	2	1	0

Symbol	Function
DPU1	Data Pointer 1 Update. When set, MOVX @DPTR and MOVC @DPTR instructions that use DPTR1 will also update DPTR1 based on DPD1. If DPD1 = 0 the operation is post-increment and if DPD1 = 1 the operation is post-decrement. When DPU1 = 0, DPTR1 is not updated.
DPU0	Data Pointer 0 Update. When set, MOVX @DPTR and MOVC @DPTR instructions that use DPTR0 will also update DPTR0 based on DPD0. If DPD0 = 0 the operation is post-increment and if DPD0 = 1 the operation is post-decrement. When DPU0 = 0, DPTR0 is not updated.
DPD1	Data Pointer 1 Decrement. When set, INC DPTR instructions targeted to DPTR1 will decrement DPTR1. When cleared, INC DPTR instructions will increment DPTR1. DPD1 also determines the direction of auto-update for DPTR1 when DPU1 = 1.
DPD0	Data Pointer 0 Decrement. When set, INC DPTR instructions targeted to DPTR0 will decrement DPTR0. When cleared, INC DPTR instructions will increment DPTR0. DPD0 also determines the direction of auto-update for DPTR0 when DPU0 = 1.
SIGEN	Signature Enable. When SIGEN = 1 all MOVC @DPTR instructions and all IAP accesses will target the signature array memory. When SIGEN = 0, all MOVC and IAP accesses target CODE memory.
DPS	Data Pointer Select. DPS selects the active data pointer for instructions that reference DPTR. When DPS = 0, DPTR will target DPTR0 and /DPTR will target DPTR1. When DPS = 1, DPTR will target DPTR1 and /DPTR will target DPTR0.

5.2.2 Data Pointer Operating Modes

The Dual Data Pointers on the AT89LP3240/6440 include three additional operating modes that affect data pointer based instructions. These modes are controlled by bits in DSPR.

5.2.2.1 DPTR Redirect

The Data Pointer Redirect to B bit, DPRB (DSPR.0), allows MOVX and MOVC instructions to use the B register as the data source/destination when the instruction references DPTR1 as shown in Table 5-6 and Table 5-7. DPRB can improve the efficiency of routines that must fetch multiple operands from different RAM locations.

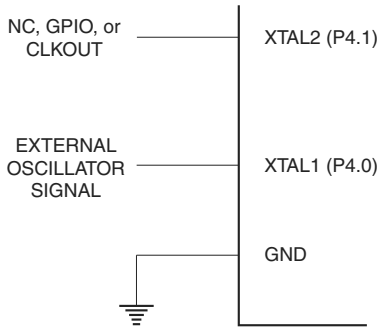
Table 5-6. MOVX @DPTR Operating Modes

		Equivalent Operation for MOVX			
		MOVX A, @DPTR		MOVX @DPTR, A	
DPRB	DPS	DPTR	/DPTR	DPTR	/DPTR
0	0	MOVX A, @DPTR0	MOVX A, @DPTR1	MOVX @DPTR0, A	MOVX @DPTR1, A
0	1	MOVX A, @DPTR1	MOVX A, @DPTR0	MOVX @DPTR1, A	MOVX @DPTR0, A
1	0	MOVX A, @DPTR0	MOVX B, @DPTR1	MOVX @DPTR0, A	MOVX @DPTR1, B
1	1	MOVX B, @DPTR1	MOVX A, @DPTR0	MOVX @DPTR1, B	MOVX @DPTR0, A

6.2 External Clock Source

The external clock option disables the oscillator amplifier and allows XTAL1 to be driven directly by an external clock source as shown in Figure 6-2. XTAL2 may be left unconnected, used as general purpose I/O P4.1, or configured to output a divided version of the system clock.

Figure 6-2. External Clock Drive Configuration



6.3 Internal RC Oscillator

The AT89LP3240/6440 has an Internal RC oscillator (IRC) tuned to 8.0 MHz ±2.5%. When enabled as the clock source, XTAL1 and XTAL2 may be used as P4.0 and P4.1 respectively. XTAL2 may also be configured to output a divided version of the system clock. The frequency of the oscillator may be adjusted within limits by changing the RC Calibration Byte stored at byte 128 of the User Signature Array. This location may be updated using the IAP interface (location 0180H in SIG space) or by an external device programmer (UROW location 0080H). See Section 25.8 “User Signature and Analog Configuration” on page 165. A copy of the factory calibration byte is stored at byte 8 of the Atmel Signature Array (0008H in SIG space).

6.4 System Clock Out

When the AT89LP3240/6440 is configured to use either an external clock or the internal RC oscillator, the system clock divided by 2 may be output on XTAL2 (P4.1). The clock out feature is enabled by setting the COE bit in CLKREG. For example, setting COE = “1” when using the internal oscillator will result in a 4.0 MHz (±2.5%) clock output on P4.1. P4.1 must be configured as an output in order to use the clock out feature.

6.5 System Clock Divider

The CDV_{2-0} bits in CLKREG allow the system clock to be divided down from the selected clock source by powers of 2. The clock divider provides users with a greater frequency range when using the Internal RC Oscillator. For example, to achieve a 1 MHz system frequency when using the IRC, CDV_{2-0} should be set to 011B for divide-by-8 operation. The divider can also be used to reduce power consumption by decreasing the operational frequency during non-critical periods. The resulting system frequency is given by the following equation:

$$f_{SYS} = \frac{f_{OSC}}{2^{CDV}}$$

where f_{OSC} is the frequency of the selected clock source. The clock divider will prescale the clock for the CPU and all peripherals. The value of CDV may be changed at any time without interrupting normal execution. Changes to CDV are synchronized such that the system clock will not

Note: During a power-up sequence, the fuse selection is always overridden and therefore the pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence if the pin will be configured as a general I/O, as this will keep the device in reset until the pin transitions high**. After the power-up delay, this input will function either as an external reset input or as a digital input as defined by the fuse bit. Only a power-up reset will temporarily override the selection defined by the reset fuse bit. Other sources of reset will not override the reset fuse bit. P4.2/$\overline{\text{RST}}$ also serves as the In-System Programming (ISP) enable. ISP is enabled when the external reset pin is held low. When the reset pin is disabled by the fuse, ISP may only be entered by pulling P4.2 low during power-up.

7.4 Watchdog Reset

When the Watchdog times out, it will generate an internal reset pulse lasting 16 clock cycles. Watchdog reset will also set the WDTOVF flag in WDTCON. To prevent a Watchdog reset, the watchdog reset sequence 1EH/E1H must be written to WDTRST before the Watchdog times out. See “Programmable Watchdog Timer” on page 141. for details on the operation of the Watchdog.

7.5 Software Reset

The CPU may generate an internal 16-clock cycle reset pulse by writing the software reset sequence 5AH/A5H to the WDRST register. A software reset will set the SWRST bit in WDTCON. See “Software Reset” on page 142 for more information on software reset. Writing any sequences other than 5AH/A5H or 1EH/E1H to WDTRST will generate an immediate reset and set both WDTOVF and SWRST to flag an error.

8. Power Saving Modes

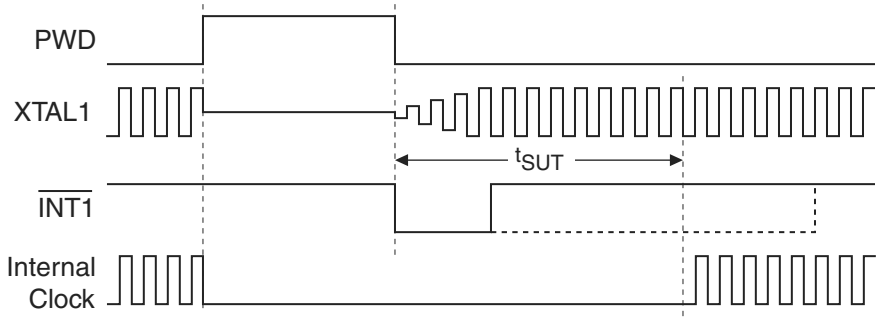
The AT89LP3240/6440 supports two different power-reducing modes: Idle and Power-down. These modes are accessed through the PCON register. Additional steps may be required to achieve the lowest possible power consumption while using these modes.

8.1 Idle Mode

Setting the IDL bit in PCON enters idle mode. Idle mode halts the internal CPU clock. The CPU state is preserved in its entirety, including the RAM, stack pointer, program counter, program status word, and accumulator. The Port pins hold the logic states they had at the time that Idle was activated. Idle mode leaves the peripherals running in order to allow them to wake up the CPU when an interrupt is generated. The timers, UART, SPI, TWI, comparators, ADC, GPI and CCA peripherals continue to function during Idle. If these functions are not needed during idle, they should be explicitly disabled by clearing the appropriate control bits in their respective SFRs. The watchdog may be selectively enabled or disabled during Idle by setting/clearing the WDIDLE bit. The Brown-out Detector, if enabled, is always active during Idle. Any enabled interrupt source or reset may terminate Idle mode. When exiting Idle mode with an interrupt, the interrupt will immediately be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into Idle.

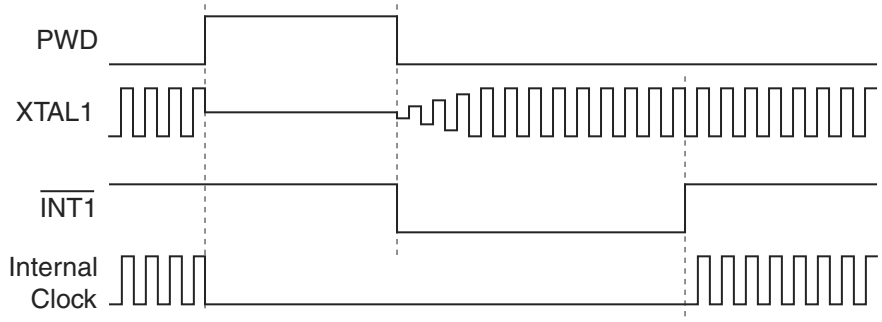
The power consumption during Idle mode can be further reduced by prescaling down the system clock using the System Clock Divider (Section 6.5 on page 32). Be aware that the clock divider will affect all peripheral functions except the ADC. Therefore baud rates or PWM periods may need to be adjusted to maintain their rate with the new clock frequency.

Figure 8-1. Interrupt Recovery from Power-down (PWDEX = 0)



When PWDEX = “1”, the wake-up period is controlled externally by the interrupt. Again, at the falling edge on the interrupt pin, power-down is exited and the oscillator is restarted. However, the internal clock will not propagate until the rising edge of the interrupt pin as shown in Figure 8-2. The interrupt pin should be held low long enough for the selected clock source to stabilize. After the rising edge on the pin the interrupt service routine will be executed.

Figure 8-2. Interrupt Recovery from Power-down (PWDEX = 1)



8.2.2 Reset Recovery from Power-down

The wake-up from Power-down through an external reset is similar to the interrupt with PWDEX = “0”. At the falling edge of $\overline{RST}$, Power-down is exited, the oscillator is restarted, and an internal timer begins counting as shown in Figure 8-3. The internal clock will not be allowed to propagate to the CPU until after the timer has timed out. The time-out period is controlled by the Start-up Timer Fuses. (See Table 7-1 on page 35). If $\overline{RST}$ returns high before the time-out, a two clock cycle internal reset is generated when the internal clock restarts. Otherwise, the device will remain in reset until $\overline{RST}$ is brought high.

8.3 Reducing Power Consumption

Several possibilities need consideration when trying to reduce the power consumption in an AT89LP-based system. Generally, Idle or Power-down mode should be used as much as possible. All unneeded functions should be disabled. In particular, the following modules may need special consideration when trying to achieve the lowest possible power consumption.

8.3.1 Brown-out Detector

If the Brown-out Detector is not needed by the application, this module should be turned off. If the Brown-out Detector is enabled by the BOD Enable Fuse, it will be enabled in all modes except Power-down. See Section 25.7 “User Configuration Fuses” on page 164.

Table 10-6. Port Pin Alternate Functions

Port Pin	Configuration Bits		Alternate Function	Notes
	PxM0.y	PxM1.y		
P1.2	P1M0.2	P1M1.2	SDA	open-drain
			GPI2	
P1.3	P1M0.3	P1M1.3	SCL	open-drain
			GPI3	
P1.4	P1M0.4	P1M1.4	$\overline{SS}$	
			GPI4	
P1.5	P1M0.5	P1M1.5	MOSI	
			GPI5	
P1.6	P1M0.6	P1M1.6	MISO	
			GPI6	
P1.7	P1M0.7	P1M1.7	SCK	
			GPI7	
P2.0	P2M0.0	P2M1.0	CCA	
P2.1	P2M0.1	P2M1.1	CCB	
P2.2	P2M0.2	P2M1.2	CCC	
			DA+	input-only
P2.3	P2M0.3	P2M1.3	CCD	
			DA-	input-only
P2.4	P2M0.4	P2M1.4	AIN0	input-only
P2.5	P2M0.5	P2M1.5	AIN1	input-only
P2.6	P2M0.6	P2M1.6	AIN2	input-only
P2.7	P2M0.7	P2M1.7	AIN3	input-only
P3.0	P3M0.0	P3M1.0	RXD	
P3.1	P3M0.1	P3M1.1	TXD	
P3.2	P3M0.2	P3M1.2	$\overline{INT0}$	
P3.3	P3M0.3	P3M1.3	$\overline{INT1}$	
P3.4	P3M0.4	P3M1.4	T0	
P3.5	P3M0.5	P3M1.5	T1	
P3.6	P3M0.6	P3M1.6	$\overline{WR}$	
P3.7	P3M0.7	P3M1.7	$\overline{RD}$	
P4.2	P3M0.5	P3M1.5	$\overline{RST}$	$\overline{RST}$ must be disabled to use P4.2
P4.6	not configurable		CMPA	Pin is tied to comparator output
P4.7	not configurable		CMPB	Pin is tied to comparator output

<table>
<tr><th>Symbol</th><th>Function</th></tr>
<tr><td>PHS [2-0]</td><td>CCA Phase Mode. PWM channels may be grouped by 2, 3 or 4 such that only one channel in a group produces a pulse in any one period. The PHS[2-0] bits may only be written when the timer is not active, i.e. TR2 = 0.
<u>PHS2</u> <u>PHS1</u> <u>PHS0</u> <u>Phase Mode</u>
0 0 0 Disabled, all channels active
0 0 1 2-phase output on channels A & B
0 1 0 3-phase output on channels A, B & C
0 1 1 4-phase output on channels A, B, C & D
1 0 0 Dual 2-phase output on channels A & B and C & D
1 0 1 reserved
1 1 0 reserved
1 1 1 reserved</td></tr>
<tr><td>T2CM [1-0]</td><td>Timer 2 Count Mode.
<u>T2CM1</u> <u>T2CM0</u> <u>Count Mode</u>
0 0 Standard Timer 2 (up count: BOTTOM →MAX)
0 1 Clear on RCAP compare (up count: MIN →TOP)
1 0 Dual-slope with single update (up-down count: MIN →TOP →MIN)
1 1 Dual-slope with double update (up-down count: MIN →TOP →MIN)</td></tr>
<tr><td>T2OE</td><td>Timer 2 Output Enable. When T2OE = 1 and C/$\overline{T}$2 = 0, the T2 pin will toggle after every Timer 2 overflow.</td></tr>
<tr><td>DCEN</td><td>Timer 2 Down Count Enable. When Timer 2 operates in Auto-Reload mode and EXEN2 = 1, setting DCEN = 1 will cause Timer 2 to count up or down depending on the state of T2EX.</td></tr>
</table>

12.2 Capture Mode

In the Capture mode, Timer 2 is a fixed 16-bit timer or counter that counts up from MIN to MAX. An overflow from MAX to MIN sets bit TF2 in T2CON. If EXEN2 = 1, a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 and TF2 bits can generate an interrupt. Capture mode is illustrated in Figure 12-1. The Timer 2 overflow rate in Capture mode is given by the following equation:

$$\text{Capture Mode:} \qquad \text{Time-out Period} = \frac{65536}{\text{Oscillator Frequency}} \times (\text{TPS} + 1)$$

bit and prepares to receive the data bytes that follows. The slaves that are not addressed set their SM2 bits and ignore the data bytes. See “Automatic Address Recognition” on page 97.

The SM2 bit can be used to check the validity of the stop bit in Mode 1. In a Mode 1 reception, if SM2 = 1, the receive interrupt is not activated unless a valid stop bit is received.

Table 16-1. SCON – Serial Port Control Register

SCON Address = 98H — Reset Value = 0000 0000B

Bit Addressable

	SM0/FE	SM1	SM2	REN	TB8	RB8	T1	RI
Bit	7	6	5	4	3	2	1	0

(SMOD0 = 0/1)[1]

Symbol	Function
FE	Framing error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames and must be cleared by software. The SMOD0 bit must be set to enable access to the FE bit. FE will be set regardless of the state of SMOD0.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1 **SM0** / **SM1** / **Mode** / **Description** / **Baud Rate**[2] 0 / 0 / 0 / shift register / $f_{osc}/2$ or $f_{osc}/4$ or Timer 1 0 / 1 / 1 / 8-bit UART / variable (Timer 1 or Timer 2) 1 / 0 / 2 / 9-bit UART / $f_{osc}/32$ or $f_{osc}/16$ 1 / 1 / 3 / 9-bit UART / variable (Timer 1 or Timer 2)
SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 determines the idle state of the shift clock such that the clock is the inverse of SM2, i.e. when SM2 = 0 the clock idles high and when SM2 = 1 the clock idles low.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired. In Mode 0, setting TB8 enables Timer 1 as the shift clock generator.
RB8	In Modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Notes: 1. SMOD0 is located at PCON.6.
2. f_{osc} = oscillator frequency. The baud rate depends on SMOD1 (PCON.7).

16.3 More About Mode 0

In Mode 0, the UART is configured as a two wire half-duplex synchronous serial interface. Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted/received, with the LSB first. Figure 16-1 on page 90 shows a simplified functional diagram of the serial port in Mode 0 and associated timing. The baud rate is programmable to 1/2 or 1/4 the oscillator frequency by setting/clearing the SMOD1 bit. However, changing SMOD1 has an effect on the relationship between the clock and data as described below. The baud rate can also be generated by Timer 1 by setting TB8. Table 16-4 lists the baud rate options for Mode 0.

Table 16-4. Mode 0 Baud Rates

TB8	SMOD1	Baud Rate
0	0	$f_{SYS}/4$
0	1	$f_{SYS}/2$
1	0	(Timer 1 Overflow) / 4
1	1	(Timer 1 Overflow) / 2

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a “1” into the 9th position of the transmit shift register and tells the TX Control Block to begin a transmission. The internal timing is such that one full bit slot may elapse between “write to SBUF” and activation of SEND.

SEND transfers the output of the shift register to the alternate output function line of P3.0, and also transfers Shift Clock to the alternate output function line of P3.1. As data bits shift out to the right, “0”s come in from the left. When the MSB of the data byte is at the output position of the shift register, the “1” that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain “0”s. This condition flags the TX Control block to do one last shift, then deactivate SEND and set TI.

Reception is initiated by the condition REN = 1 and R1 = 0. At the next clock cycle, the RX Control unit writes the bits 11111110 to the receive shift register and activates RECEIVE in the next clock phase. RECEIVE enables Shift Clock to the alternate output function line of P3.1. As data bits come in from the right, “1”s shift out to the left. When the “0” that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control block to do one last shift and load SBUF. Then RECEIVE is cleared and RI is set.

The relationship between the shift clock and data is determined by the combination of the SM2 and SMOD1 bits as listed in Table 16-5 and shown in Figure 16-2. The SM2 bit determines the idle state of the clock when not currently transmitting/receiving. The SMOD1 bit determines if the output data is stable for both edges of the clock, or just one.

Table 16-5. Mode 0 Clock and Data Modes

SM2	SMOD1	Clock Idle	Data Changed	Data Sampled
0	0	High	While clock is high	Positive edge of clock
0	1	High	Negative edge of clock	Positive edge of clock
1	0	Low	While clock is low	Negative edge of clock
1	1	Low	Negative edge of clock	Positive edge of clock

Symbol	Function
SPR0 SPR1	SPI clock rate select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{OSC.}$, is as follows: SPR1 SPR0 SCK (TSCK = 0) SCK (TSCK = 1) 0 0 $f_{OSC}/4$ $f_{T1OVF}/4$ 0 1 $f_{OSC}/8$ $f_{T1OVF}/8$ 1 0 $f_{OSC}/32$ $f_{T1OVF}/32$ 1 1 $f_{OSC}/64$ $f_{T1OVF}/64$

Notes: 1. Set up the clock mode before enabling the SPI: set all bits needed in SPCR except the SPE bit, then set SPE.
2. Enable the master SPI prior to the slave device.
3. Slave echoes master on the next Tx if not loaded with new data.

Table 17-3. SPDR – SPI Data Register

SPDR Address = EAH

Not Bit Addressable

Reset Value = 00H (after cold reset)
unchanged (after warm reset)

	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Bit	7	6	5	4	3	2	1	0

Table 17-4. SPSR – SPI Status Register

SPSR Address = E8H

Not Bit Addressable

Reset Value = 0000 X000B

	SPIF	WCOL	MODF	TXE	–	SSIG	DISSO	ENH
Bit	7	6	5	4	3	2	1	0

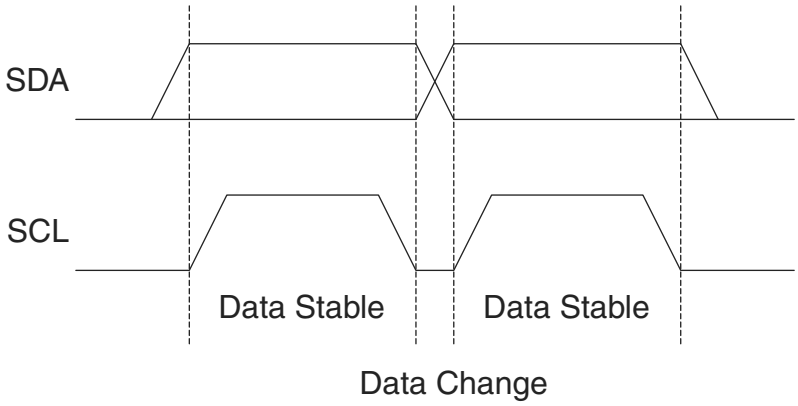
Symbol	Function
SPIF	SPI Transfer Complete Interrupt Flag. When a serial transfer is complete, the SPIF bit is set by hardware and an interrupt is generated if ESP = 1. The SPIF bit may be cleared by software or by reading the SPI status register followed by reading/writing the SPI data register.
WCOL	Write Collision Flag. The WCOL bit is set by hardware if SPDR is written while the transmit buffer is full. The ongoing transfer is not affected. WCOL may be cleared by software or by reading the SPI status register followed by reading/writing the SPI data register.
MODF	Mode Fault Flag. MODF is set by hardware when a master mode collision is detected (MSTR = 1, SSIG = 0 and $\overline{SS}$ = 0) and an interrupt is generated if ESP = 1. MODF must be cleared by software.
TXE	Transmit Buffer Empty Flag. Set by hardware when the transmit buffer is loaded into the shift register, allowing a new byte to be loaded. TXE must be cleared by software. When ENH = 1 and ESP = 1, TXE will generate an interrupt.

18.1 Data Transfer and Frame Format

18.1.1 Transferring Bits

Each data bit transferred on the TWI bus is accompanied by a pulse on the clock line. The level of the data line must be stable when the clock line is high. The only exception to this rule is for generating start and stop conditions.

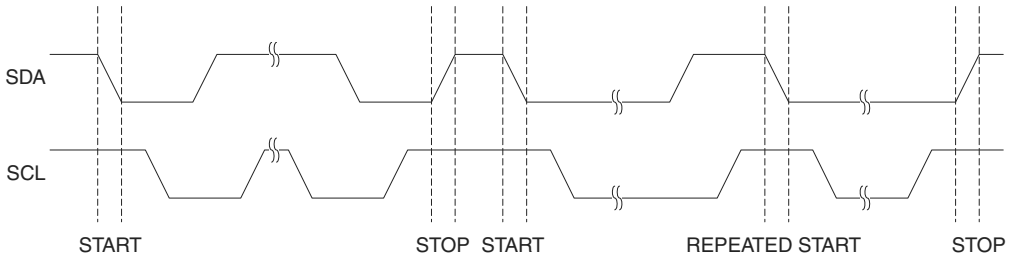
Figure 18-2. Data Validity



18.1.2 START and STOP Conditions

The Master initiates and terminates a data transmission. The transmission is initiated when the Master issues a START condition on the bus, and it is terminated when the Master issues a STOP condition. Between a START and a STOP condition, the bus is considered busy, and no other Master should try to seize control of the bus. A special case occurs when a new START condition is issued between a START and STOP condition. This is referred to as a REPEATED START condition, and is used when the Master wishes to initiate a new transfer without relinquishing control of the bus. After a REPEATED START, the bus is considered busy until the next STOP. This is identical to the START behavior, and therefore START is used to describe both START and REPEATED START for the remainder of this data sheet, unless otherwise noted. As depicted below, START and STOP conditions are signalled by changing the level of the SDA line when the SCL line is high.

Figure 18-3. START, REPEATED START, and STOP Conditions



18.1.3 Address Packet Format

All address packets transmitted on the TWI bus are nine bits long, consisting of seven address bits, one READ/$\overline{\text{WRITE}}$ control bit and an acknowledge bit. If the READ/$\overline{\text{WRITE}}$ bit is set, a read operation is to be performed, otherwise a write operation should be performed. When a slave recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle. If the addressed Slave is busy, or for some other reason can not service the Mas-

SLA: Slave Address

In Figure 18-11 to Figure 18-14, circles are used to indicate that the TWIF flag is set. The numbers in the circles show the status code held in TWSR. At these points, actions must be taken by the application to continue or complete the TWI transfer. The TWI transfer is suspended until the TWIF flag is cleared by software.

When the TWIF flag is set, the status code in TWSR is used to determine the appropriate software action. For each status code, the required software action and details of the following serial transfer are given in Table 18-6 to Table 18-9.

18.6.1 Master Transmitter Mode

In the Master Transmitter mode, a number of data bytes are transmitted to a Slave Receiver. In order to enter a Master mode, a START condition must be transmitted. The format of the following address packet determines whether Master Transmitter or Master Receiver mode is to be entered. If SLA+W is transmitted, MT mode is entered, if SLA+R is transmitted, MR mode is entered.

A START condition is sent by writing the following value to TWCR:

TWCR	–	TWEN	STA	STO	TWIF	AA	–	–
Value	X	1	1	0	0	X	X	X

TWEN must be set to enable the Two-wire Serial Interface, STA must be written to one to transmit a START condition and TWIF must be cleared. The TWI will then test the Two-wire Serial Bus and generate a START condition as soon as the bus becomes free. After a START condition has been transmitted, the TWIF flag is set by hardware, and the status code in TWSR will be 08h (see Table 18-6). In order to enter MT mode, SLA+W must be transmitted. This is done by writing SLA+W to TWDR. Thereafter the TWIF bit should be cleared to continue the transfer.

When SLA+W has been transmitted and an acknowledgment bit has been received, TWIF is set again and a number of status codes in TWSR are possible. Possible status codes in Master mode are 18h, 20h, or 38h. The appropriate action to be taken for each of these status codes is detailed in Table 18-6.

After SLA+W has been successfully transmitted, a data packet should be transmitted. This is done by writing the data byte to TWDR. TWDR must only be written when TWIF is high. If not, the access will be discarded and the previous value will be transmitted. After updating TWDR, the TWIF bit should be cleared to continue the transfer. This scheme is repeated until the last byte has been sent and the transfer is ended by generating a STOP condition or a repeated START condition. A STOP condition is generated by writing the following value to TWCR:

TWCR	–	TWEN	STA	STO	TWIF	AA	–	–
Value	X	1	0	1	0	X	X	X

A REPEATED START condition is generated by writing the following value to TWCR:

TWCR	–	TWEN	STA	STO	TWIF	AA	–	–
Value	X	1	1	0	0	X	X	X

After a repeated START condition (status 10h) the Two-wire Serial Interface can access the same slave again, or a new slave without transmitting a STOP condition. Repeated START enables the master to switch between slaves, Master Transmitter mode and Master Receiver mode without losing control of the bus.

Table 20-2. DADC – DADC Control Register

DADC = D9H — Reset Value = 0000 0000B

Not Bit Addressable

	ADIF	GO/BSY	DAC	ADCE	LADJ	ACK2	ACK1	ACK0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
ADIF	ADC Interrupt Flag. Set by hardware when a conversion completes. Cleared by hardware when calling the interrupt service routine.
GO/BSY	Conversion Start/Busy Flag. In software triggered mode, writing a 1 to this bit starts a conversion. The bit remains high while the conversion is in progress and is cleared by hardware when the conversion completes. In hardware triggered mode, this bit is set and cleared by hardware to flag when the DADC is busy.
DAC	Digital-to-Analog Conversion Enable. Set to configure the DADC in Digital-to-Analog (DAC) mode. Clear to configure the DADC in Analog-to-Digital (ADC) mode.
ADCE	DADC Enable. Set to enable the DADC. Clear to disable the DADC.
LADJ	Left Adjust Enable. When cleared, the ADC results are right adjusted and the MSBs are sign extended. When set, the ADC results are left adjusted and the LSBs are zeroed.
ACK [2-0]	DADC Clock Select

ACK3	ACK1	ACK0	Clock Source
0	0	0	Internal RC Oscillator/4 (2MHz)
0	0	1	$f_{sys}/2$
0	1	0	$f_{sys}/4$
0	1	1	$f_{sys}/8$
1	0	0	$f_{sys}/16$
1	0	1	$f_{sys}/32$
1	1	0	$f_{sys}/64$
1	1	1	$f_{sys}/128$

Table 20-3. DADL – DADC Data Low Register

DADL = DCH — Reset Value = 0000 0000B

Not Bit Addressable

	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	ADC.1	ADC.0
Bit	7	6	5	4	3	2	1	0

Table 20-4. DADH – DADC Data High Register

DADH = DDH — Reset Value = 0000 0000B

Not Bit Addressable

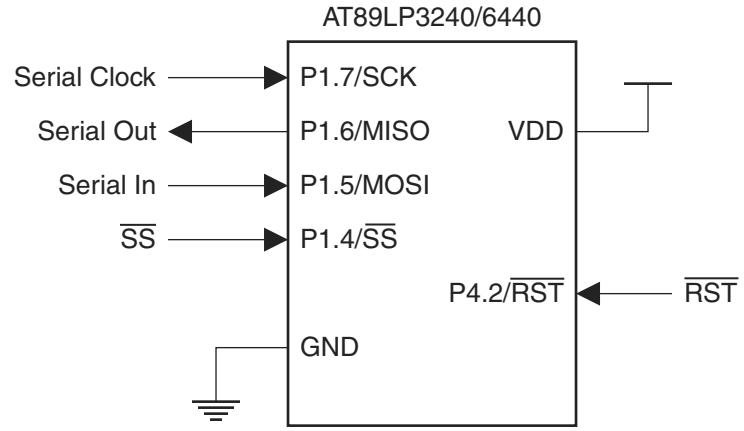
	ADC.15	ADC.14	ADC.13	ADC.12	ADC.11	ADC.10	ADC.9	ADC.8
Bit	7	6	5	4	3	2	1	0

Table 22-1. Instruction Execution Times and Exceptions (Continued)

POP direct	2	24	2/3[4]	D0
XCH A, Rn	1	12	1	C8-CF
XCH A, direct	2	12	2	C5
XCH A, @Ri	1	12	2	C6-C7
XCHD A, @Ri	1	12	2	D6-D7
		Clock Cycles		
Branching	**Bytes**	**8051**	**AT89LP**	**Hex Code**
JC rel	2	24	3	40
JNC rel	2	24	3	50
JB bit, rel	3	24	4	20
JNB bit, rel	3	24	4	30
JBC bit, rel	3	24	4	10
JZ rel	2	24	3	60
JNZ rel	2	24	3	70
SJMP rel	2	24	3	80
ACALL addr11	2	24	3/5[4]	11,31,51,71,91, B1,D1,F1
LCALL addr16	3	24	4/6[4]	12
RET	1	24	4/5[4]	22
RETI	1	24	4/5[4]	32
AJMP addr11	2	24	3	01,21,41,61,81, A1,C1,E1
LJMP addr16	3	24	4	02
JMP @A+DPTR	1	24	2	73
JMP @A+PC[1]	2	–	3	A5 73
CJNE A, direct, rel	3	24	4	B5
CJNE A, #data, rel	3	24	4	B4
CJNE Rn, #data, rel	3	24	4	B8-BF
CJNE @Ri, #data, rel	3	24	4	B6-B7
CJNE A, @R0, rel[1]	3	–	4	A5 B6
CJNE A, @R1, rel[1]	3	–	4	A5 B7
DJNZ Rn, rel	2	24	3	D8-DF
DJNZ direct, rel	3	24	4	D5
NOP	1	12	1	00
BREAK[1][3]	2	–	2	A5 00

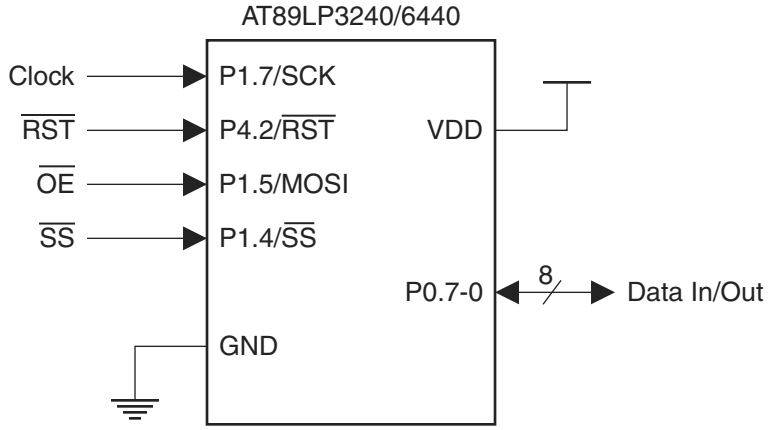
Notes:
1. This escaped instruction is an extension to the instruction set. See Section 22.1 on page 147.
2. MOVX @DPTR instructions take 2 clock cycles when accessing ERAM and 4 clock cycles when accessing FDATA, XDATA or CODE. (3 and 5 cycles for MOVX @/DPTR).
3. The BREAK instruction acts as a 2 cycle NOP.
4. Instructions accessing the stack require additional cycles when using the extended stack.

Figure 25-1. In-System Programming Device Connections



The Parallel interface is a special mode of the serial interface, i.e. the serial interface is used to enable the parallel interface. After enabling the interface serially over P1.7/SCK and P1.5/MOSI, P1.5 is reconfigured as an active-low output enable ($\overline{OE}$) for data on Port 0. When $\overline{OE}$ = 1, command, address and write data bytes are input on Port 0 and sampled at the rising edge of SCK. When $\overline{OE}$ = 0, read data bytes are output on Port 0 and should be sampled on the falling edge of SCK. The P1.7/SCK, P1.4/$\overline{SS}$ and P4.2/$\overline{RST}$ pins continue to function in the same manner. With the addition of VDD and GND, the parallel interface requires a minimum of fourteen connections as shown in Figure 25-2. Note that a connection to P1.6/MISO is not required for using the parallel interface.

Figure 25-2. Parallel Programming Device Connections



The Programming Interface is the only means of externally programming the AT89LP3240/6440 microcontroller. The Interface can be used to program the device both in-system and in a standalone serial programmer. The Interface does not require any clock other than SCK and is not limited by the system clock frequency. During Programming the system clock source of the target device can operate normally.

When designing a system where In-System Programming will be used, the following observations must be considered for correct operation:

25.8 User Signature and Analog Configuration

The User Signature Array contains 256 bytes of non-volatile memory in two 128-byte pages. The first page of the User Signature Array (0000H–007FH) is available for serial numbers, firmware revision information, date codes or other user parameters. The User Signature Array may only be written by an external device when the User Signature Programming Fuse is enabled. When the fuse is enabled, Chip Erase will also erase the first page of the array. When the fuse is disabled, the array is not affected by write or erase commands. Programming of the Signature Array can also be disabled by the Lock Bits. However, reading the signature is always allowed and the array should not be used to store security sensitive information. The User Signature Array may be modified during execution through the In-Application Programming interface, regardless of the state of the User Signature Programming fuse or Lock Bits, provided that the IAP Fuse is enabled. Note that the address of the User Signature Array, as seen by the IAP interface, equals the User Signature address plus 256 (0100H–01FFH instead of 0000H–00FFH).

The second page of the User Signature Array (0080H–00FFH) contains analog configuration parameters for the AT89LP3240/6440. Each byte represents a parameter as listed in Table 25-6 and is preset in the factory. The parameters are read at POR and the device is configured accordingly. The second page of the array is not affected by Chip Erase. Other bytes in this page may be used as additional signature space; however, care should be taken to preserve the parameter values when modifying other bytes.

Table 25-6. Analog Configuration Definitions

Address	Parameter Name	Description
0080H	RC Oscillator Calibration Byte	The RC Calibration Byte controls the frequency of the internal RC oscillator. The frequency is inversely proportional to the calibration value such that higher values result in lower frequencies. A copy of the factory-set calibration value is stored at location 0008H of the Atmel Signature.

25.9 Programming Interface Timing

This section details general system timing sequences and constraints for entering or exiting In-System Programming as well as parameters related to the Serial Peripheral Interface during ISP. The general timing parameters for the following waveform figures are listed in section “Timing Parameters” on page 169.

25.9.1 Power-up Sequence

Execute this sequence to enter programming mode immediately after power-up. In the $\overline{RST}$ pin is disabled or if the ISP Fuse is disabled, this is the only method to enter programming (see “External Reset” on page 35).

1. Apply power between VDD and GND pins. $\overline{RST}$ should remain low.
2. Wait at least t_{PWRUP} and drive $\overline{SS}$ high.
3. Wait at least t_{SUT} for the internal Power-on Reset to complete. The value of t_{SUT} will depend on the current settings of the device.
4. Start programming session.

3. Parameter t_{LHLL} applies only when ALES = 1.
4. The strobe pulse width may be lengthened by 1, 2 or 3 additional t_{CLCL} using wait states.
5. Parameter t_{WHLH} applies only when ALES = 0, or when two MOVX instructions occur in succession.

Figure 26-15. External Data Memory Read Cycle

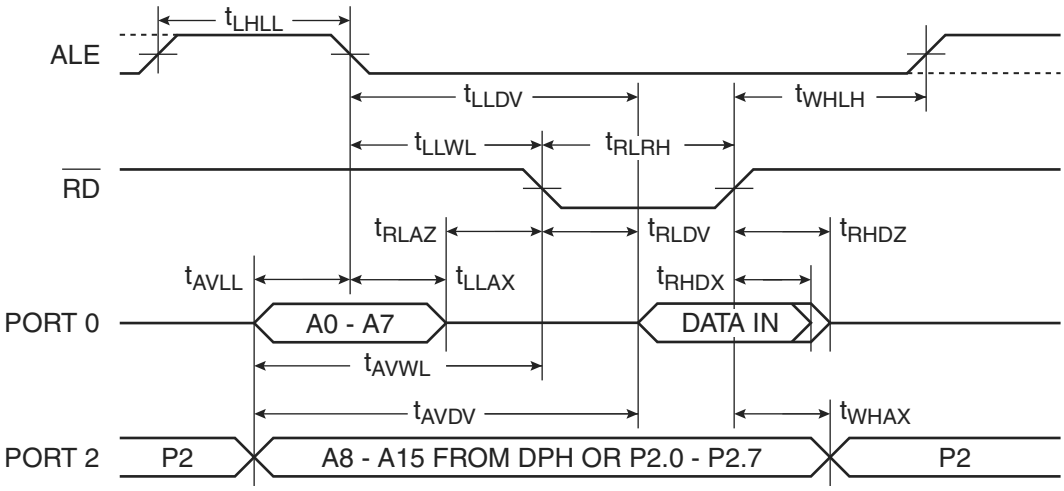
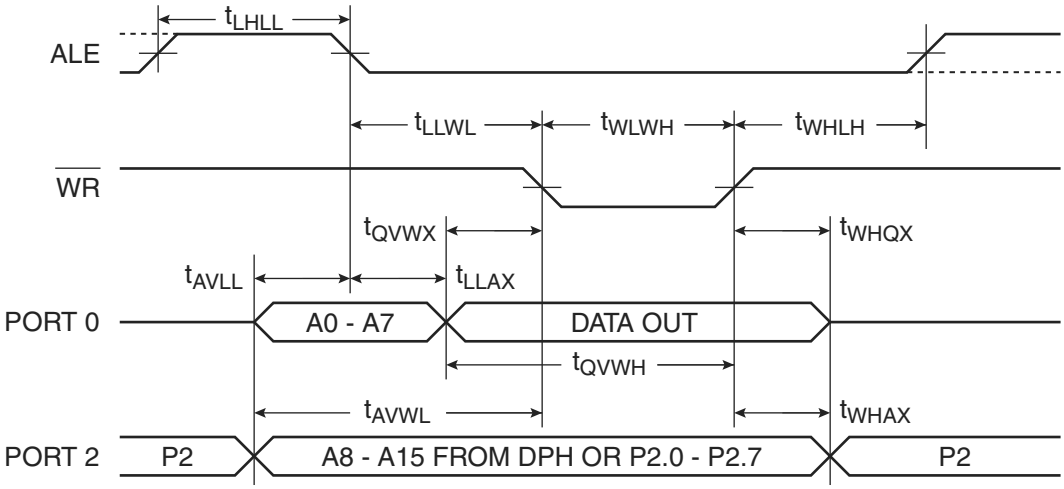


Figure 26-16. External Data Memory Write Cycle



26.8 Serial Peripheral Interface Timing

The values shown in these tables are valid for T_A = -40°C to 85°C and V_{DD} = 2.4 to 3.6V, unless otherwise noted.

Table 26-5. SPI **Master** Characteristics

Symbol	Parameter	Min	Max	Units
t_{CLCL}	Oscillator Period	41.6		ns
t_{SCK}	Serial Clock Cycle Time	$4t_{CLCL}$		ns
t_{SHSL}	Clock High Time	$t_{SCK}/2$ - 25		ns
t_{SLSH}	Clock Low Time	$t_{SCK}/2$ - 25		ns
t_{SR}	Rise Time		25	ns
t_{SF}	Fall Time		25	ns

29. Revision History

Revision No.	History
Revision A – September 2009	• Initial Release
Revision B– September 2010	• Removed Preliminary status • Updated “DC Characteristics” on page 170 • Updated “Typical Characteristics” on page 171 • Renamed AVDD to VDD
Revision C– February 2011	• Added section “System Configuration” on page 8 • Added the AT89LP3240 device • Updated oscillator connection diagram, Figure 6-1 on page 31

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