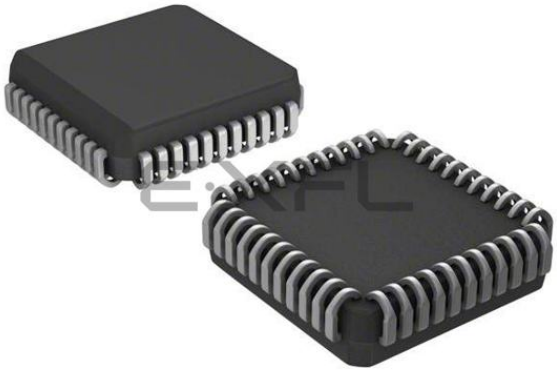


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

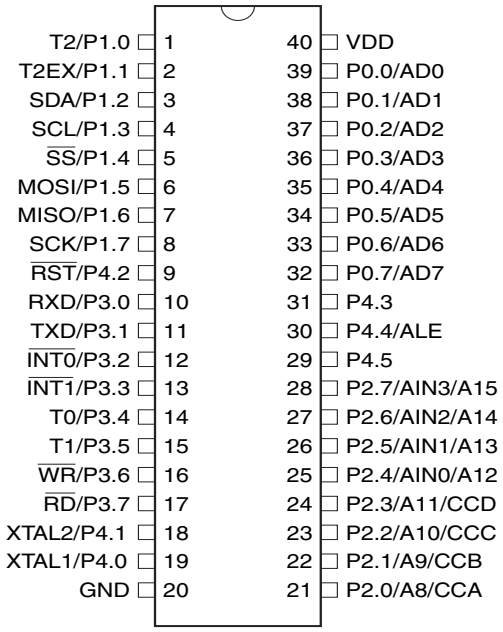
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

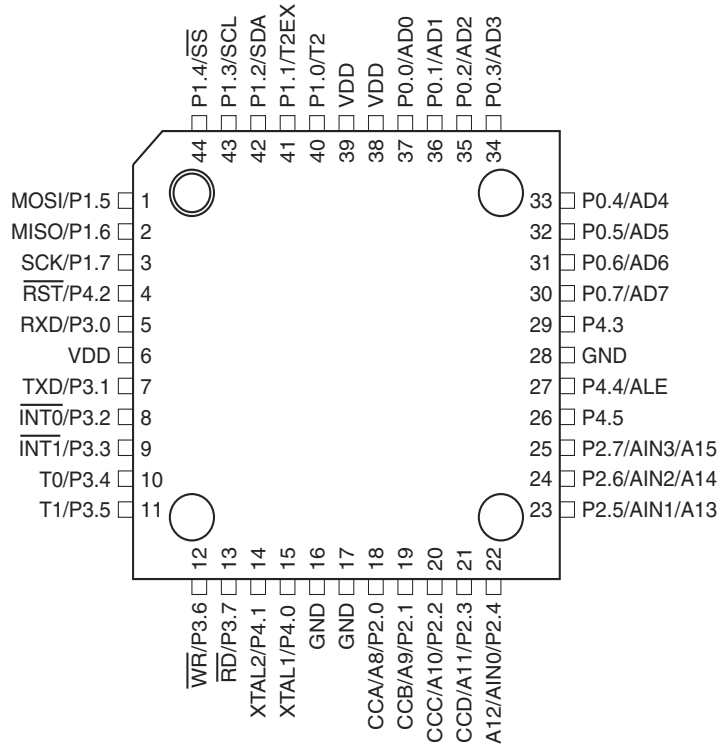
Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp6440-20ju

1. Pin Configurations

1.1 40P6: 40-lead PDIP



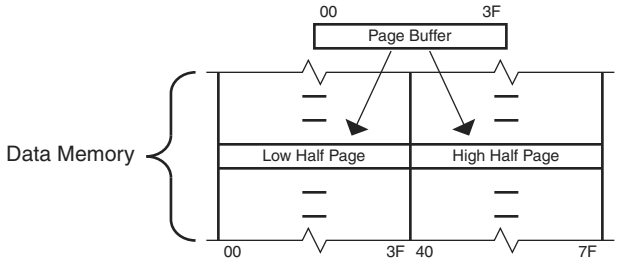
1.2 44A: 44-lead TQFP (Top View)



To enable write access to the nonvolatile data memory, the MWEN bit (MEMCON.4) must be set to one. When MWEN = 1 and DMEN = 1, MOVX @DPTR,A may be used to write to FDATA. FDATA uses flash memory with a page-based programming model. Flash data memory differs from traditional EEPROM data memory in the method of writing data. EEPROM generally can update a single byte with any value. Flash memory splits programming into write and erase operations. A Flash write can only program zeroes, i.e change ones into zeroes ($1 \rightarrow 0$). Any ones in the write data are ignored. A Flash erase sets an entire page of data to ones so that all bytes become FFH. Therefore after an erase, each byte in the page can be written only once with any possible value. Bytes can not be overwritten once they are changed from the erased state without possibility of corrupting the data. Therefore, if even a single byte needs updating; then the contents of the page must first be saved, the entire page must be erased and the zero bits in all bytes (old and new data combined) must be written. Avoiding unnecessary page erases greatly improves the endurance of the memory.

The AT89LP3240/6440 includes 64 data pages of 128 bytes each. One or more bytes in a page may be written at one time. The AT89LP3240/6440 includes a temporary page buffer of 64 bytes, or half of a page. Because the page buffer is 64 bytes long, the maximum number of bytes written at one time is 64. Therefore, two write cycles are required to fill the entire 128-byte page, one for the low half page (00H–3FH) and one for the high half page (40H–7FH) as shown in Figure 3-4.

Figure 3-4. Page Programming Structure



The LDPG bit (MEMCON.5) allows multiple data bytes to be loaded to the temporary page buffer. While LDPG = 1, MOVX @DPTR,A instructions will load data to the page buffer, but will not start a write sequence. Note that a previously loaded byte must not be reloaded prior to the write sequence. To write the half page into the memory, LDPG must first be cleared and then a MOVX @DPTR,A with the final data byte is issued. The address of the final MOVX determines which half page will be written. If a MOVX @DPTR,A instruction is issued while LDPG = 0 without loading any previous bytes, only a single byte will be written. The page buffer is reset after each write operation. Figures 3-5 and Figure 3-6 on page 16 show the difference between byte writes and page writes.

The auto-erase bit AERS (MEMCON.6) can be set to one to perform a page erase automatically at the beginning of any write sequence. The page erase will erase the entire page, i.e. both the low and high half pages. However, the write operation paired with the auto-erase can only program one of the half pages. A second write cycle without auto-erase is required to update the other half page.

Figure 3-8 shows a hardware configuration for accessing 256-byte blocks of external RAM using an 8-bit paged address. Port 0 serves as a multiplexed address/data bus to the RAM. The ALE strobe is used to latch the address byte into an external register so that Port 0 can be freed for data input/output. The Port 2 I/O lines (or other ports) can provide control lines to page the memory; however, this operation is not handled automatically by hardware. The software application must change the Port 2 register when appropriate to access different pages. The MOVX @Ri instructions use Paged Address mode.

Figure 3-8. External Memory 8-bit Paged Address Mode

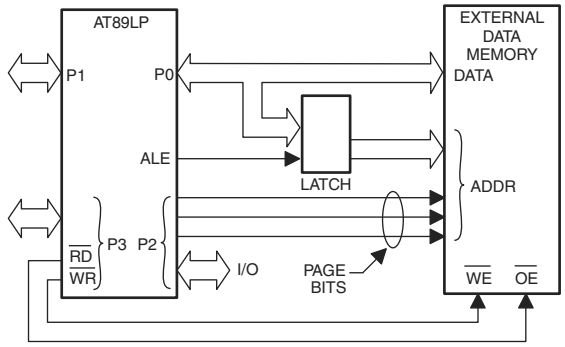


Table 3-4. AUXR – Auxiliary Control Register

AUXR = 8EH — Reset Value = xxx0 0000B

Not Bit Addressable

	–	–	–	XSTK	WS1	WS0	EXRAM	ALES
Bit	7	6	5	4	3	2	1	0

Symbol	Function
XSTK	Extended Stack Enable. When XSTK = 0 the stack resides in IDATA and is limited to 256 bytes. Set XSTK = 1 to place the stack in EDATA for up to 4K bytes of extended stack space. All PUSH, POP, CALL and RET instructions will incur a one or two cycle penalty when accessing the extended stack.
WS[1-0]	Wait State Select. Determines the number of wait states inserted into external memory accesses. WS1 / WS0 / Wait States / $\overline{RD}$ / $\overline{WR}$ Strobe Width 0 0 0 1 x t_{CYC} 0 1 1 2 x t_{CYC} 1 0 2 3 x t_{CYC} 1 1 3 4 x t_{CYC}
EXRAM	External RAM Enable. When EXRAM = 0, MOVX instructions can access the internally mapped portions of the address space. Accesses to addresses above internally mapped memory will access external memory. Set EXRAM = 1 to bypass the internal memory and map the entire address space to external memory.
ALES	ALE Idle State. When ALES = 0 the idle polarity of ALE is high (active). When ALES = 1 the idle polarity of ALE is low (inactive). The ALE strobe pulse is always active high. ALES must be zero in order to use P4.4 as a general I/O.

Note that prior to using the external memory interface, Port 2, $\overline{WR}$ (P3.6), $\overline{RD}$ (P3.7) and ALE (P4.4) must be configured as outputs. See Section 10.1 “Port Configuration” on page 45. Port 0 is configured automatically to push-pull output mode when outputting address or data and is

5.3 Instruction Set Extensions

Table 5-8 lists the additions to the 8051 instruction set that are supported by the AT89LP3240/6440. For more information on the instruction set see Section 22. “Instruction Set Summary” on page 143. For detailed descriptions of the extended instructions see Section 22.1 “Instruction Set Extensions” on page 147.

Table 5-8. AT89LP3240/6440 Extended Instructions

Opcode	Mnemonic	Description	Bytes	Cycles
A5 00	BREAK	Software breakpoint	2	2
A5 03	ASR M	Arithmetic shift right of M register	2	2
A5 23	LSL M	Logical shift left of M register	2	2
A5 73	JMP @A+PC	Indirect jump relative to PC	2	3
A5 90	MOV /DPTR, #data16	Move 16-bit constant to alternate data pointer	4	4
A5 93	MOVC A, @A+/DPTR	Move code location to ACC relative to alternate data pointer	2	4
A5 A3	INC /DPTR	Increment alternate data pointer	2	3
A5 A4	MAC AB	Multiply and accumulate	2	9
A5 B6	CJNE A, @R0, rel	Compare ACC to indirect RAM and jump if not equal	3	4
A5 B7	CJNE A, @R1, rel	Compare ACC to indirect RAM and jump if not equal	3	4
A5 E0	MOVX A, @/DPTR	Move external to ACC; 16-bit address in alternate data pointer	2	3/5
A5 E4	CLR M	Clear M register	2	2
A5 F0	MOVX @/DPTR, A	Move ACC to external; 16-bit address in alternate data pointer	2	3/5

- The /DPTR instructions provide support for the dual data pointer features described above (See Section 5.2).
- The ASR M, LSL M, CLR M and MAC AB instructions are part of the Multiply-Accumulate Unit (See Section 5.1).
- The JMP @A+PC instruction supports localized jump tables without using a data pointer.
- The CJNE A, @R_i, rel instructions allow compares of array values with non-constant values.
- The BREAK instruction is used by the On-Chip Debug system. See Section 24. on page 155.

Table 9-3. IE2 – Interrupt Enable 2 Register

IE = B4H — Reset Value = xxxx x000B

Not Bit Addressable

	–	–	–	ETWI	EADC	ESPI	ECC	EGP
Bit	7	6	5	4	3	2	1	0

Symbol	Function
ETWI	Two-Wire Interface Interrupt Enable
EADC	ADC Interrupt Enable
ESPI	Serial Peripheral Interface Interrupt Enable
ECC	Compare/Capture Array Interrupt Enable
EGP	General-purpose Interrupt Enable

Table 9-4. IP – Interrupt Priority Register

IP = B8H — Reset Value = 0000 0000B

Bit Addressable

	IP0D	PC	PT2	PS	PT1	PX1	PT0	PX0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
IP0D	Interrupt Priority 0 Disable. Set IP0D to 1 to disable all interrupts with priority level zero. Clear to 0 to enable all interrupts with priority level zero when EA = 1.
PC	Comparator Interrupt Priority Low
PT2	Timer 2 Interrupt Priority Low
PS	Serial Port Interrupt Priority Low
PT1	Timer 1 Interrupt Priority Low
PX1	External Interrupt 1 Priority Low
PT0	Timer 0 Interrupt Priority Low
PX0	External Interrupt 0 Priority Low

Table 9-5. IP2 – Interrupt Priority 2 Register

IP = B5H — Reset Value = 0xxx x000B

No Bit Addressable

	IP2D	–	–	PTWI	PADC	PSP	PCC	PGP
Bit	7	6	5	4	3	2	1	0

Symbol	Function
IP2D	Interrupt Priority 2 Disable. Set IP2D to 1 to disable all interrupts with priority level two. Clear to 0 to enable all interrupts with priority level two when EA = 1.
PTWI	Two-wire Interface Interrupt Priority Low
PADC	ADC Interrupt Priority Low

Symbol	Function
PSP	Serial Peripheral Interface Interrupt Priority Low
PCC	Compare/Capture Array Interrupt Priority Low
PGP	General-purpose Interrupt 0 Priority Low

Table 9-6. IPH – Interrupt Priority High Register

IPH = B7H — Reset Value = 0000 0000B

Not Bit Addressable

	IP1D	PCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
Bit	7	6	5	4	3	2	1	0

Symbol	Function
IP1D	Interrupt Priority 1 Disable. Set IP1D to 1 to disable all interrupts with priority level one. Clear to 0 to enable all interrupts with priority level one when EA = 1.
PCH	Comparator Interrupt Priority High
PT2H	Timer 2 Interrupt Priority High
PSH	Serial Port Interrupt Priority High
PT1H	Timer 1 Interrupt Priority High
PX1H	External Interrupt 1 Priority High
PT0H	Timer 0 Interrupt Priority High
PX0H	External Interrupt 0 Priority High

Table 9-7. IP2H – Interrupt Priority 2 High Register

IPH = B6H — Reset Value = 0xxx x000B

Not Bit Addressable

	IP3D	–	–	PTWH	PADH	PSPH	PCCH	PGPH
Bit	7	6	5	4	3	2	1	0

Symbol	Function
IP3D	Interrupt Priority 3 Disable. Set IP3D to 1 to disable all interrupts with priority level three. Clear to 0 to enable all interrupts with priority level three when EA = 1.
PTWH	Two-Wire Interface Interrupt Priority High
PADH	ADC Interrupt Priority High
PSPH	Serial Peripheral Interface Interrupt Priority High
PCCH	Compare/Capture Array Interrupt Priority High
PGPH	General-purpose Interrupt 0 Priority High

Table 11-4. TCONB – Timer/Counter Control Register B

TCONB = 91H — Reset Value = 0010 0100B

Not Bit Addressable

	PWM1EN	PWM0EN	PSC12	PSC11	PSC10	PSC02	PSC01	PSC00
Bit	7	6	5	4	3	2	1	0

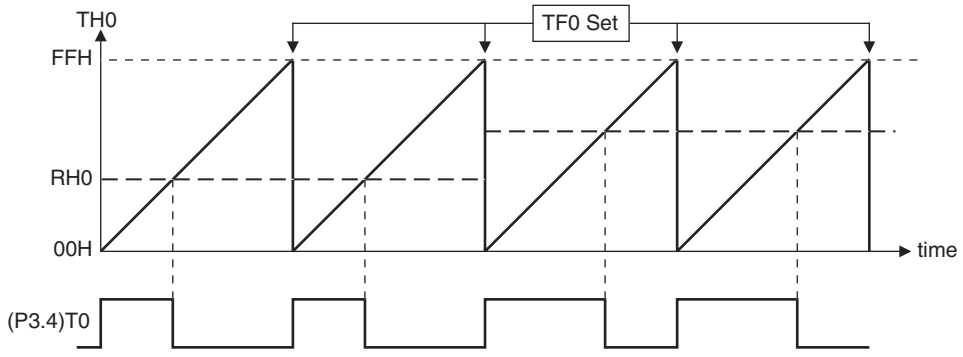
Symbol	Function
PWM1EN	Configures Timer 1 for Pulse Width Modulation output on T1 (P3.5).
PWM0EN	Configures Timer 0 for Pulse Width Modulation output on T0 (P3.4).
PSC12 PSC11 PSC10	Prescaler for Timer 1 Mode 0. The number of active bits in TL1 equals PSC1 + 1. After reset PSC1 = 100B which enables 5 bits of TL1 for compatibility with the 13-bit Mode 0 in AT89S2051.
PSC02 PSC01 PSC00	Prescaler for Timer 0 Mode 0. The number of active bits in TL0 equals PSC0 + 1. After reset PSC0 = 100B which enables 5 bits of TL0 for compatibility with the 13-bit Mode 0 in AT89C52.

11.5 Pulse Width Modulation

On the AT89LP3240/6440, Timer 0 and Timer 1 may be independently configured as 8-bit asymmetrical (edge-aligned) pulse width modulators (PWM) by setting the PWM0EN or PWM1EN bits in TCONB, respectively. In PWM Mode the generated waveform is output on the timer's input pin, T0 or T1. Therefore, C/$\overline{T}$x must be set to “0” when in PWM mode and the T0 (P3.4) and T1 (P3.5) must be configured in an output mode. The Timer Overflow Flags and Interrupts will continue to function while in PWM Mode and Timer 1 may still generate the baud rate for the UART. The timer GATE function also works in PWM mode, allowing the output to be halted by an external input. Each PWM channel has four modes selected by the mode bits in TMOD.

An example waveform for Timer 0 in PWM Mode 0 is shown in Figure 11-5. TH0 acts as an 8-bit counter while RH0 stores the 8-bit compare value. When TH0 is 00H the PWM output is set high. When the TH0 count reaches the value stored in RH0 the PWM output is set low. Therefore, the pulse width is proportional to the value in RH0. To prevent glitches, writes to RH0 only take effect on the FFH to 00H overflow of TH0. Setting RH0 to 00H will keep the PWM output low.

Figure 11-5. 8-bit Asymmetrical Pulse Width Modulation



12. Enhanced Timer 2

The AT89LP3240/6440 includes a 16-bit Timer/Counter 2 with the following features:

- 16-bit timer/counter with one 16-bit reload/capture register
- One external reload/capture input
- Up/Down counting mode with external direction control
- UART baud rate generation
- Output-pin toggle on timer overflow
- Dual slope symmetric operating modes

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON. Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON and T2MOD, as shown in Table 12-3. Timer 2 also serves as the time base for the Compare/Capture Array (See Section 13. “Compare/Capture Array” on page 69).

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the register is incremented every clock cycle. Since a clock cycle consists of one oscillator period, the count rate is equal to the oscillator frequency. The timer rate can be prescaled by a value between 1 and 16 using the Timer Prescaler (see Table 6-2 on page 33).

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled every clock cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since two clock cycles are required to recognize a 1-to-0 transition, the maximum count rate is 1/2 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full clock cycle.

Table 12-1. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	DCEN	T2OE	TR2	MODE
0	0	0	0	1	16-bit Auto-reload
0	0	1	0	1	16-bit Auto-reload Up-Down
0	1	X	0	1	16-bit Capture
1	X	X	X	1	Baud Rate Generator
X	X	X	1	1	Frequency Generator
X	X	X	X	0	(Off)

The following definitions for Timer 2 are used in the subsequent paragraphs:

Table 12-2. Timer 2 Definitions

Symbol	Definition
MIN	0000H
MAX	FFFFH
BOTTOM	16-bit value of {RCAP2H,RCAP2L} (standard modes)
TOP	16-bit value of {RCAP2H,RCAP2L} (enhanced modes)

Table 13-6. Summary of Multi-Phasic Modes

PHS_{2-0}	Mode	Behavior	
		PHSD = 0	PHSD = 1
000	Off	Normal Operation (all channels active at all times)	
001	1:2	A →B →A →B	B →A →B →A
010	1:3	A →B →C →A →B →C	C →B →A →C →B →A
011	1:4	A →B →C →D →A →B →C →D	D →C →B →A →D →C →B →A
100	2:4	A →B →A →B C →D →C →D	B →A →B →A D →C →D →C

Figure 13-12. Multi-Phasic PWM Output Stage

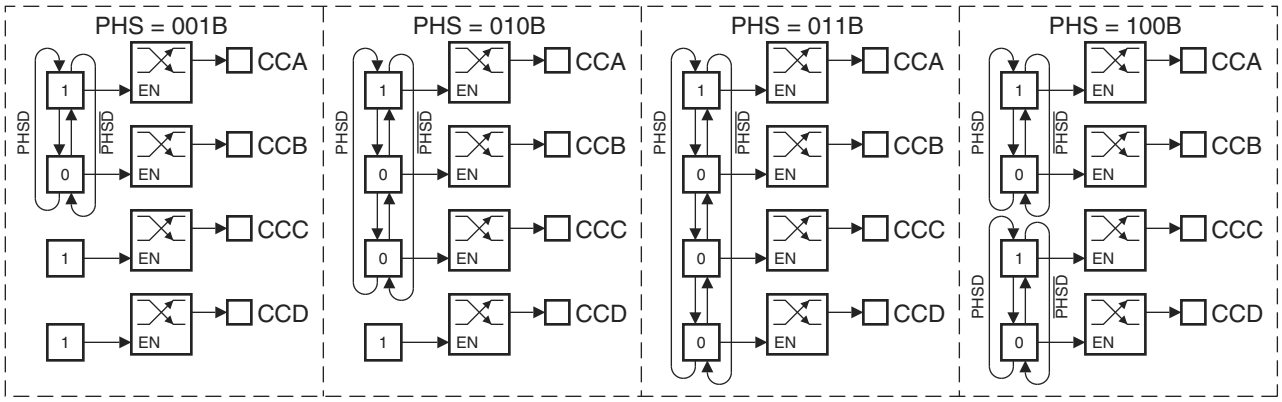
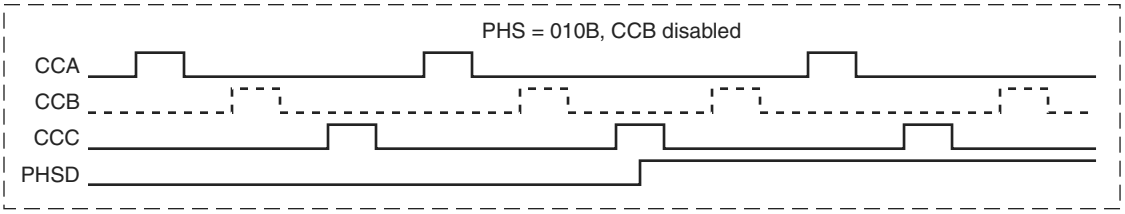


Figure 13-13. Three-Phase Mode with Channel B Disabled



bit and prepares to receive the data bytes that follows. The slaves that are not addressed set their SM2 bits and ignore the data bytes. See “Automatic Address Recognition” on page 97.

The SM2 bit can be used to check the validity of the stop bit in Mode 1. In a Mode 1 reception, if SM2 = 1, the receive interrupt is not activated unless a valid stop bit is received.

Table 16-1. SCON – Serial Port Control Register

SCON Address = 98H — Reset Value = 0000 0000B

Bit Addressable

	SM0/FE	SM1	SM2	REN	TB8	RB8	T1	RI
Bit	7	6	5	4	3	2	1	0

(SMOD0 = 0/1)[1]

Symbol	Function
FE	Framing error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames and must be cleared by software. The SMOD0 bit must be set to enable access to the FE bit. FE will be set regardless of the state of SMOD0.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1 **SM0** / **SM1** / **Mode** / **Description** / **Baud Rate**[2] 0 / 0 / 0 / shift register / $f_{osc}/2$ or $f_{osc}/4$ or Timer 1 0 / 1 / 1 / 8-bit UART / variable (Timer 1 or Timer 2) 1 / 0 / 2 / 9-bit UART / $f_{osc}/32$ or $f_{osc}/16$ 1 / 1 / 3 / 9-bit UART / variable (Timer 1 or Timer 2)
SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 determines the idle state of the shift clock such that the clock is the inverse of SM2, i.e. when SM2 = 0 the clock idles high and when SM2 = 1 the clock idles low.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired. In Mode 0, setting TB8 enables Timer 1 as the shift clock generator.
RB8	In Modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Notes: 1. SMOD0 is located at PCON.6.
2. f_{osc} = oscillator frequency. The baud rate depends on SMOD1 (PCON.7).

16.5 More About Modes 2 and 3

Eleven bits are transmitted (through TXD), or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of “0” or “1”. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/16 or 1/32 of the oscillator frequency in Mode 2. Mode 3 may have a variable baud rate generated from either Timer 1 or Timer 2, depending on the state of RCLK and TCLK.

Figures 16-5 and 16-6 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.

The transmission begins when $\overline{\text{SEND}}$ is activated, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that. The first shift clocks a “1” (the stop bit) into the 9th bit position of the shift register. Thereafter, only “0”s are clocked in. Thus, as data bits shift out to the right, “0”s are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain “0”s. This condition flags the TX Control unit to do one last shift, then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a 1-to-0 transition detected at RXD. For this purpose, RXD is sampled at a rate of 16 times the established baud rate. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit continues looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame proceeds.

As data bits come in from the right, “1”s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8 and to set RI is generated if, and only if, the following conditions are met at the time the final shift pulse is generated:

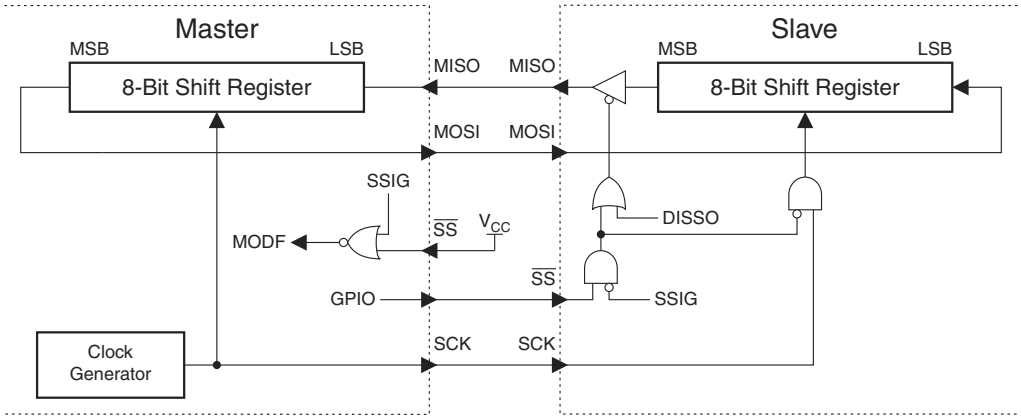
RI = 0, and

Either SM2 = 0 or the received 9th data bit = 1

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit continues looking for a 1-to-0 transition at the RXD input.

Note that the value of the received stop bit is irrelevant to SBUF, RB8, or RI.

Figure 17-2. SPI Master-Slave Interconnection



When the SPI is configured as a Master (MSTR in SPCR is set), the operation of the $\overline{SS}$ pin depends on the setting of the Slave Select Ignore bit, SSIG. If SSIG = 1, the $\overline{SS}$ pin is a general purpose output pin which does not affect the SPI system. Typically, the pin will be driving the $\overline{SS}$ pin of an SPI Slave. If SSIG = 0, $\overline{SS}$ must be held high to ensure Master SPI operation. If the $\overline{SS}$ pin is driven low by peripheral circuitry when the SPI is configured as a Master with SSIG = 0, the SPI system interprets this as another master selecting the SPI as a slave and starting to send data to it. To avoid bus contention, the SPI system takes the following actions:

1. The MSTR bit in SPCR is cleared and the SPI system becomes a Slave. As a result of the SPI becoming a Slave, the MOSI and SCK pins become inputs.
2. The MODF Flag in SPSR is set, and if the SPI interrupt is enabled, the interrupt routine will be executed.

Thus, when interrupt-driven SPI transmission is used in Master mode, and there exists a possibility that $\overline{SS}$ may be driven low, the interrupt should always check that the MSTR bit is still set. If the MSTR bit has been cleared by a slave select, it must be set by the user to re-enable SPI Master mode.

17.1 Master Operation

An SPI master device initiates all data transfers on the SPI bus. The AT89LP3240/6440 is configured for master operation by setting MSTR = 1 in SPCR. Writing to the SPI data register (SPDR) while in master mode loads the transmit buffer. If the SPI shift register is empty, the byte in the transmit buffer is moved to the shift register; the transmit buffer empty flag, TXE, is set; and a transmission begins. The transfer may start after an initial delay, while the clock generator waits for the next full bit slot of the specified baud rate. The master shifts the data out serially on the MOSI line while providing the serial shift clock on SCK. When the transfer finishes, the SPIF flag is set to “1” and an interrupt request is generated, if enabled. The data received from the addressed SPI slave device is also transferred from the shift register to the receive buffer. Therefore, the SPIF bit flags both the transmit-complete and receive-data-ready conditions. The received data is accessed by reading SPDR.

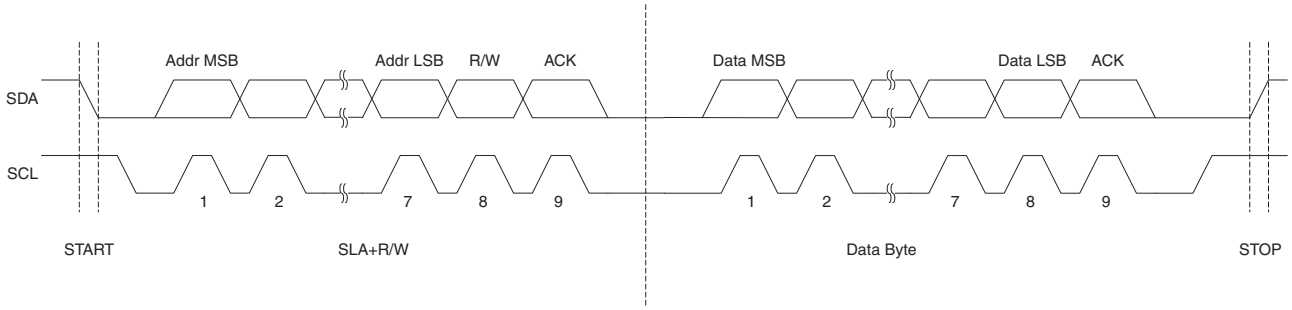
While the TXE flag is set, the transmit buffer is empty. TXE can be cleared by software or by writing to SPDR. Writing to SPDR will clear TXE and load the transmit buffer. The user may load the buffer while the shift register is busy, i.e. before the current transfer completes. When the current transfer completes, the queued byte in the transmit buffer is moved to the shift register and the next transfer commences. TXE will generate an interrupt if the SPI interrupt is enabled

18.1.5 Combining Address and Data Packets Into a Transmission

A transmission basically consists of a START condition, a SLA+R/W, one or more data packets and a STOP condition. An empty message, consisting of a START followed by a STOP condition, is illegal. Note that the wired-ANDing of the SCL line can be used to implement handshaking between the Master and the Slave. The Slave can extend the SCL low period by pulling the SCL line low. This is useful if the clock speed set up by the Master is too fast for the Slave, or the Slave needs extra time for processing between the data transmissions. The Slave extending the SCL low period will not affect the SCL high period, which is determined by the Master. As a consequence, the Slave can reduce the TWI data transfer speed by prolonging the SCL duty cycle.

Figure 18-6 shows a typical data transmission. Note that several data bytes can be transmitted between the SLA+R/W and the STOP condition, depending on the software protocol implemented by the application software.

Figure 18-6. Typical Data Transmission



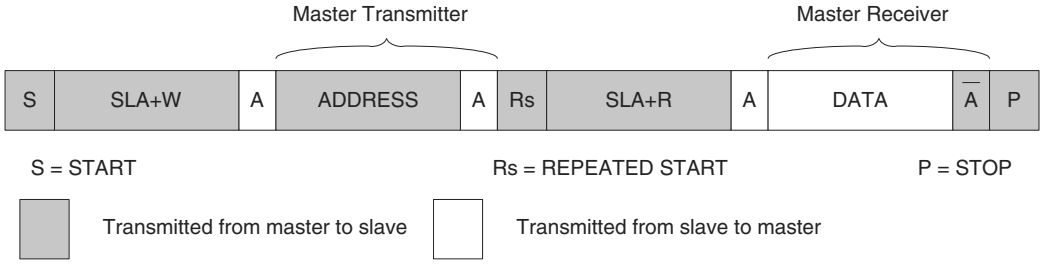
18.2 Multi-master Bus Systems, Arbitration and Synchronization

The TWI protocol allows bus systems with several masters. Special concerns have been taken in order to ensure that transmissions will proceed as normal, even if two or more masters initiate a transmission at the same time. Two problems arise in multi-master systems:

- An algorithm must be implemented allowing only one of the masters to complete the transmission. All other masters should cease transmission when they discover that they have lost the selection process. This selection process is called arbitration. When a contending master discovers that it has lost the arbitration process, it should immediately switch to Slave mode to check whether it is being addressed by the winning master. The fact that multiple masters have started transmission at the same time should not be detectable to the slaves (i.e., the data being transferred on the bus must not be corrupted).
- Different masters may use different SCL frequencies. A scheme must be devised to synchronize the serial clocks from all masters, in order to let the transmission proceed in a lockstep fashion. This will facilitate the arbitration process.

The wired-ANDing of the bus lines is used to solve both these problems. The serial clocks from all masters will be wired-ANDed, yielding a combined clock with a high period equal to the one from the master with the shortest high period. The low period of the combined clock is equal to the low period of the master with the longest low period. Note that all masters listen to the SCL line, effectively starting to count their SCL high and low Time-out periods when the combined SCL line goes high or low, respectively.

Figure 18-15. Combining Several TWI Modes to Access a Serial EEPROM

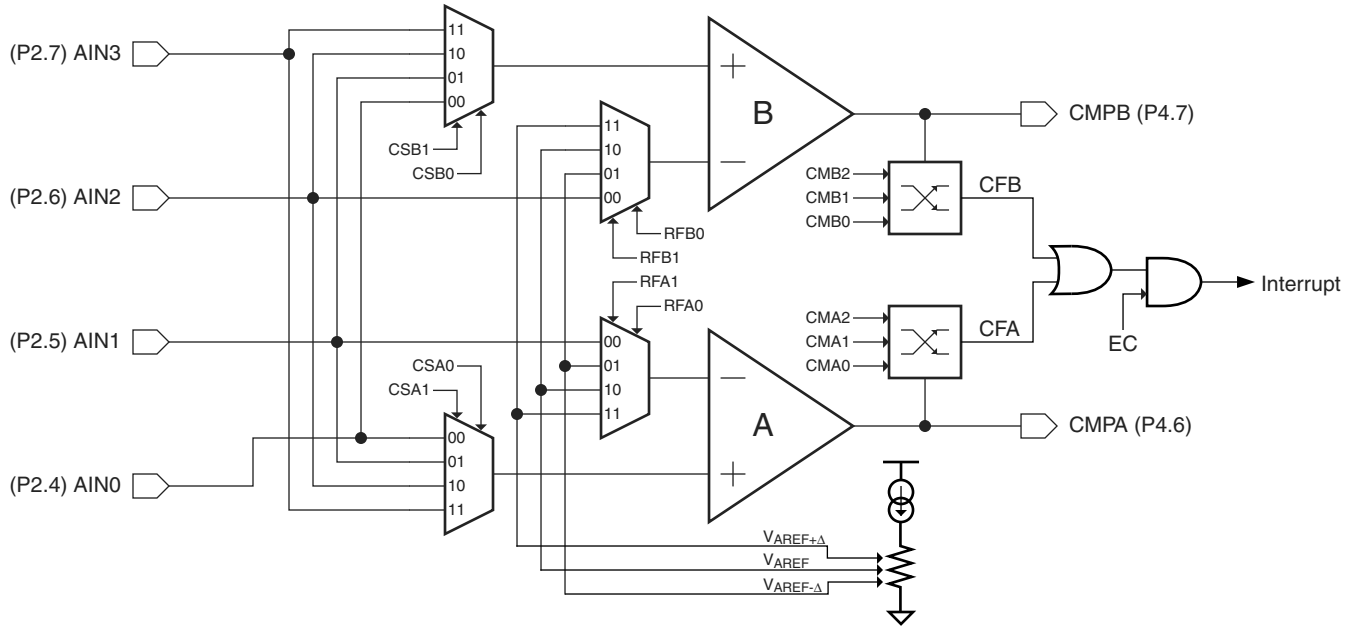


19. Dual Analog Comparators

The AT89LP3240/6440 provides two analog comparators. The analog comparators have the following features:

- Internal 3-level Voltage Reference (1.2V, 1.3V, 1.4V)
- Four Shared Analog Input Channels
  - Configure as Multiple Input Window Comparator
- Selectable Interrupt Conditions
  - High- or Low-level
  - Rising- or Falling-edge
  - Output Toggle
- Hardware Debouncing Modes

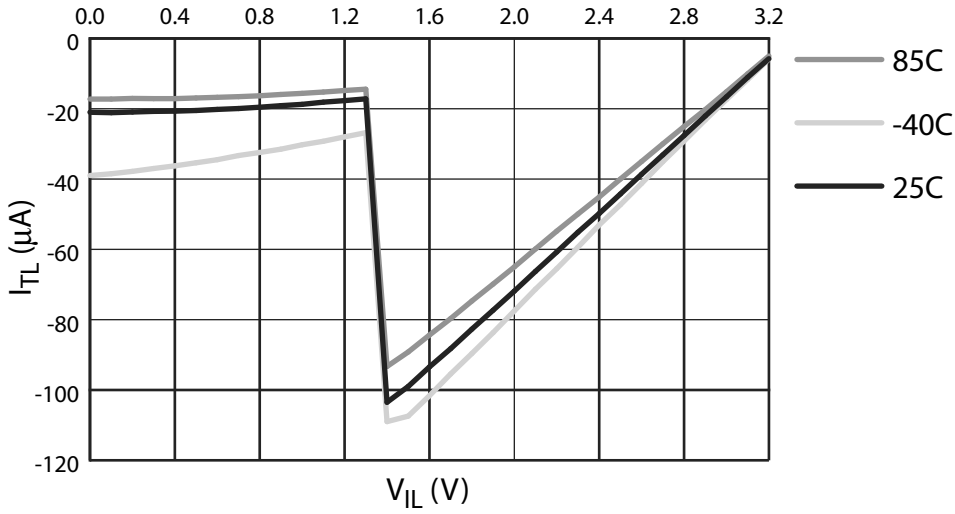
Figure 19-1. Dual Comparator Block Diagram



A block diagram of the dual analog comparators with relevant connections is shown in Figure 19-1. Input options allow the comparators to function in a number of different configurations as shown in Figure 19-4. Comparator operation is such that the output is a logic “1” when the positive input is greater than the negative input. Otherwise the output is a zero. Setting the CENA (ACSRA.3) and CENB (ACSRB.3) bits enable Comparator A and B respectively. The user must

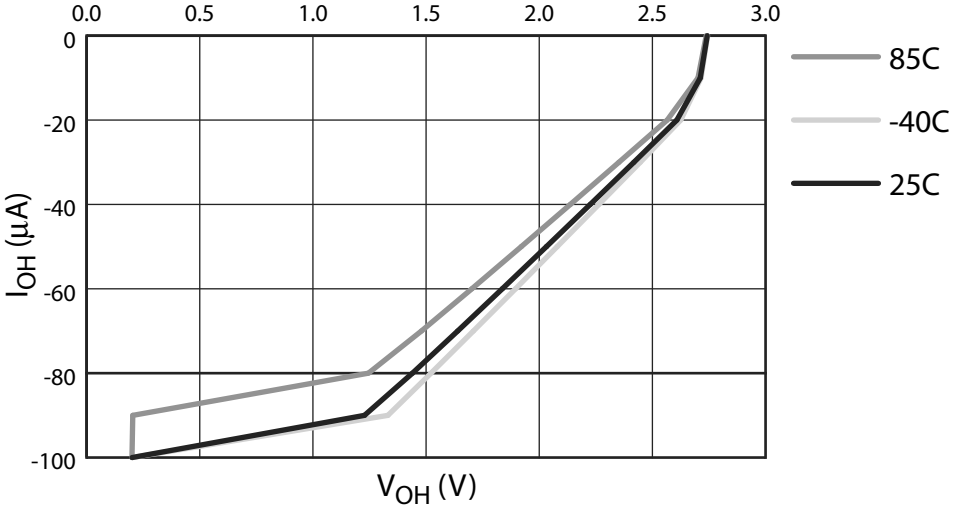
26.4.3 Quasi-Bidirectional Input

Figure 26-7. Quasi-bidirectional Input Transition Current at 3.3V



26.4.4 Quasi-Bidirectional Output

Figure 26-8. Quasi-Bidirectional Output I-V Source Characteristic at 3V



3. Parameter t_{LHLL} applies only when ALES = 1.
4. The strobe pulse width may be lengthened by 1, 2 or 3 additional t_{CLCL} using wait states.
5. Parameter t_{WHLH} applies only when ALES = 0, or when two MOVX instructions occur in succession.

Figure 26-15. External Data Memory Read Cycle

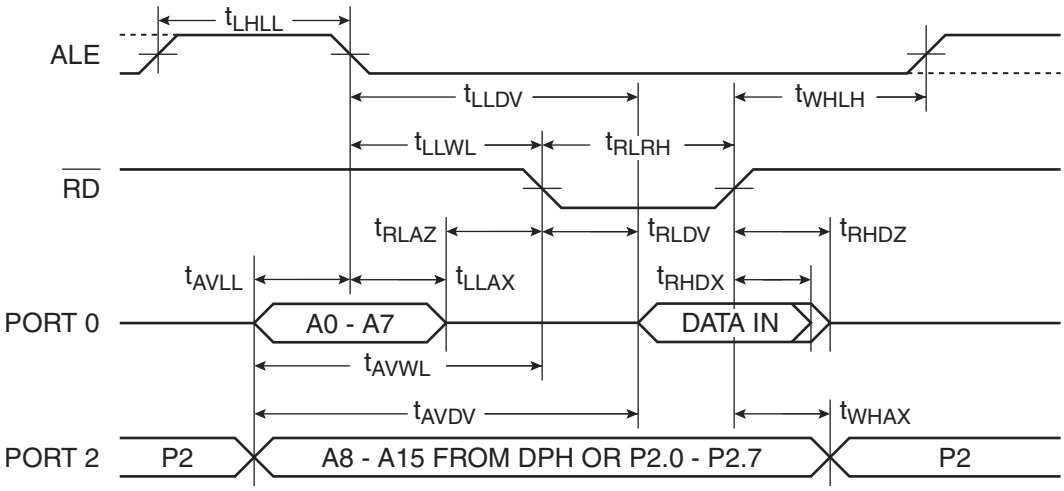
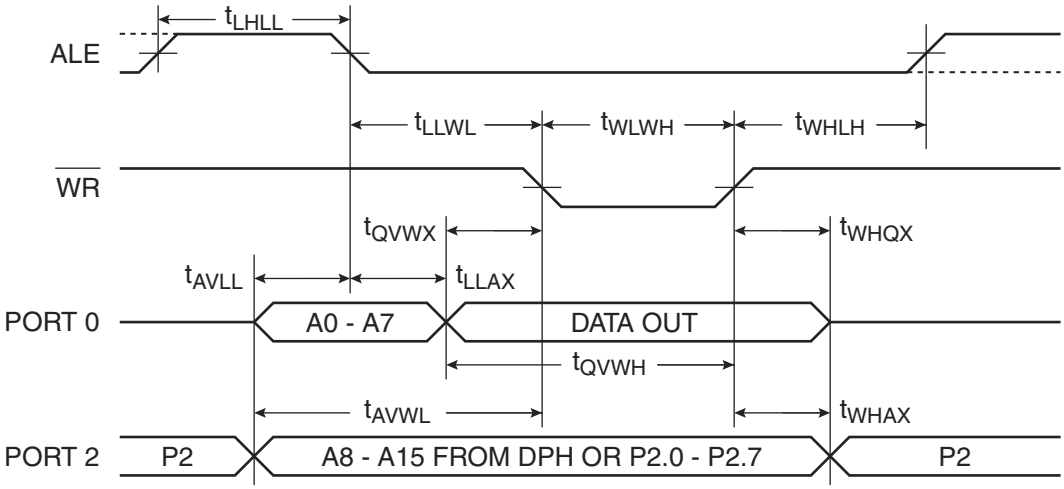


Figure 26-16. External Data Memory Write Cycle



26.8 Serial Peripheral Interface Timing

The values shown in these tables are valid for T_A = -40°C to 85°C and V_{DD} = 2.4 to 3.6V, unless otherwise noted.

Table 26-5. SPI **Master** Characteristics

Symbol	Parameter	Min	Max	Units
t_{CLCL}	Oscillator Period	41.6		ns
t_{SCK}	Serial Clock Cycle Time	$4t_{CLCL}$		ns
t_{SHSL}	Clock High Time	$t_{SCK}/2$ - 25		ns
t_{SLSH}	Clock Low Time	$t_{SCK}/2$ - 25		ns
t_{SR}	Rise Time		25	ns
t_{SF}	Fall Time		25	ns

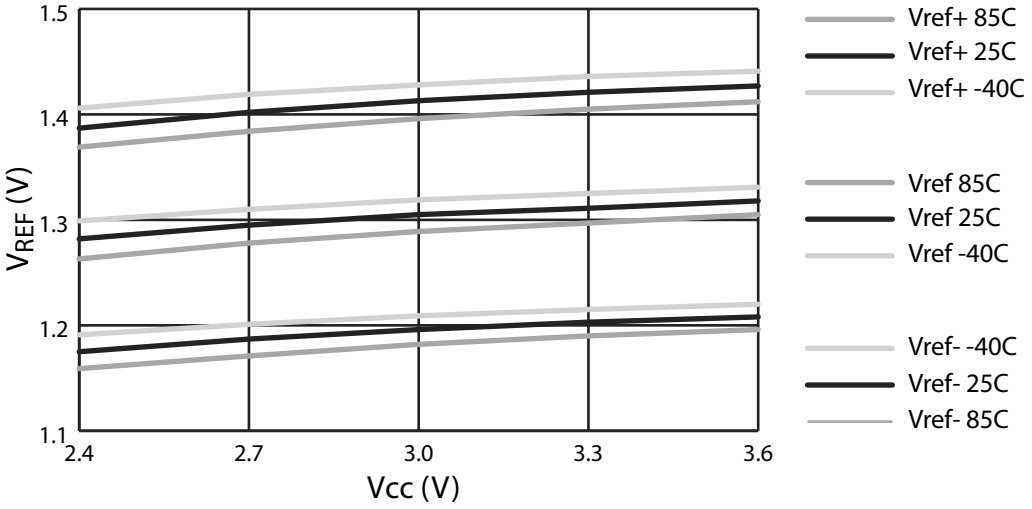
26.11 Dual Analog Comparator Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{DD} = 2.4 to 3.6V, unless otherwise noted.

Table 26-8. Dual Analog Comparator Characteristics

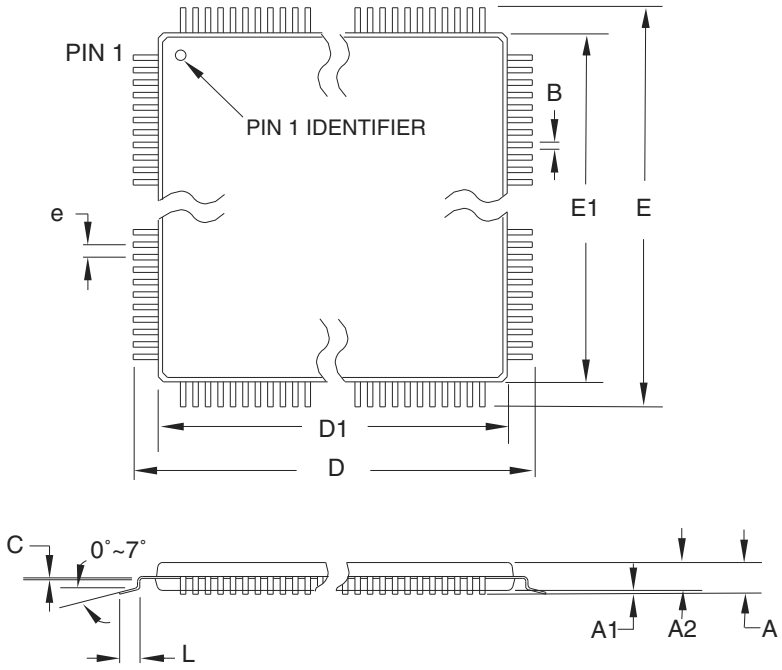
Symbol	Parameter	Condition	Min	Max	Units
V_{CM}	Common Mode Input Voltage		GND	V_{DD}	V
V_{OS}	Input Offset Voltage	V_{DD} = 3.6V		20	mV
V_{AREF}	Analog Reference Voltage		1.23	1.36	V
$V_{\Delta REF}$	Reference Delta Voltage		90	120	mV
t_{CMP}	Comparator Propagation Delay	$V_{IN+} - V_{IN-}$ = 20mV; V_{DD} = 2.4V		200	ns
t_{AREF}	Reference Settling Time		3		µs

Figure 26-23. Analog Reference Voltage Typical Characteristics



28. Packaging Information

28.1 44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

Table of Contents (Continued)

7.4 Watchdog Reset 36

7.5 Software Reset 36

8 Power Saving Modes 36

8.1 Idle Mode 36

8.2 Power-down Mode 37

8.3 Reducing Power Consumption 38

9 Interrupts 39

9.1 Interrupt Response Time 41

10 I/O Ports 45

10.1 Port Configuration 45

10.2 Port Analog Functions 48

10.3 Port Read-Modify-Write 48

10.4 Port Alternate Functions 49

11 Enhanced Timer 0 and Timer 1 with PWM 51

11.1 Mode 0 – Variable Width Timer/Counter 52

11.2 Mode 1 – 16-bit Auto-Reload Timer/Counter 52

11.3 Mode 2 – 8-bit Auto-Reload Timer/Counter 53

11.4 Mode 3 – 8-bit Split Timer 53

11.5 Pulse Width Modulation 56

12 Enhanced Timer 2 60

12.1 Timer 2 Registers 61

12.2 Capture Mode 62

12.3 Auto-Reload Mode 63

12.4 Baud Rate Generator 67

12.5 Frequency Generator (Programmable Clock Out) 68

13 Compare/Capture Array 69

13.1 CCA Registers 70

13.2 Input Capture Mode 72

13.3 Output Compare Mode 75

13.4 Pulse Width Modulation Mode 77

14 External Interrupts 82

15 General-purpose Interrupts 83

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: (+1) (408) 441-0311
Fax: (+1) (408) 487-2600
www.atmel.com
8051@atmel.com

Atmel Asia Limited
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
JAPAN
Tel: (+81) (3) 3523-3551
Fax: (+81) (3) 3523-7581