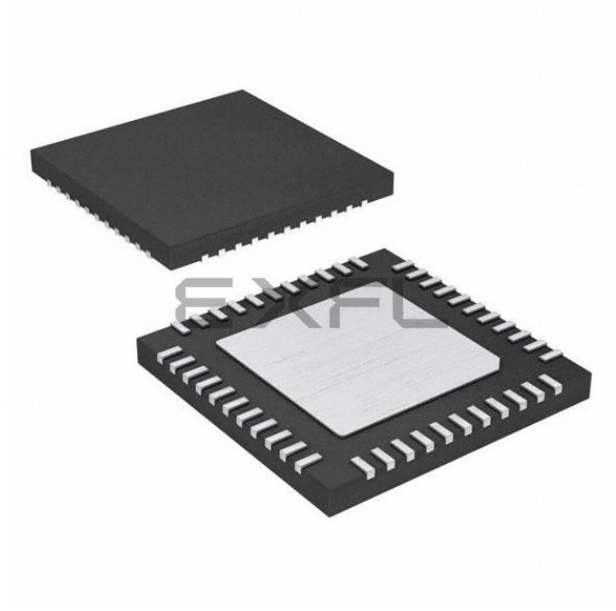

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp6440-20mu

There is no difference in counting rate between Timer 2's Auto-Reload/Capture and Baud Rate/Clock Out modes. All modes increment the timer once per clock cycle. Timer 2 in Auto-Reload/Capture mode increments at 12 times the rate of standard 8051s. Setting TPS_{3-0} = 1101B will force Timer 2 to count every twelve clocks. Timer 2 in Baud Rate or Clock Out mode increments at twice the rate of standard 8051s. Setting TPS_{3-0} = 0001B will force Timer 2 to count every two clocks.

2.3.6 Serial Port

The baud rate of the UART in Mode 0 defaults to 1/4 the clock frequency, compared to 1/12 the clock frequency in the standard 8051. In should also be noted that when using Timer 1 to generate the baud rate in UART Modes 1 or 3, the timer counts at the clock frequency and not at 1/12 the clock frequency. To maintain the same baud rate in the AT89LP3240/6440 while running at the same frequency as a standard 8051, the time-out period must be 12 times longer. Mode 1 of Timer 1 supports 16-bit auto-reload to facilitate longer time-out periods for generating low baud rates.

Timer 2 generated baud rates are twice as fast in the AT89LP3240/6440 than on standard 8051s when operating at the same frequency. The Timer Prescaler can also scale the baud rate to match an existing application.

2.3.7 SPI

The Serial Peripheral Interface (SPI) has a dedicated interrupt vector. The ESPI (IE2.2) bit replaces SPIE (SPCR.7). SPCR.7 (TSCK) now enables timer-generated baud rate.

The SPI includes Mode Fault detection. If multiple-master capabilities are not required, SSIG (SPSR.2) must be set to one for master mode to function correctly when $\overline{SS}$ (P1.4) is a general purpose I/O.

2.3.8 Watchdog Timer

The Watchdog Timer in AT89LP3240/6440 counts at a rate of once per clock cycle. This compares to once every 12 clocks in the standard 8051. A common prescaler is available to divide the time base for all timers and reduce the counting rate.

2.3.9 I/O Ports

The I/O ports of the AT89LP3240/6440 may be configured in four different modes. By default all the I/O ports revert to input-only (tristated) mode at power-up or reset. In the standard 8051, all ports are weakly pulled high during power-up or reset. To enable 8051-like ports, the ports must be put into quasi-bidirectional mode by clearing the P1M0, P2M0, P3M0 and P4M0 SFRs. The user can also configure the ports to start in quasi-bidirectional mode by disabling the Tristate-Port User Fuse. When this fuse is disabled, P1M0, P2M0, P3M0 and P4M0 will reset to 00h instead of FFh and the ports will be weakly pulled high. Port 0 and the upper nibble of Port 2 always power up tristated regardless of the fuse setting due to their analog functions.

2.3.10 External Memory Interface

The AT89LP3240/6440 does not support external program memory. The $\overline{PSEN}$ and $\overline{EA}$ functions are not supported and those pins are replaced with general purpose I/O. The ALE strobe does not toggle continuously and cannot be used as a board-level clock.

3. Memory Organization

The AT89LP3240/6440 uses a Harvard Architecture with separate address spaces for program and data memory. The program memory has a regular linear address space with support for 64K bytes of directly addressable application code. The data memory has 256 bytes of internal RAM and 128 bytes of Special Function Register I/O space. The AT89LP3240/6440 supports external data memory with portions of the external data memory space implemented on chip as Extra RAM and nonvolatile Flash data memory. External program memory is not supported. The memory address spaces of the AT89LP3240/6440 are listed in Table 3-1.

Table 3-1. AT89LP3240/6440 Memory Address Spaces

Name	Description	Range
DATA	Directly addressable internal RAM	00H–7FH
IDATA	Indirectly addressable internal RAM and stack space	00H–FFH
SFR	Directly addressable I/O register space	80H–FFH
EDATA	On-chip Extra RAM and extended stack space	0000H–0FFFH
FDATA	On-chip nonvolatile Flash data memory	1000H–2FFFH
XDATA	External data memory	3000H–FFFFH
CODE	On-chip nonvolatile Flash program memory (AT89LP3240)	0000H–7FFFH
	On-chip nonvolatile Flash program memory (AT89LP6440)	0000H–FFFFH
SIG	On-chip nonvolatile Flash signature array	0000H–01FFH

3.1 Program Memory

The AT89LP3240/6440 contains 32K/64K bytes of on-chip In-System Programmable Flash memory for program storage. The Flash memory has an endurance of at least 100,000 write/erase cycles and a minimum data retention time of 10 years. The reset and interrupt vectors are located within the first 83 bytes of program memory (refer to Table 9-1 on page 41). Constant tables can be allocated within the entire 32K/64K program memory address space for access by the MOVC instruction. The AT89LP3240/6440 does not support external program memory. A map of the AT89LP3240/6440 program memory is shown in Figure 3-1.

3.1.1 SIG

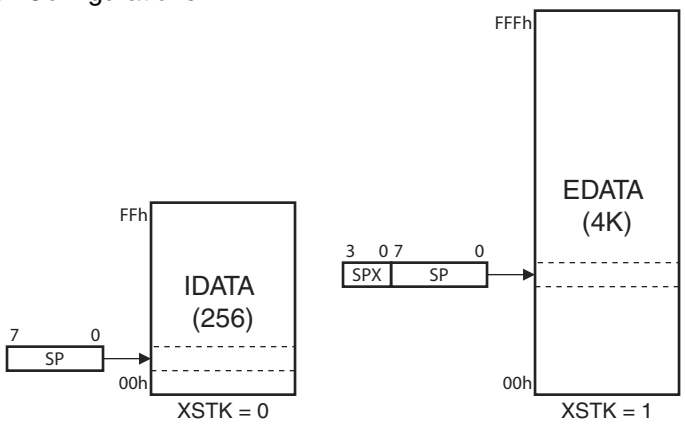
In addition to the 64K code space, the AT89LP3240/6440 also supports a 256-byte User Signature Array and a 128-byte Atmel Signature Array that are accessible by the CPU. The Atmel Signature Array is initialized with the Device ID in the factory. The second page of the User Signature Array (0180H–01FFH) is initialized with analog configuration data including the Internal RC Oscillator calibration byte. The User Signature Array is available for user identification codes or constant parameter data. Data stored in the signature array is not secure. Security bits will disable writes to the array; however, reads by an external device programmer are always allowed.

In order to read from the signature arrays, the SIGEN bit (DPCF.3) must be set (See Table 5-5 on page 28). While SIGEN is one, MOVC A,@A+DPTR will access the signature arrays. The User Signature Array is mapped from addresses 0100h to 01FFh and the Atmel Signature Array is mapped from addresses 0000h to 007Fh. SIGEN must be cleared before using MOVC to access the code memory. The User Signature Array may also be modified by the In-Application Programming interface. When IAP = 1 and SIGEN = 1, MOVX @DPTR instructions will access the array (See Section 3.5 on page 21).

tain separate copies of SP for use with each stack space. Interrupts should be disabled while swapping copies of SP in such an application to prevent illegal stack accesses.

All interrupt calls and PUSH, POP, ACALL, LCALL, RET and RETI instructions will incur a one or two-cycle penalty while the extended stack is enabled, depending on the number of stack access in each instruction. The extended stack may only exist within the internal EDATA space; it cannot be placed in XDATA. The stack will continue to use EDATA even if EDATA is disabled by setting EXRAM = 1.

Figure 3-14. Stack Configurations



3.5 In-Application Programming (IAP)

The AT89LP3240/6440 supports In-Application Programming (IAP), allowing the program memory to be modified during execution. IAP can be used to modify the user application on the fly or to use program memory for nonvolatile data storage. The same page structure write protocol for FDATA also applies to IAP (See Section 3.3.3.1 “Write Protocol” on page 14). The CPU is always placed in idle while modifying the program memory. When the write completes, the CPU will continue executing with the instruction after the MOVX @DPTR,A instruction that started the write.

To enable access to the program memory, the IAP bit (MEMCON.7) must be set to one and the IAP User Fuse must be enabled. The IAP User Fuse can disable all IAP operations. When this fuse is disabled, the IAP bit will be forced to 0. While IAP is enabled, all MOVX @DPTR instructions will access the CODE space instead of EDATA/FDATA/XDATA. IAP also allows reprogramming of the User Signature Array when SIGEN = 1. The IAP access settings are summarized in Table 3-5.

Table 3-5. IAP Access Settings

IAP	SIGEN	DMEN	MOVX @DPTR	MOVC @DPTR
0	0	0	EDATA (0000–0FFFH)	CODE (0000–FFFFH)
0	0	1	FDATA (1000–2FFFH)	CODE (0000–FFFFH)
0	1	0	EDATA (0000–0FFFH)	SIG (0000–01FFH)
0	1	1	FDATA (1000–2FFFH)	SIG (0000–01FFH)
1	0	X	CODE (0000–FFFFH)	CODE (0000–FFFFH)
1	1	X	SIG (0000–01FFH)	SIG (0000–01FFH)

pass through intermediate frequencies. When CDV is updated, the new frequency will take affect within a maximum period of 128 x t_{OSC}.

Table 6-2. CLKREG – Clock Control Register

CLKREG = 8FH — Reset Value = 0000 0000B

Not Bit Addressable

	TPS3	TPS2	TPS1	TPS0	CDV2	CDV1	CDV0	COE
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TPS[3-0]	Timer Prescaler. The Timer Prescaler selects the time base for Timer 0, Timer 1, Timer 2 and the Watchdog Timer. The prescaler is implemented as a 4-bit binary down counter. When the counter reaches zero it is reloaded with the value stored in the TPS bits to give a division ratio between 1 and 16. By default the timers will count every clock cycle (TPS = 0000B). To configure the timers to count at a standard 8051 rate of once every 12 clock cycles, TPS should be set to 1011B.
CDV[2-0]	System Clock Division. Determines the frequency of the system clock relative to the oscillator clock source. CDIV2 CDIV1 CDIV0 System Clock Frequency 0 0 0 $f_{OSC}/1$ 0 0 1 $f_{OSC}/2$ 0 1 0 $f_{OSC}/4$ 0 1 1 $f_{OSC}/8$ 1 0 0 $f_{OSC}/16$ 1 0 1 $f_{OSC}/32$ 1 1 0 $f_{OSC}/64$ 1 1 1 $f_{OSC}/128$
COE	Clock Out Enable. Set COE to output the system clock divided by 2 on XTAL2 (P4.1). The internal RC oscillator or external clock source must be selected in order to use this feature and P4.1 must be configured as an output.

7. Reset

During reset, all I/O Registers are set to their initial values, the port pins are tristated, and the program starts execution from the Reset Vector, 0000H. The AT89LP3240/6440 has five sources of reset: power-on reset, brown-out reset, external reset, watchdog reset, and software reset.

7.1 Power-on Reset

A Power-on Reset (POR) is generated by an on-chip detection circuit. The detection level V_{POR} is nominally 1.4V. The POR is activated whenever V_{DD} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. A power-on sequence is shown in Figure 7-1 on page 34. When V_{DD} reaches the Power-on Reset threshold voltage V_{POR}, an initialization sequence lasting t_{POR} is started. When the initialization sequence completes, the start-up timer determines how long the device is kept in POR after V_{DD} rise. The POR signal is activated again, without any delay, when V_{DD} falls below the POR threshold level. A Power-on Reset (i.e. a cold reset) will set the POF flag in PCON. The internally

Table 10-6. Port Pin Alternate Functions

Port Pin	Configuration Bits		Alternate Function	Notes
	PxM0.y	PxM1.y		
P1.2	P1M0.2	P1M1.2	SDA	open-drain
			GPI2	
P1.3	P1M0.3	P1M1.3	SCL	open-drain
			GPI3	
P1.4	P1M0.4	P1M1.4	$\overline{SS}$	
			GPI4	
P1.5	P1M0.5	P1M1.5	MOSI	
			GPI5	
P1.6	P1M0.6	P1M1.6	MISO	
			GPI6	
P1.7	P1M0.7	P1M1.7	SCK	
			GPI7	
P2.0	P2M0.0	P2M1.0	CCA	
P2.1	P2M0.1	P2M1.1	CCB	
P2.2	P2M0.2	P2M1.2	CCC	
			DA+	input-only
P2.3	P2M0.3	P2M1.3	CCD	
			DA-	input-only
P2.4	P2M0.4	P2M1.4	AIN0	input-only
P2.5	P2M0.5	P2M1.5	AIN1	input-only
P2.6	P2M0.6	P2M1.6	AIN2	input-only
P2.7	P2M0.7	P2M1.7	AIN3	input-only
P3.0	P3M0.0	P3M1.0	RXD	
P3.1	P3M0.1	P3M1.1	TXD	
P3.2	P3M0.2	P3M1.2	$\overline{INT0}$	
P3.3	P3M0.3	P3M1.3	$\overline{INT1}$	
P3.4	P3M0.4	P3M1.4	T0	
P3.5	P3M0.5	P3M1.5	T1	
P3.6	P3M0.6	P3M1.6	$\overline{WR}$	
P3.7	P3M0.7	P3M1.7	$\overline{RD}$	
P4.2	P3M0.5	P3M1.5	$\overline{RST}$	$\overline{RST}$ must be disabled to use P4.2
P4.6	not configurable		CMPA	Pin is tied to comparator output
P4.7	not configurable		CMPB	Pin is tied to comparator output

<table>
<tr><th>Symbol</th><th>Function</th></tr>
<tr><td>PHS [2-0]</td><td>CCA Phase Mode. PWM channels may be grouped by 2, 3 or 4 such that only one channel in a group produces a pulse in any one period. The PHS[2-0] bits may only be written when the timer is not active, i.e. TR2 = 0.
<u>PHS2</u> <u>PHS1</u> <u>PHS0</u> <u>Phase Mode</u>
0 0 0 Disabled, all channels active
0 0 1 2-phase output on channels A & B
0 1 0 3-phase output on channels A, B & C
0 1 1 4-phase output on channels A, B, C & D
1 0 0 Dual 2-phase output on channels A & B and C & D
1 0 1 reserved
1 1 0 reserved
1 1 1 reserved</td></tr>
<tr><td>T2CM [1-0]</td><td>Timer 2 Count Mode.
<u>T2CM1</u> <u>T2CM0</u> <u>Count Mode</u>
0 0 Standard Timer 2 (up count: BOTTOM →MAX)
0 1 Clear on RCAP compare (up count: MIN →TOP)
1 0 Dual-slope with single update (up-down count: MIN →TOP →MIN)
1 1 Dual-slope with double update (up-down count: MIN →TOP →MIN)</td></tr>
<tr><td>T2OE</td><td>Timer 2 Output Enable. When T2OE = 1 and C/$\overline{T}$2 = 0, the T2 pin will toggle after every Timer 2 overflow.</td></tr>
<tr><td>DCEN</td><td>Timer 2 Down Count Enable. When Timer 2 operates in Auto-Reload mode and EXEN2 = 1, setting DCEN = 1 will cause Timer 2 to count up or down depending on the state of T2EX.</td></tr>
</table>

12.2 Capture Mode

In the Capture mode, Timer 2 is a fixed 16-bit timer or counter that counts up from MIN to MAX. An overflow from MAX to MIN sets bit TF2 in T2CON. If EXEN2 = 1, a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 and TF2 bits can generate an interrupt. Capture mode is illustrated in Figure 12-1. The Timer 2 overflow rate in Capture mode is given by the following equation:

$$\text{Capture Mode:} \qquad \text{Time-out Period} = \frac{65536}{\text{Oscillator Frequency}} \times (\text{TPS} + 1)$$

RCAP2L and then overflows. The overflow sets TF2 and causes the timer registers to be reloaded with MIN. If EXEN2 = 1, a 1-to-0 transition on T2EX will clear the timer and set EXF2. The Timer 2 overflow rate for this mode is given in the following equation:

Auto-Reload Mode:
DCEN = 0, T2CM = 01B

$$\text{Time-out Period} = \frac{\{\text{RCAP2H}, \text{RCAP2L}\} + 1}{\text{Oscillator Frequency}} \times (\text{TPS} + 1)$$

Timer 2 Count Mode 1 is provided to support variable precision asymmetrical PWM in the CCA. The value of TOP stored in RCAP2H and RCAP2L is double-buffered such that a new TOP value takes affect only after an overflow. The behavior of Count Mode 0 versus Count Mode 1 is shown in Figure 12-3.

Figure 12-2. Timer 2 Diagram: Auto-Reload Mode (DCEN = 0)

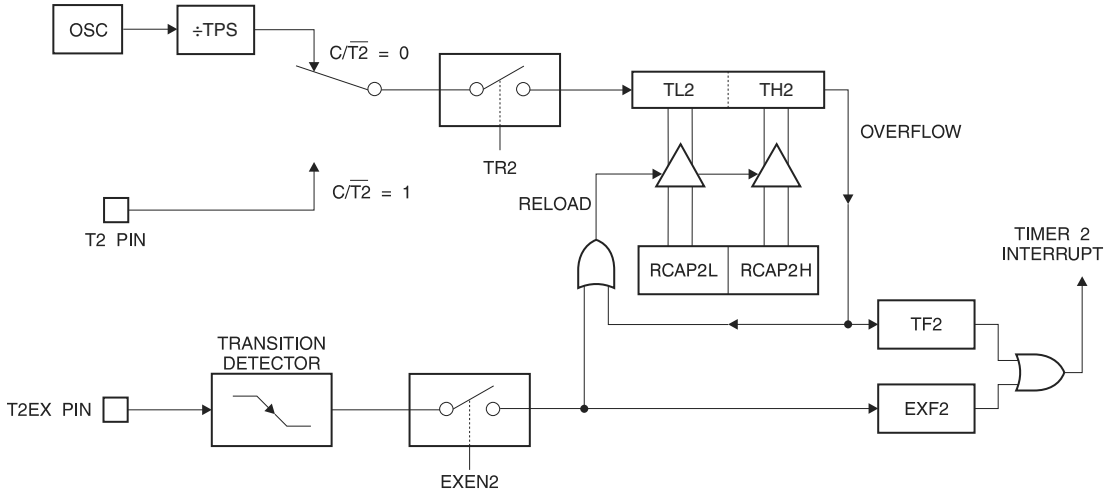
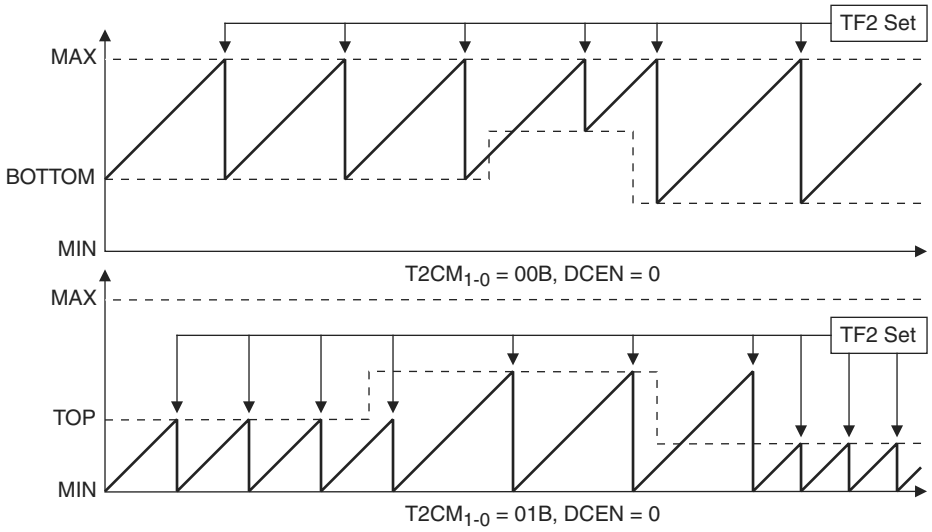


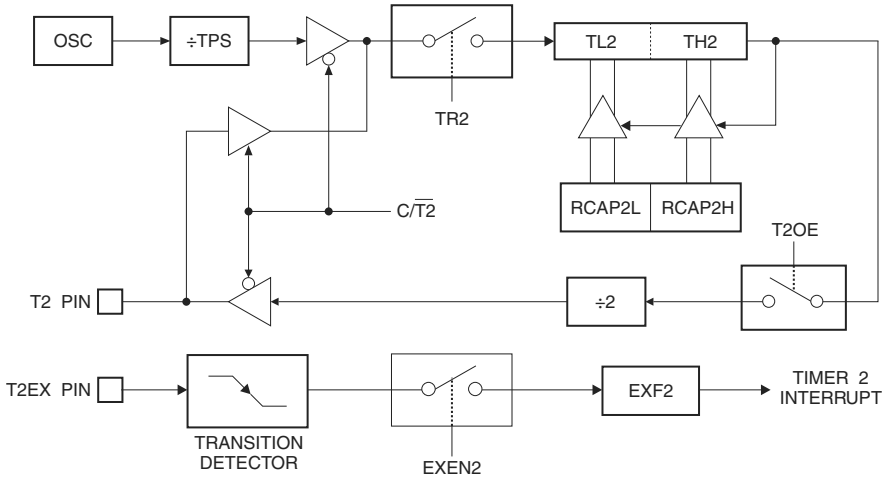
Figure 12-3. Timer 2 Waveform: Auto-Reload Mode (DCEN = 0)



12.3.2 Up or Down Counter

Setting DCEN = 1 enables Timer 2 to count up or down, as shown in Figure 12-4. In this mode, the T2EX pin controls the direction of the count (if EXEN2 = 1). A logic 1 at T2EX makes Timer 2 count up. When $T2CM_{1-0}$ = 00B, the timer will overflow at MAX and set the TF2 bit. This overflow also causes BOTTOM, the 16-bit value in RCAP2H and RCAP2L, to be reloaded into the timer

Figure 12-9. Timer 2 in Clock-out Mode



13. Compare/Capture Array

The AT89LP3240/6440 includes a four channel Compare/Capture Array (CCA) that performs a variety of timing operations including input event capture, output compare waveform generation and pulse width modulation (PWM). Timer 2 serves as the time base for the four 16-bit compare/capture modules. The CCA has the following features:

- Four 16-bit Compare/Capture channels
- Common time base provided by Timer 2
- Selectable external and internal capture events including pin change, timer overflow and comparator output change
- Symmetric/Asymmetric PWM with selectable polarity
- Multi-phasic PWM outputs
- One interrupt flag per channel with a common interrupt vector

The block diagram of the CCA is given in Figure 13-1. Each channel consists of an 8-bit control register and a 16-bit data register. The channel registers are not directly accessible. The CCA address register T2CCA provides an index into the array. The control, data low and data high bytes of the currently indexed channel are accessed through the T2CCC, T2CCL and T2CCH registers respectively.

Each channel can be individually configured for capture or compare mode. Capture mode is the default setting. During capture mode the current value of the time base is copied into the channel's data register when the specified external or internal event occurs. An interrupt flag is set at the same time and the time base may be optionally cleared. To enable compare mode, the CCM*x* bit in the channel's control register (CCC*x*) should be set to 1. In compare mode an interrupt flag is set and an output pin is optionally toggled when the value of the time base matches the value of the channel's data register. The time base may also be optionally cleared on a compare match.

Timer 2 must be running (TR2 = 1) in order to perform captures or compares with the CCA. However, when TR2 = 0 the external capture events will still set their associated flags and may be used as additional external interrupts.

Table 15-1. GPMOD – General-purpose Interrupt Mode Register

GPMOD = 9AH — Reset Value = 0000 0000B

Not Bit Addressable

	GPMOD7	GPMOD6	GPMOD5	GPMOD4	GPMOD3	GPMOD2	GPMOD1	GPMOD0
Bit	7	6	5	4	3	2	1	0

GPMOD.x 0 = level-sensitive interrupt for P1.x

1 = edge-triggered interrupt for P1.x

Table 15-2. GPLS – General-purpose Interrupt Level Select Register

GPLS = 9BH — Reset Value = 0000 0000B

Not Bit Addressable

	GPLS7	GPLS6	GPLS5	GPLS4	GPLS3	GPLS2	GPLS1	GPLS0
Bit	7	6	5	4	3	2	1	0

GPMOD.x 0 = detect low level or negative edge on P1.x

1 = detect high level or positive edge on P1.x

Table 15-3. GPIEN – General-purpose Interrupt Enable Register

GPIEN = 9CH — Reset Value = 0000 0000B

Not Bit Addressable

	GPIEN7	GPIEN6	GPIEN5	GPIEN4	GPIEN3	GPIEN2	GPIEN1	GPIEN0
Bit	7	6	5	4	3	2	1	0

GPIEN.x 0 = interrupt for P1.x disabled

1 = interrupt for P1.x enabled

Table 15-4. GPIF – General-purpose Interrupt Flag Register

GPIF = 9DH — Reset Value = 0000 0000B

Not Bit Addressable

	GPIF7	GPIF6	GPIF5	GPIF4	GPIF3	GPIF2	GPIF1	GPIF0
Bit	7	6	5	4	3	2	1	0

GPIF.x 0 = interrupt on P1.x inactive

1 = interrupt on P1.x active. Must be cleared by software.

16.4 More About Mode 1

Ten bits are transmitted (through TXD), or received (through RXD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the AT89LP3240/6440, the baud rate is determined either by the Timer 1 overflow rate, the TImer 2 overflow rate, or both. In this case one timer is for transmit and the other is for receive. Figure 16-4 shows a simplified functional diagram of the serial port in Mode 1 and associated timings for transmit and receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a “1” into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.

The transmission begins when $\overline{\text{SEND}}$ is activated, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, “0”s are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, the “1” that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain “0”s. This condition flags the TX Control unit to do one last shift, then deactivate $\overline{\text{SEND}}$ and set TI. This occurs at the tenth divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a 1-to-0 transition detected at RXD. For this purpose, RXD is sampled at a rate of 16 times the established baud rate. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its roll-overs with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done to reject noise. In order to reject false bits, if the value accepted during the first bit time is not 0, the receive circuits are reset and the unit continues looking for another 1-to-0 transition. If the start bit is valid, it is shifted into the input shift register, and reception of the rest of the frame proceeds.

As data bits come in from the right, “1”s shift out to the left. When the start bit arrives at the left-most position in the shift register, (which is a 9-bit register in Mode 1), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8 and to set RI is generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

RI = 0 and

Either SM2 = 0, or the received stop bit = 1

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether or not the above conditions are met, the unit continues looking for a 1-to-0 transition in RXD.

16.6 Framing Error Detection

In addition to all of its usual modes, the UART can perform framing error detection by looking for missing stop bits, and automatic address recognition. When used for framing error detect, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE, SCON.7 can only be cleared by software. The FE bit will be set by a framing error regardless of the state of SMOD0.

16.7 Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON for Modes 1, 2 or 3. In the 9-bit UART modes, Mode 2 and Mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9-bit mode requires that the 9th information bit be a “1” to indicate that the received information is an address and not data.

In Mode 1 (8-bit) the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8th address bits and the information is either a Given or Broadcast address.

Automatic Address Recognition is not available during Mode 0.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are “don’t care”. The SADEN mask can be logically ANDed with the SADDR to create the “Given” address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples show the versatility of this scheme:

Slave 0
SADDR = 1100 0000
SADEN = 1111 1101
Given = 1100 00X0

Slave 1
SADDR = 1100 0000
SADEN = 1111 1110
Given = 1100 000X

In the previous example, SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a “0” in bit 0 and it ignores bit 1. Slave 1 requires a “0” in bit 1 and bit 0 is ignored. A unique address for slave 0 would be 1100 0010 since slave 1 requires a “0” in bit 1. A unique address for slave 1 would be 1100 0001 since a “1” in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

Table 17-1. SPI Pin Configuration and Behavior when SPE = 1

Pin	Mode	Master (MSTR = 1)	Slave (MSTR = 0)
SCK	Quasi-bidirectional	Output	Input (Internal Pull-up)
	Push-Pull Output	Output	Input (Tristate)
	Input-Only	No output (Tristated)	Input (Tristate)
	Open-Drain Output	Output	Input (External Pull-up)
MOSI	Quasi-bidirectional	Output(1)	Input (Internal Pull-up)
	Push-Pull Output	Output(2)	Input (Tristate)
	Input-Only	No output (Tristated)	Input (Tristate)
	Open-Drain Output	Output(1)	Input (External Pull-up)
MISO	Quasi-bidirectional	Input (Internal Pull-up)	Output ($\overline{SS}$ = 0) Internal Pull-up ($\overline{SS}$ = 1 or DISSO = 1)
	Push-Pull Output	Input (Tristate)	Output ($\overline{SS}$ = 0) Tristated ($\overline{SS}$ = 1 or DISSO = 1)
	Input-Only	Input (Tristate)	No output (Tristated)
	Open-Drain Output	Input (External Pull-up)	Output ($\overline{SS}$ = 0) External Pull-up ($\overline{SS}$ = 1 or DISSO = 1)

Notes: 1. In these modes MOSI is active only during transfers. MOSI will be pulled high between transfers to allow other masters to control the line.

2. In Push-Pull mode MOSI is active only during transfers, otherwise it is tristated to prevent line contention. A weak external pull-up may be required to prevent MOSI from floating.

Table 17-2. SPCR – SPI Control Register

SPCR Address = E9H — Reset Value = 0000 0000B

Not Bit Addressable

	TSCK	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TSCK	SCK Clock Mode. When TSCK = 0, the SCK baud rate is based on the system clock, divided by the SPR_{1-0} ratio.When TSCK = 1, the SCK baud rate is based on the Timer 1 overflow rate, divided by the SPR_{1-0} ratio.
SPE	SPI enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/slave select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects slave SPI mode.
CPOL	Clock polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI clock phase and polarity control.
CPHA	Clock phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI clock phase and polarity control.

average TWI bus clock period. The SCL frequency is generated according to the following equation:

$$\text{SCL frequency} = \frac{\text{System Clock}}{16 \times (\text{TWBR} + 1)}$$

18.3.3 Bus Interface Unit

This unit contains the Data and Address Shift Register (TWDR), a START/STOP Controller and Arbitration detection hardware. The TWDR contains the address or data bytes to be transmitted, or the address or data bytes received. In addition to the 8-bit TWDR, the Bus Interface Unit also contains a register containing the (N)ACK bit to be transmitted or received. This (N)ACK Register is not directly accessible by the application software. However, when receiving, it can be set or cleared by manipulating the TWI Control Register (TWCR). When in Transmitter mode, the value of the received (N)ACK bit can be determined by the value in the TWSR. The START/STOP Controller is responsible for generation and detection of START, REPEATED START, and STOP conditions.

If the TWI has initiated a transmission as Master, the Arbitration Detection hardware continuously monitors the transmission trying to determine if arbitration is in process. If the TWI has lost an arbitration, the Control Unit is informed. Correct action can then be taken and appropriate status codes generated.

18.3.4 Address Match Unit

The Address Match unit checks if received address bytes match the 7-bit address in the TWI Address Register (TWAR). If the TWI General Call Recognition Enable (GC) bit in the TWAR is written to one, all incoming address bits will also be compared against the General Call address. Upon an address match, the Control unit is informed, allowing correct action to be taken. The TWI may or may not acknowledge its address, depending on settings in the TWCR.

18.3.5 Control Unit

The Control unit monitors the TWI bus and generates responses corresponding to settings in the TWI Control Register (TWCR). When an event requiring the attention of the application occurs on the TWI bus, the TWI Interrupt Flag (TWIF) is asserted. In the next clock cycle, the TWI Status Register (TWSR) is updated with a status code identifying the event. The TWSR only contains relevant status information when the TWI interrupt flag is asserted. At all other times, the TWSR contains a special status code indicating that no relevant status information is available. As long as the TWIF flag is set, the SCL line is held low. This allows the application software to complete its tasks before allowing the TWI transmission to continue.

The TWIF flag is set in the following situations:

- After the TWI has transmitted a START/REPEATED START condition.
- After the TWI has transmitted SLA+R/W.
- After the TWI has transmitted an address byte.
- After the TWI has lost arbitration.
- After the TWI has been addressed by own slave address or general call.
- After the TWI has received a data byte.
- After a STOP or REPEATED START has been received while still addressed as a Slave.
- When a bus error has occurred due to an illegal START or STOP condition.

22. Instruction Set Summary

The AT89LP3240/6440 is fully binary compatible with the 8051 instruction set. The difference between the AT89LP3240/6440 and the standard 8051 is the number of cycles required to execute an instruction. Instructions in the AT89LP3240/6440 may take 1 to 9 clock cycles to complete. The execution times of most instructions may be computed using Table 22-1.

Table 22-1. Instruction Execution Times and Exceptions

Generic Instruction Types	Cycle Count Formula
Most arithmetic, logical, bit and transfer instructions	# bytes
Branches and Calls	# bytes + 1
Single Byte Indirect (i.e. ADD A, @Ri, etc.)	2
RET, RETI	4/5[4]
MOVC	3
MOVX	2/4[2]
MUL	2
DIV	4
MAC	9
INC DPTR	2

		Clock Cycles		
Arithmetic	**Bytes**	**8051**	**AT89LP**	**Hex Code**
ADD A, Rn	1	12	1	28-2F
ADD A, direct	2	12	2	25
ADD A, @Ri	1	12	2	26-27
ADD A, #data	2	12	2	24
ADDC A, Rn	1	12	1	38-3F
ADDC A, direct	2	12	2	35
ADDC A, @Ri	1	12	2	36-37
ADDC A, #data	2	12	2	34
SUBB A, Rn	1	12	1	98-9F
SUBB A, direct	2	12	2	95
SUBB A, @Ri	1	12	2	96-97
SUBB A, #data	2	12	2	94
INC Rn	1	12	1	08-0F
INC direct	2	12	2	05
INC @Ri	1	12	2	06-07
INC A	2	12	2	04
DEC Rn	1	12	1	18-1F
DEC direct	2	12	2	15
DEC @Ri	1	12	2	16-17
DEC A	2	12	2	14
INC DPTR	1	24	2	A3

22.1 Instruction Set Extensions

The following instructions are extensions to the standard 8051 instruction set that provide enhanced capabilities not found in standard 8051 devices. All extended instructions start with an A5H escape code. For this reason random A5H reserved codes should not be placed in the instruction stream even though other devices may have treated these as NOPs.

Other AT89LP devices may not support all of these instructions.

22.1.1 ASR M

Function: Shift MAC Accumulator Right Arithmetically

Description: The forty bits in the M register are shifted one bit to the right. Bit 39 retains its value to preserve the sign of the value. No flags are affected.

Example: The M register holds the value 0C5B1A29384H . The following instruction,

```
ASR   M
```

leaves the M register holding the value 0E2D8D149C2H.

Bytes: 2

Cycles: 2

Encoding:

A5	0	0	0	0	0	0	1	1

Operation: ASR
$(M_n) \leftarrow (M_{n+1})$ n = 0 - 38
$(M_{39}) \leftarrow (M_{39})$

22.1.2 BREAK

Function: Software Breakpoint (Halt execution)

Description: BREAK transfers control from normal execution to the On-Chip Debug (OCD) handler if OCD is enabled. The PC is left pointing to the following instruction. If OCD is disabled, BREAK acts as a double NOP. No flags are affected.

Example: If On-Chip Debugging is allowed, the following instruction,

```
BREAK
```

will halt instruction execution prior to the immediately following instruction. If debugging is not allowed, the BREAK is treated as a double NOP.

Bytes: 2

Cycles: 2

Encoding:

A5	0	0	0	0	0	0	0	0

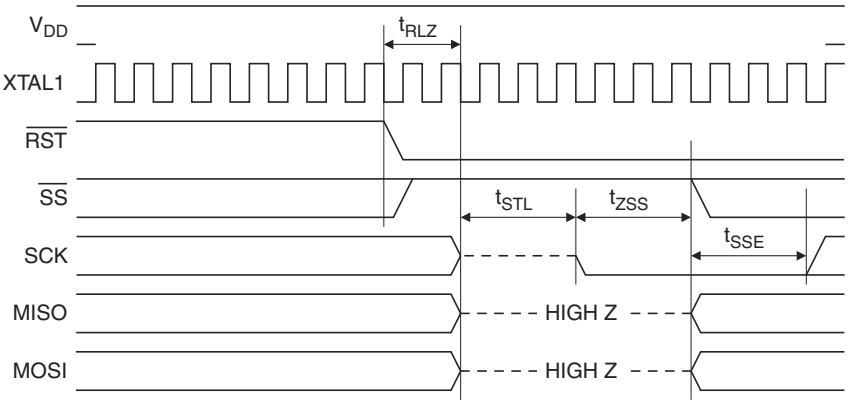
Operation: BREAK
(PC) ←(PC) + 2

23. Register Index

Table 23-1. Special Function Register Cross Reference

Name	Address	Description Index
ACC	E0H	
ACSRA	97H	Table 19-1 on page 130
ACSRB	9FH	Table 19-2 on page 131
AREF	AFH	Table 19-3 on page 132
AUXR	8EH	Table 3-4 on page 18
AX	E1H	Section 5.1 on page 24
B	F0H	
BX	F7H	Section 5.1 on page 24
CLKREG	8FH	Table 6-2 on page 33
DADC	D9H	Table 20-2 on page 139
DADH	DDH	Table 20-4 on page 139
DADI	DAH	Table 20-3 on page 139
DADL	DCH	Table 20-3 on page 139
DPCF (AUXR1)	A2H	Table 5-5 on page 28
DPH0	83H	Section 5.2 on page 25
DPH1	85H	Section 5.2 on page 25
DPL0	82H	Section 5.2 on page 25
DPL1	83H	Section 5.2 on page 25
DSPR	E2H	Table 5-1 on page 26
FIRD	E3H	Section 5.2.2.3 on page 29
GPIEN	9CH	Table 15-3 on page 84
GPIF	9DH	Table 15-4 on page 84
GPLS	9BH	Table 15-2 on page 84
GPMOD	9AH	Table 15-1 on page 84
IE	A8H	Table 9-2 on page 42
IE2	B4H	Table 9-3 on page 43
IP	B8H	Table 9-4 on page 43
IP2	B5H	Table 9-5 on page 43
IPH	B7H	Table 9-6 on page 44
IPH2	B6H	Table 9-7 on page 44
MACH	E5H	Section 5.1 on page 24
MACL	E4H	Section 5.1 on page 24
MEMCON	96H	Table 3-3 on page 17
P0	80H	Table 10-3 on page 45
P0M0	BAH	Table 10-2 and Table 10-3 on page 45
P0M1	BBH	Table 10-2 and Table 10-3 on page 45

Figure 25-9. In-System Programming (ISP) Start Sequence

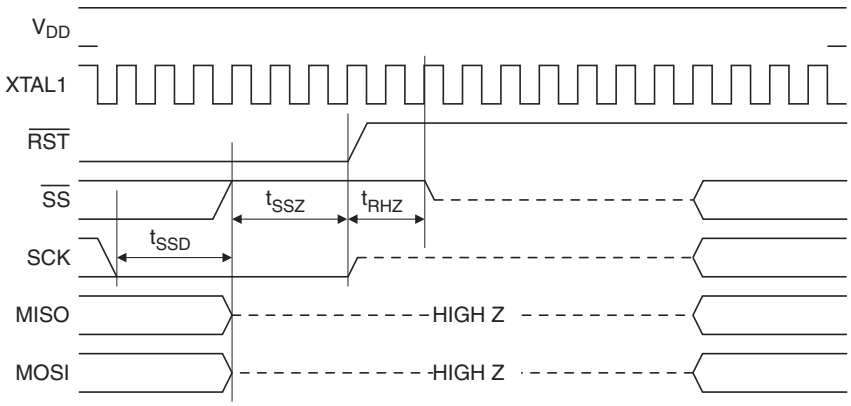


25.9.4 ISP Exit Sequence

Execute this sequence to exit ISP mode and resume CPU execution mode.

1. Drive SCK low.
1. Wait at least t_{SSD} and drive $\overline{SS}$ high.
2. Tristate MOSI.
3. Wait at least t_{SSZ} and bring $\overline{RST}$ high.
4. Tristate SCK.
5. Wait t_{RHZ} and tristate $\overline{SS}$.

Figure 25-10. In-System Programming (ISP) Exit Sequence



Note: The waveforms on this page are not to scale.

25.9.5 Serial Peripheral Interface

The Serial Peripheral Interface (SPI) is a byte-oriented full-duplex synchronous serial communication channel. During In-System Programming, the programmer always acts as the SPI master and the target device always acts as the SPI slave. The target device receives serial data on MOSI and outputs serial data on MISO. The Programming Interface implements a standard SPI Port with a fixed data order and For In-System Programming, bytes are transferred MSB first as shown in Figure 25-11. The SCK phase and polarity follow SPI clock mode 0 (CPOL = 0,

Figure 26-18. SPI Slave Timing (CPHA = 0)

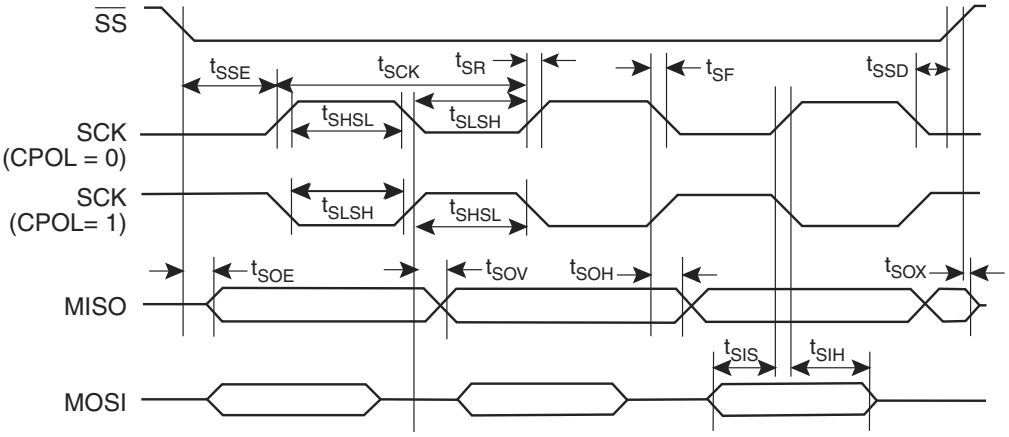


Figure 26-19. SPI Master Timing (CPHA = 1)

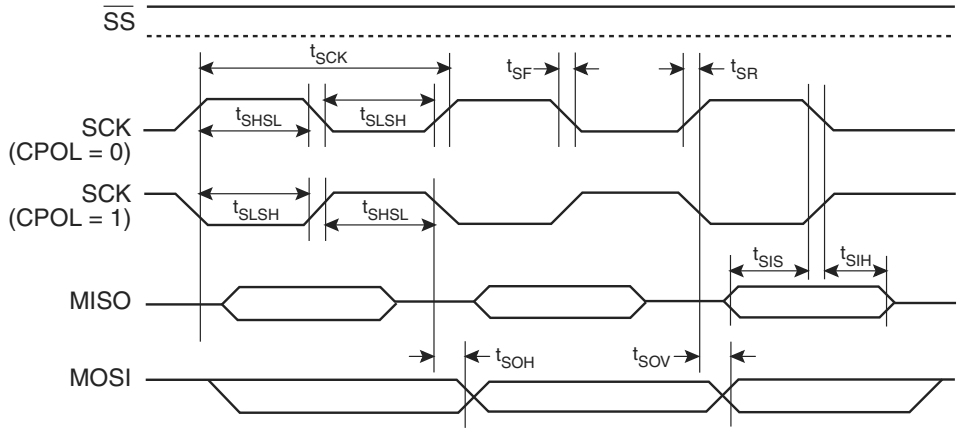
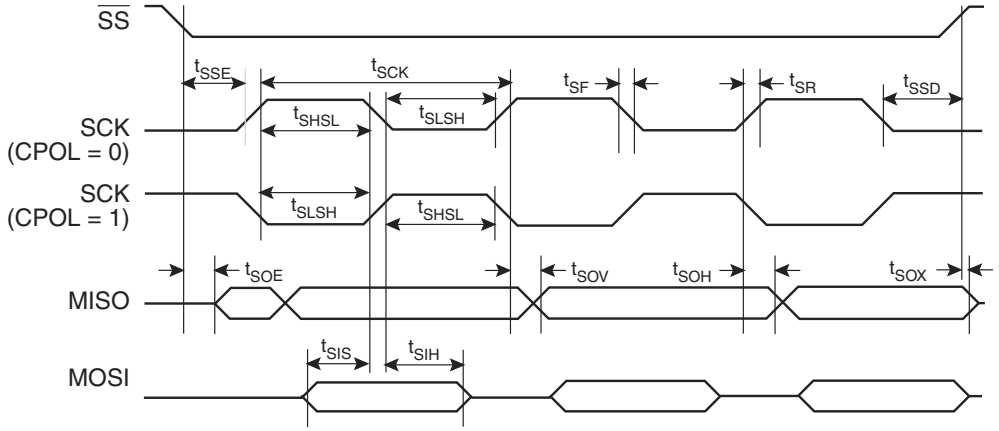


Figure 26-20. SPI Slave Timing (CPHA = 1)



27. Ordering Information

27.1 Green Package Option (Pb/Halide-free)

Code Flash	Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
32KB	20	2.4V to 3.6V	AT89LP3240-20AU	44A	Industrial (-40° C to 85° C)
			AT89LP3240-20PU	40P6	
			AT89LP3240-20JU	44J	
			AT89LP3240-20MU	44M1	
64KB	20	2.4V to 3.6V	AT89LP6440-20AU	44A	
			AT89LP6440-20PU	40P6	
			AT89LP6440-20JU	44J	
			AT89LP6440-20MU	44M1	

Package Types	
44A	44-lead, Thin Plastic Quad Flat Package (TQFP)
40P6	40-lead, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
44M1	44-pad, 7 x 7 x 1.0 mm Body, Plastic Very Thin Quad Flat No Lead Package (VQFN/MLF)

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