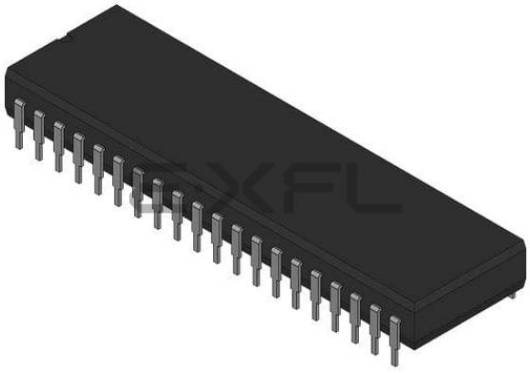
# Atmel - AT89LP6440-20PU Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 4.25K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.600", 15.24mm) |
| Supplier Device Package | 40-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/atmel/at89lp6440-20pu |

## 1.5 Pin Description

**Table 1-1.** AT89LP3240/6440 Pin Description

| Pin Number | | | | Symbol | Type | Description |
|---|---|---|---|---|---|---|
| TQFP | PLCC | PDIP | VQFN | | | |
| 1 | 7 | 6 | 1 | P1.5 | I/O<br>I/O<br><br>I | **P1.5**: User-configurable I/O Port 1 bit 5.<br>**MOSI**: SPI master-out/slave-in. When configured as master, this pin is an output. When configured as slave, this pin is an input.<br>**GPI5**: General-purpose Interrupt input 5. |
| 2 | 8 | 7 | 2 | P1.6 | I/O<br>I/O<br><br>I | **P1.6**: User-configurable I/O Port 1 bit 6.<br>**MISO**: SPI master-in/slave-out. When configured as master, this pin is an input. When configured as slave, this pin is an output.<br>**GPI6**: General-purpose Interrupt input 6. |
| 3 | 9 | 8 | 3 | P1.7 | I/O<br>I/O<br><br>I | **P1.7**: User-configurable I/O Port 1 bit 7.<br>**SCK**: SPI Clock. When configured as master, this pin is an output. When configured as slave, this pin is an input.<br>**GPI7**: General-purpose Interrupt input 7. |
| 4 | 10 | 9 | 4 | P4.2 | I/O<br>I<br><br>I | **P4.2**: User-configurable I/O Port 4 bit 2 (if Reset Fuse is disabled).<br>**$\overline{\text{RST}}$**: External **Active-Low** Reset input (if Reset Fuse is enabled. See “External Reset” on page 35.).<br>**DCL**: Serial Clock input for On-Chip Debug Interface when OCD is enabled. |
| 5 | 11 | 10 | 5 | P3.0 | I/O<br>I | **P3.0**: User-configurable I/O Port 3 bit 0.<br>**RXD**: Serial Port Receiver Input. |
| 6 | 12 | | 6 | VDD | I | Supply Voltage |
| 7 | 13 | 11 | 7 | P3.1 | I/O<br>O | **P3.1**: User-configurable I/O Port 3 bit 1.<br>**TXD**: Serial Port Transmitter Output. |
| 8 | 14 | 12 | 8 | P3.2 | I/O<br>I | **P3.2**: User-configurable I/O Port 3 bit 2.<br>**$\overline{\text{INT0}}$**: External Interrupt 0 Input or Timer 0 Gate Input. |
| 9 | 15 | 13 | 9 | P3.3 | I/O<br>I | **P3.3**: User-configurable I/O Port 3 bit 3.<br>**INT1**: External Interrupt 1 Input or Timer 1 Gate Input |
| 10 | 16 | 14 | 10 | P3.4 | I/O<br>I/O | **P3.4**: User-configurable I/O Port 3 bit 4.<br>**T1**: Timer/Counter 0 External input or PWM output. |
| 11 | 17 | 15 | 11 | P3.5 | I/O<br>I/O | **P3.5**: User-configurable I/O Port 3 bit 5.<br>**T1**: Timer/Counter 1 External input or PWM output. |
| 12 | 18 | 16 | 12 | P3.6 | I/O<br>O | **P3.6**: User-configurable I/O Port 3 bit 6.<br>**$\overline{\text{WR}}$**: External memory interface Write Strobe (active-low). |
| 13 | 19 | 17 | 13 | P3.7 | I/O<br>O | **P3.7**: User-configurable I/O Port 3 bit 7.<br>**$\overline{\text{RD}}$**: External memory interface Read Strobe (active-low). |
| 14 | 20 | 18 | 14 | P4.1 | I/O<br>O<br><br>O<br><br>I/O | **P4.1**: User-configurable I/O Port 4 bit 1.<br>**XTAL2**: Output from inverting oscillator amplifier. It may be used as a port pin if the internal RC oscillator is selected as the clock source.<br>**CLKOUT**: When the internal RC oscillator is selected as the clock source, may be used to output the internal clock divided by 2.<br>**DDA**: Serial Data input/output for On-Chip Debug Interface when OCD is enabled and the external clock is selected as the clock source. |
| 15 | 21 | 19 | 15 | P4.0 | I/O<br>I<br><br>I/O | **P4.0**: User-configurable I/O Port 4 bit 0.<br>**XTAL1**: Input to the inverting oscillator amplifier and internal clock generation circuits. It may be used as a port pin if the internal RC oscillator is selected as the clock source.<br>**DDA**: Serial Data input/output for On-Chip Debug Interface when OCD is enabled and the internal RC oscillator is selected as the clock source. |
| 16 | 22 | N/A | 16 | GND | I | Ground |

## 2.3 Comparison to Standard 8051

The AT89LP3240/6440 is part of a family of devices with enhanced features that are fully binary compatible with the 8051 instruction set. In addition, most SFR addresses, bit assignments, and pin alternate functions are identical to Atmel's existing standard 8051 products. However, due to the high performance nature of the device, some system behaviors are different from those of Atmel's standard 8051 products such as AT89S52 or AT89C2051. The major differences from the standard 8051 are outlined in the following paragraphs and may be useful to users migrating to the AT89LP3240/6440 from older devices.

### 2.3.1 System Clock

The maximum CPU clock frequency equals the externally supplied XTAL1 frequency. The oscillator is not divided by 2 to provide the internal clock and X2 mode is not supported. The System Clock Divider can scale the CPU clock versus the oscillator source (See Section 6.5 on page 32).

### 2.3.2 Reset

The $\overline{\text{RST}}$ pin of the AT89LP3240/6440 is **active-LOW** as compared with the active-high reset in the standard 8051. In addition, the $\overline{\text{RST}}$ pin is sampled every clock cycle and must be held low for a minimum of two clock cycles, instead of 24 clock cycles, to be recognized as a valid reset.

### 2.3.3 Instruction Execution with Single-cycle Fetch

The CPU fetches one code byte from memory every clock cycle instead of every six clock cycles. This greatly increases the throughput of the CPU. As a consequence, the CPU no longer executes instructions in 12, 24 or 48 clock cycles. Each standard instruction executes in only 1 to 4 clock cycles. See “Instruction Set Summary” on page 143 for more details. Any software delay loops or instruction-based timing operations may need to be retuned to achieve the desired results.

### 2.3.4 Interrupt Handling

The interrupt controller polls the interrupt flags during the last clock cycle of any instruction. In order for an interrupt to be serviced at the end of an instruction, its flag needs to have been latched as active during the next to last clock cycle of the instruction, or in the last clock cycle of the previous instruction if the current instruction executes in only a single clock cycle.

The external interrupt pins, $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$, are sampled at every clock cycle instead of once every 12 clock cycles. Coupled with the shorter instruction timing and faster interrupt response, this leads to a higher maximum rate of incidence for the external interrupts.

The Serial Peripheral Interface (SPI) has a dedicated interrupt vector. The SPI no longer shares its interrupt with the Serial Port and the ESPI (IE2.2) bit replaces SPIE (SPCR.7).

### 2.3.5 Timer/Counters

By default Timer0, Timer 1 and Timer 2 are incremented at a rate of once per clock cycle. This compares to once every 12 clocks in the standard 8051. A common prescaler is available to divide the time base for all timers and reduce the increment rate. The $TPS_{3-0}$ bits in the CLKREG SFR control the prescaler (Table 6-2 on page 33). Setting $TPS_{3-0}$ = 1011B will cause the timers to count once every 12 clocks.

The external Timer/Counter pins, T0, T1, T2 and T2EX, are sampled at every clock cycle instead of once every 12 clock cycles. This increases the maximum rate at which the Counter modules may function.

There is no difference in counting rate between Timer 2's Auto-Reload/Capture and Baud Rate/Clock Out modes. All modes increment the timer once per clock cycle. Timer 2 in Auto-Reload/Capture mode increments at 12 times the rate of standard 8051s. Setting $TPS_{3-0}$ = 1101B will force Timer 2 to count every twelve clocks. Timer 2 in Baud Rate or Clock Out mode increments at twice the rate of standard 8051s. Setting $TPS_{3-0}$ = 0001B will force Timer 2 to count every two clocks.

### 2.3.6 Serial Port

The baud rate of the UART in Mode 0 defaults to 1/4 the clock frequency, compared to 1/12 the clock frequency in the standard 8051. In should also be noted that when using Timer 1 to generate the baud rate in UART Modes 1 or 3, the timer counts at the clock frequency and not at 1/12 the clock frequency. To maintain the same baud rate in the AT89LP3240/6440 while running at the same frequency as a standard 8051, the time-out period must be 12 times longer. Mode 1 of Timer 1 supports 16-bit auto-reload to facilitate longer time-out periods for generating low baud rates.

Timer 2 generated baud rates are twice as fast in the AT89LP3240/6440 than on standard 8051s when operating at the same frequency. The Timer Prescaler can also scale the baud rate to match an existing application.

### 2.3.7 SPI

The Serial Peripheral Interface (SPI) has a dedicated interrupt vector. The ESPI (IE2.2) bit replaces SPIE (SPCR.7). SPCR.7 (TSCK) now enables timer-generated baud rate.

The SPI includes Mode Fault detection. If multiple-master capabilities are not required, SSIG (SPSR.2) must be set to one for master mode to function correctly when $\overline{SS}$ (P1.4) is a general purpose I/O.

### 2.3.8 Watchdog Timer

The Watchdog Timer in AT89LP3240/6440 counts at a rate of once per clock cycle. This compares to once every 12 clocks in the standard 8051. A common prescaler is available to divide the time base for all timers and reduce the counting rate.

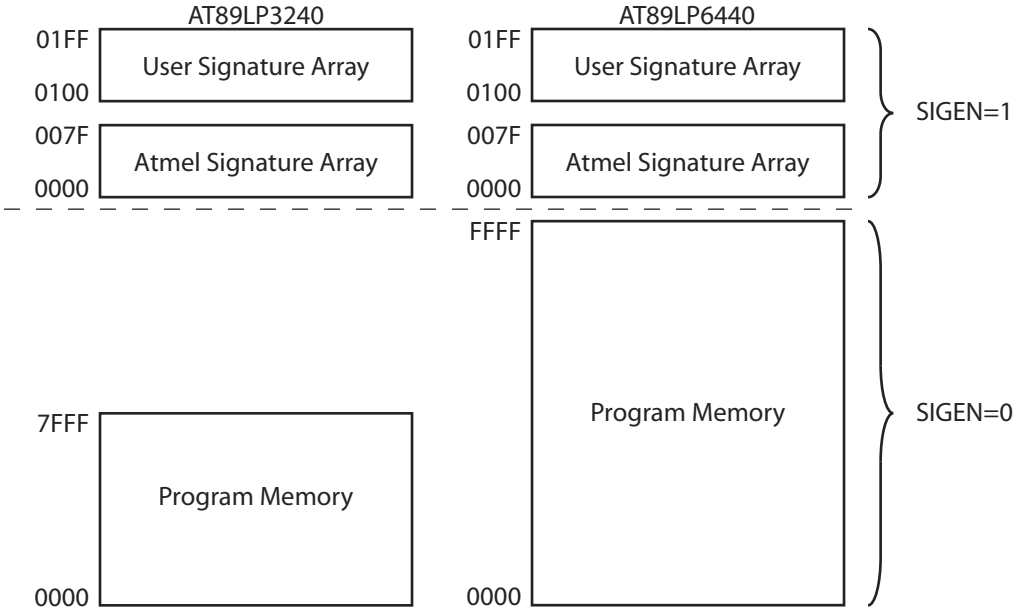
### 2.3.9 I/O Ports

The I/O ports of the AT89LP3240/6440 may be configured in four different modes. By default all the I/O ports revert to input-only (tristated) mode at power-up or reset. In the standard 8051, all ports are weakly pulled high during power-up or reset. To enable 8051-like ports, the ports must be put into quasi-bidirectional mode by clearing the P1M0, P2M0, P3M0 and P4M0 SFRs. The user can also configure the ports to start in quasi-bidirectional mode by disabling the Tristate-Port User Fuse. When this fuse is disabled, P1M0, P2M0, P3M0 and P4M0 will reset to 00h instead of FFh and the ports will be weakly pulled high. Port 0 and the upper nibble of Port 2 always power up tristated regardless of the fuse setting due to their analog functions.

### 2.3.10 External Memory Interface

The AT89LP3240/6440 does not support external program memory. The $\overline{PSEN}$ and $\overline{EA}$ functions are not supported and those pins are replaced with general purpose I/O. The ALE strobe does not toggle continuously and cannot be used as a board-level clock.

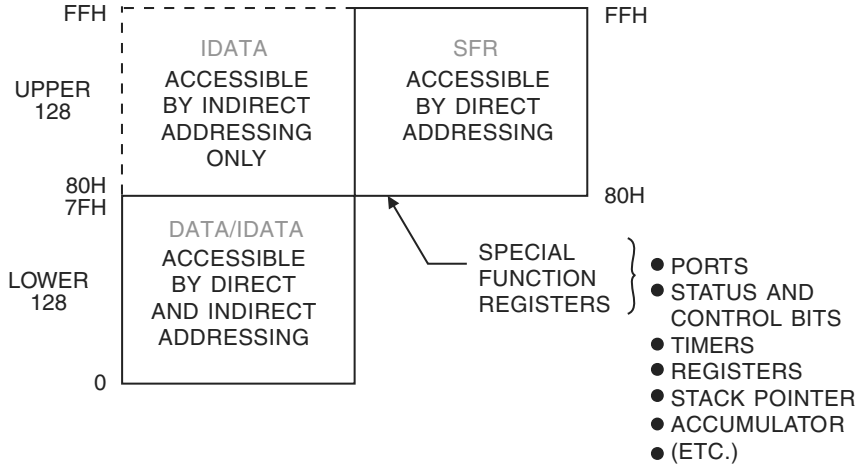
**Figure 3-1.** Program Memory Map




## 3.2 Internal Data Memory

The AT89LP3240/6440 contains 256 bytes of general SRAM data memory plus 128 bytes of I/O memory mapped into a single 8-bit address space. Access to the internal data memory does not require any configuration. The internal data memory has three address spaces: DATA, IDATA and SFR; as shown in Figure 3-2. Some portions of external data memory are also implemented internally. See “External Data Memory” below for more information.

**Figure 3-2.** Internal Data Memory Map




### 3.2.1 DATA

The first 128 bytes of RAM are directly addressable by an 8-bit address (00H–7FH) included in the instruction. The lowest 32 bytes of DATA memory are grouped into 4 banks of 8 registers each. The RS0 and RS1 bits (PSW.3 and PSW.4) select which register bank is in use. Instructions using register addressing will only access the currently specified bank. The lower 128 bit addresses are also mapped into DATA addresses 20H—2FH.

meet the minimum system requirements before the device exits reset and starts normal operation. The $\overline{RST}$ pin may be held low externally until these conditions are met.

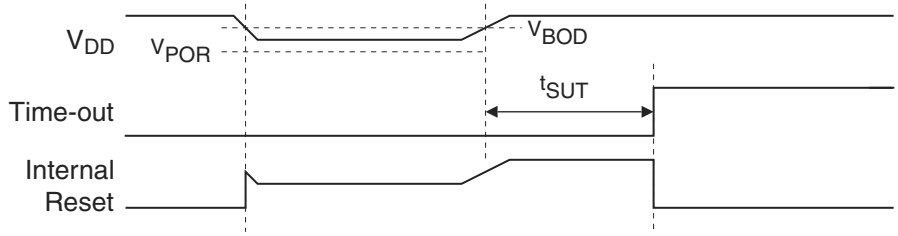
**Table 7-1.** Start-up Timer Settings

| SUT Fuse 1 | SUT Fuse 0 | Clock Source | $t_{SUT}$ (± 5%) µs |
|---|---|---|---|
| 0 | 0 | Internal RC/External Clock | 16 |
| | | Crystal Oscillator | 1024 |
| 0 | 1 | Internal RC/External Clock | 512 |
| | | Crystal Oscillator | 2048 |
| 1 | 0 | Internal RC/External Clock | 1024 |
| | | Crystal Oscillator | 4096 |
| 1 | 1 | Internal RC/External Clock | 4096 |
| | | Crystal Oscillator | 16384 |

## 7.2 Brown-out Reset

The AT89LP3240/6440 has an on-chip Brown-out Detection (BOD) circuit for monitoring the $V_{DD}$ level during operation by comparing it to a fixed trigger level. The trigger level $V_{BOD}$ for the BOD is nominally 2.0V. The purpose of the BOD is to ensure that if $V_{DD}$ fails or dips while executing at speed, the system will gracefully enter reset without the possibility of errors induced by incorrect execution. A BOD sequence is shown in Figure 7-3. When $V_{DD}$ decreases to a value below the trigger level $V_{BOD}$, the internal reset is immediately activated. When $V_{DD}$ increases above the trigger level plus about 200 mV of hysteresis, the start-up timer releases the internal reset after the specified time-out period has expired (Table 7-1). The Brown-out Detector must be enabled by setting the BOD Enable Fuse. (See “User Configuration Fuses” on page 164.)

**Figure 7-3.** Brown-out Detector Reset




The AT89LP3240/6440 allows for a wide $V_{DD}$ operating range. The on-chip BOD may not be sufficient to prevent incorrect execution if $V_{BOD}$ is lower than the minimum required $V_{DD}$ range, such as when a 3.6V supply is coupled with high frequency operation. In such cases an external Brown-out Reset circuit connected to the $\overline{RST}$ pin may be required.

## 7.3 External Reset

The P4.2/$\overline{RST}$ pin can function as either an active-**LOW** reset input or as a digital general-purpose I/O, P4.2. The Reset Pin Enable Fuse, when set to “1”, enables the external reset input function on P4.2. (See “User Configuration Fuses” on page 164.) When cleared, P4.2 may be used as an input or output pin. When configured as a reset input, the pin must be held low for at least two clock cycles to trigger the internal reset. The $\overline{RST}$ pin includes an on-chip pull-up resistor tied to $V_{DD}$. The pull-up is disabled when the pin is configured as P4.2.

**Table 9-3.** IE2 – Interrupt Enable 2 Register

IE = B4H — Reset Value = xxxx x000B

Not Bit Addressable

| | – | – | – | ETWI | EADC | ESPI | ECC | EGP |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| ETWI | Two-Wire Interface Interrupt Enable |
| EADC | ADC Interrupt Enable |
| ESPI | Serial Peripheral Interface Interrupt Enable |
| ECC | Compare/Capture Array Interrupt Enable |
| EGP | General-purpose Interrupt Enable |

**Table 9-4.** IP – Interrupt Priority Register

IP = B8H — Reset Value = 0000 0000B

Bit Addressable

| | IP0D | PC | PT2 | PS | PT1 | PX1 | PT0 | PX0 |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| IP0D | Interrupt Priority 0 Disable. Set IP0D to 1 to disable all interrupts with priority level zero. Clear to 0 to enable all interrupts with priority level zero when EA = 1. |
| PC | Comparator Interrupt Priority Low |
| PT2 | Timer 2 Interrupt Priority Low |
| PS | Serial Port Interrupt Priority Low |
| PT1 | Timer 1 Interrupt Priority Low |
| PX1 | External Interrupt 1 Priority Low |
| PT0 | Timer 0 Interrupt Priority Low |
| PX0 | External Interrupt 0 Priority Low |

**Table 9-5.** IP2 – Interrupt Priority 2 Register

IP = B5H — Reset Value = 0xxx x000B

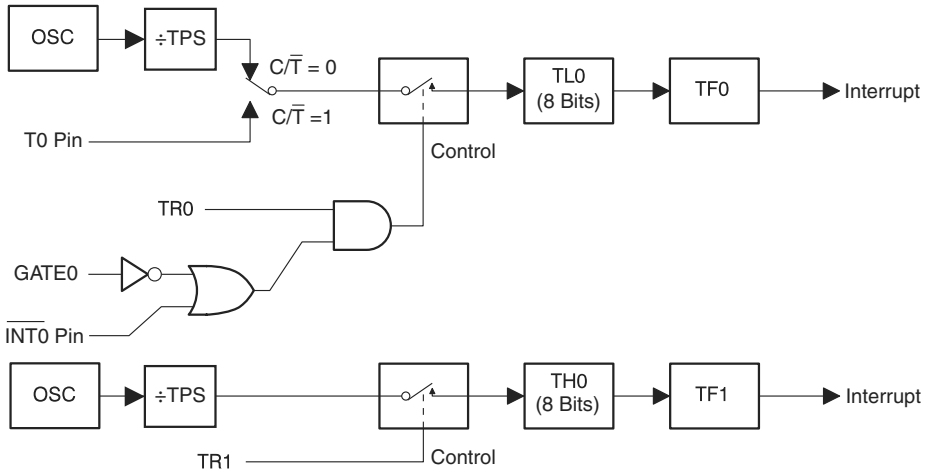
No Bit Addressable

| | IP2D | – | – | PTWI | PADC | PSP | PCC | PGP |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| IP2D | Interrupt Priority 2 Disable. Set IP2D to 1 to disable all interrupts with priority level two. Clear to 0 to enable all interrupts with priority level two when EA = 1. |
| PTWI | Two-wire Interface Interrupt Priority Low |
| PADC | ADC Interrupt Priority Low |

Mode 3 is for applications requiring an extra 8-bit timer or counter. With Timer 0 in Mode 3, the AT89LP3240/6440 can appear to have four Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3. In this case, Timer 1 can still be used by the serial port as a baud rate generator or in any application not requiring an interrupt.

**Figure 11-4.** Timer/Counter 0 Mode 3: Two 8-bit Counters




Note: RH0/RL0 are not required by Timer 0 during Mode 3 and may be used as temporary storage registers.

**Table 11-2.** TCON – Timer/Counter Control Register

TCON = 88H — Reset Value = 0000 0000B

Bit Addressable

| | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| TF1 | Timer 1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to interrupt routine. |
| TR1 | Timer 1 run control bit. Set/cleared by software to turn Timer/Counter on/off. |
| TF0 | Timer 0 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to interrupt routine. |
| TR0 | Timer 0 run control bit. Set/cleared by software to turn Timer/Counter on/off. |
| IE1 | Interrupt 1 edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed. |
| IT1 | Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts. |
| IE0 | Interrupt 0 edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed. |
| IT0 | Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts. |

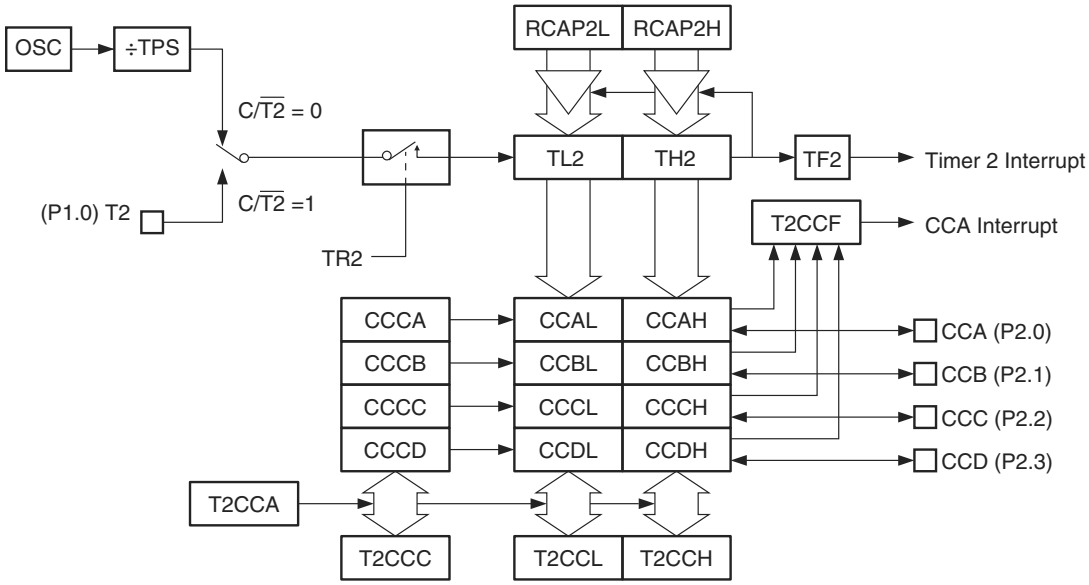
<table>
<tr><th>Symbol</th><th>Function</th></tr>
<tr><td>PHS [2-0]</td><td>CCA Phase Mode. PWM channels may be grouped by 2, 3 or 4 such that only one channel in a group produces a pulse in any one period. The PHS[2-0] bits may only be written when the timer is not active, i.e. TR2 = 0.<br><u>PHS2</u> <u>PHS1</u> <u>PHS0</u> <u>Phase Mode</u><br>0 0 0 Disabled, all channels active<br>0 0 1 2-phase output on channels A & B<br>0 1 0 3-phase output on channels A, B & C<br>0 1 1 4-phase output on channels A, B, C & D<br>1 0 0 Dual 2-phase output on channels A & B and C & D<br>1 0 1 reserved<br>1 1 0 reserved<br>1 1 1 reserved</td></tr>
<tr><td>T2CM [1-0]</td><td>Timer 2 Count Mode.<br><u>T2CM1</u> <u>T2CM0</u> <u>Count Mode</u><br>0 0 Standard Timer 2 (up count: BOTTOM →MAX )<br>0 1 Clear on RCAP compare (up count: MIN →TOP )<br>1 0 Dual-slope with single update (up-down count: MIN →TOP →MIN )<br>1 1 Dual-slope with double update (up-down count: MIN →TOP →MIN )</td></tr>
<tr><td>T2OE</td><td>Timer 2 Output Enable. When T2OE = 1 and C/$\overline{T}$2 = 0, the T2 pin will toggle after every Timer 2 overflow.</td></tr>
<tr><td>DCEN</td><td>Timer 2 Down Count Enable. When Timer 2 operates in Auto-Reload mode and EXEN2 = 1, setting DCEN = 1 will cause Timer 2 to count up or down depending on the state of T2EX.</td></tr>
</table>

## 12.2 Capture Mode

In the Capture mode, Timer 2 is a fixed 16-bit timer or counter that counts up from MIN to MAX. An overflow from MAX to MIN sets bit TF2 in T2CON. If EXEN2 = 1, a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 and TF2 bits can generate an interrupt. Capture mode is illustrated in Figure 12-1. The Timer 2 overflow rate in Capture mode is given by the following equation:

$$\text{Capture Mode:} \qquad \text{Time-out Period} = \frac{65536}{\text{Oscillator Frequency}} \times (\text{TPS} + 1)$$

**Figure 13-1.** Compare/Capture Array Block Diagram




## 13.1 CCA Registers

The Compare/Capture Array has five Special Function Registers: T2CCA, T2CCC, T2CCL, T2CCH and T2CCF. The T2CCF register contains the interrupt flags for each CCA channel. The CCA interrupt is a logic OR of the bits in T2CCF. The flags are set by hardware when a compare/capture event occurs on the relevant channel and must be cleared by software. The T2CCF bits will only generate an interrupt when the ECC bit (IE2.1) is set and the CIEN*x* bit in the associated channel's CCC*x* register is set.

The T2CCC, T2CCL and T2CCH register locations are not true SFRs. These locations represent access points to the contents of the array. Writes/reads to/from the T2CCC, T2CCL and T2CCH locations will access the control, data low and data high bytes of the CCA channel currently selected by the index in T2CCA. Channels currently not indexed by T2CCA are not accessible.

When writing to T2CCH, the value is stored in a shadow register. When T2CCL is written, the 16-bit value formed by the contents of T2CCL and the T2CCH shadow is written into the array. Therefore, T2CCH must be written prior to writing T2CCL. All four channels use the same T2CCH shadow register. If the value of T2CCH remains constant for multiple writes, there is no need to update T2CCH between T2CCL writes. Every write to T2CCL will use the last value of T2CCH for the upper data byte. It is not possible to write to the data register of a channel configured for capture mode.

The configuration bits for each channel are stored in the CCC*x* registers accessible through T2CCC. See Table 13-5 on page 74 for a description of the CCC*x* register.

**Table 13-1.** T2CCA – Timer/Counter 2 Compare/Capture Address

T2CCA Address = 0D1H — Reset Value = xxxx xx00B

Not Bit Addressable

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | T2CCA.1 | T2CCA.0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function | | |
|---|---|---|---|
| T2CCA [1-0] | Compare/Capture Address. Selects which CCA channel is currently accessible through the T2CCH, T2CCL and T2CCC registers. Only one channel may be accessed at a time. | | |
| | **T2CCA1** | **T2CCA0** | **Channel** |
| | 0 | 0 | A – T2CCH, T2CCL and T2CCC access data and control for Channel A |
| | 0 | 1 | B – T2CCH, T2CCL and T2CCC access data and control for Channel B |
| | 1 | 0 | C – T2CCH, T2CCL and T2CCC access data and control for Channel C |
| | 1 | 1 | D – T2CCH, T2CCL and T2CCC access data and control for Channel D |

**Table 13-2.** T2CCH – Timer/Counter 2 Compare/Capture Data High

T2CCH Address = 0D2H — Reset Value = 0000 0000B

Not Bit Addressable

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | T2CCD.15 | T2CCD.14 | T2CCD.13 | T2CCD.12 | T2CCD.11 | T2CCD.10 | T2CCD.9 | T2CCD.8 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| T2CCD [15-8] | Compare/Capture Data (High Byte). Reads from T2CCH will return the high byte from the CCA channel currently selected by T2CCA. The high byte of the selected CCA channel will be updated with the contents of T2CCH when T2CCL is written. When writing multiple channels with the same high byte, T2CCH need not be updated between writes to T2CCL. |

Note: All writes/reads to/from T2CCH will access channel *X* as currently selected by T2CCA.The data registers for the remaining unselected channels are not accessible.

**Table 13-3.** T2CCL – Timer/Counter 2 Compare/Capture Data Low

T2CCC Address = 0D3H — Reset Value = 0000 0000B

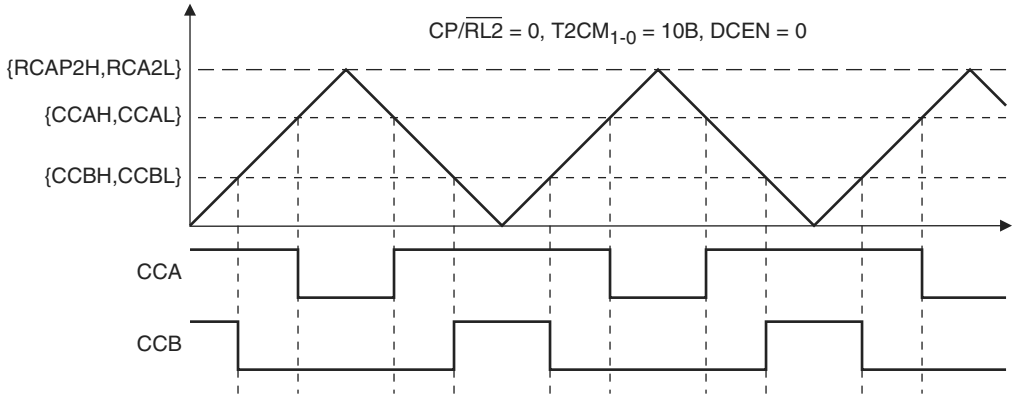
Not Bit Addressable

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | T2CCD.7 | T2CCD.6 | T2CCD.5 | T2CCD.4 | T2CCD.3 | T2CCD.2 | T2CCD.1 | T2CCD.0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| T2CCD [7-0] | Compare/Capture Data (Low Byte). Reads from T2CCL will return the low byte from the CCA channel currently selected by T2CCA. Writes to T2CCL will update the selected CCA channel with the 16-bit contents of T2CCH and T2CCL. |

Note: All writes/reads to/from T2CCL will access channel *X* as currently selected by T2CCA.The data registers for the remaining unselected channels are not accessible.

**Figure 13-6.** Dual-Slope Waveform Example




### 13.3.2 Timer 2 Operation for Compare Mode

Compare channels will work with any Timer 2 operating mode. The full 16-bit compare range may not be available in all modes. In order for a compare output action to take place, the compare values must be within the counting range of Timer 2. CTC*x* must be cleared to 0 for all channels if Timer 2 is operating in Baud Rate mode or errors may occur in the serial communication.

## 13.4 Pulse Width Modulation Mode

In Pulse Width Modulation (PWM) Mode, a compare channel can output a square wave with programmable frequency and duty cycle. Setting CCMx = 1 and $CxM_{2-0}$ = 10xB enables PWM Mode. PWM Mode is similar to Output Compare Mode except that the compare value is double-buffered. A diagram of a CCA channel in PWM Mode is shown in Figure 13-7. The PWM polarity is selectable between inverting and non-inverting modes. PWM is intended for use with Timer 2 in Auto-Reload Mode (CP/$\overline{RL2}$ = 0, DCEN = 0) using count modes 1, 2 or 3. The PWM can operate in asymmetric (edge-aligned) or symmetric (center-aligned) mode depending on the T2CM selection. The CCA PWM has variable precision from 2 to 16 bits. A trade-off between frequency and precision is made by changing the TOP value of the timer. The CCA PWM always uses the greatest precision allowable for the selected output frequency, as compared to Timer 0 and 1 whose PWMs are fixed at 8-bit precision regardless of frequency.

**Figure 13-7.** CCA PWM Mode Diagram

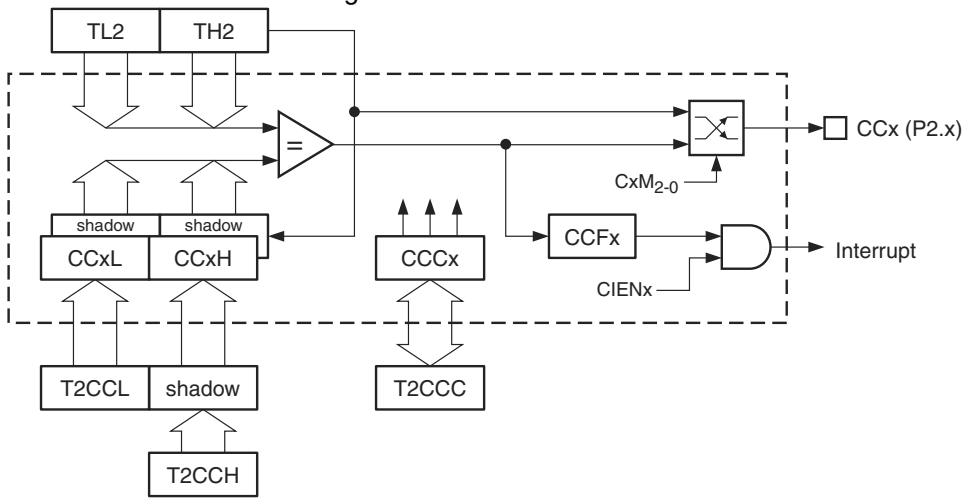


**Figure 16-5.** Serial Port Mode 2

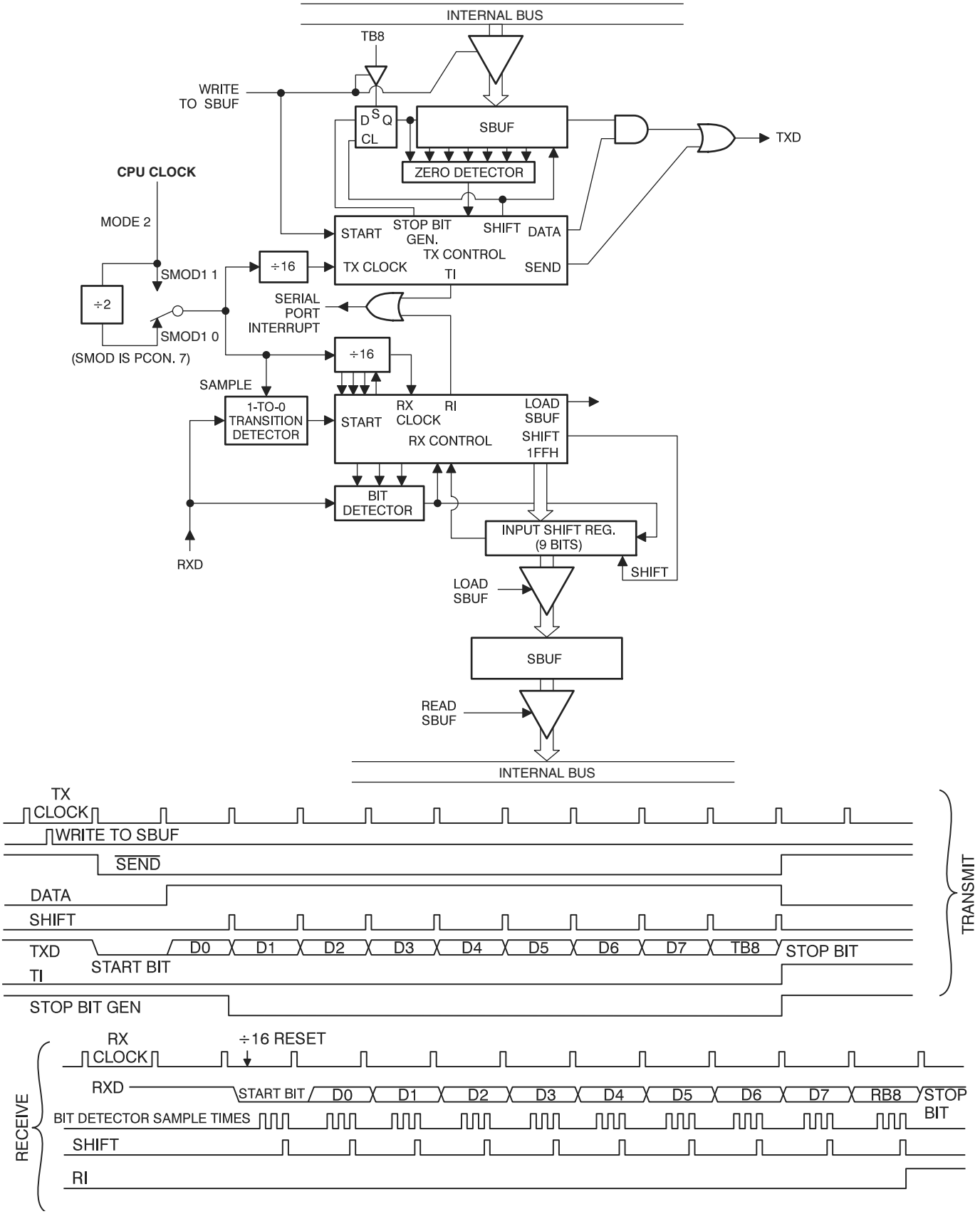
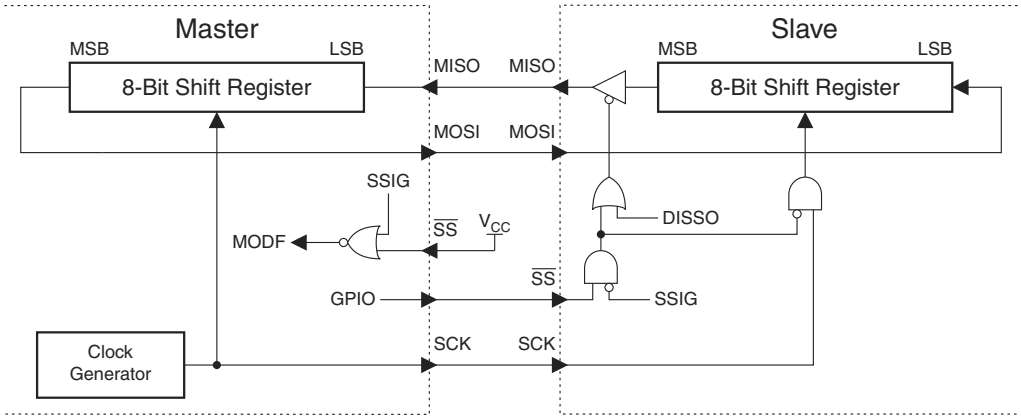


**Figure 17-2.** SPI Master-Slave Interconnection




When the SPI is configured as a Master (MSTR in SPCR is set), the operation of the $\overline{SS}$ pin depends on the setting of the Slave Select Ignore bit, SSIG. If SSIG = 1, the $\overline{SS}$ pin is a general purpose output pin which does not affect the SPI system. Typically, the pin will be driving the $\overline{SS}$ pin of an SPI Slave. If SSIG = 0, $\overline{SS}$ must be held high to ensure Master SPI operation. If the $\overline{SS}$ pin is driven low by peripheral circuitry when the SPI is configured as a Master with SSIG = 0, the SPI system interprets this as another master selecting the SPI as a slave and starting to send data to it. To avoid bus contention, the SPI system takes the following actions:

1. The MSTR bit in SPCR is cleared and the SPI system becomes a Slave. As a result of the SPI becoming a Slave, the MOSI and SCK pins become inputs.
2. The MODF Flag in SPSR is set, and if the SPI interrupt is enabled, the interrupt routine will be executed.

Thus, when interrupt-driven SPI transmission is used in Master mode, and there exists a possibility that $\overline{SS}$ may be driven low, the interrupt should always check that the MSTR bit is still set. If the MSTR bit has been cleared by a slave select, it must be set by the user to re-enable SPI Master mode.

## 17.1 Master Operation

An SPI master device initiates all data transfers on the SPI bus. The AT89LP3240/6440 is configured for master operation by setting MSTR = 1 in SPCR. Writing to the SPI data register (SPDR) while in master mode loads the transmit buffer. If the SPI shift register is empty, the byte in the transmit buffer is moved to the shift register; the transmit buffer empty flag, TXE, is set; and a transmission begins. The transfer may start after an initial delay, while the clock generator waits for the next full bit slot of the specified baud rate. The master shifts the data out serially on the MOSI line while providing the serial shift clock on SCK. When the transfer finishes, the SPIF flag is set to “1” and an interrupt request is generated, if enabled. The data received from the addressed SPI slave device is also transferred from the shift register to the receive buffer. Therefore, the SPIF bit flags both the transmit-complete and receive-data-ready conditions. The received data is accessed by reading SPDR.

While the TXE flag is set, the transmit buffer is empty. TXE can be cleared by software or by writing to SPDR. Writing to SPDR will clear TXE and load the transmit buffer. The user may load the buffer while the shift register is busy, i.e. before the current transfer completes. When the current transfer completes, the queued byte in the transmit buffer is moved to the shift register and the next transfer commences. TXE will generate an interrupt if the SPI interrupt is enabled

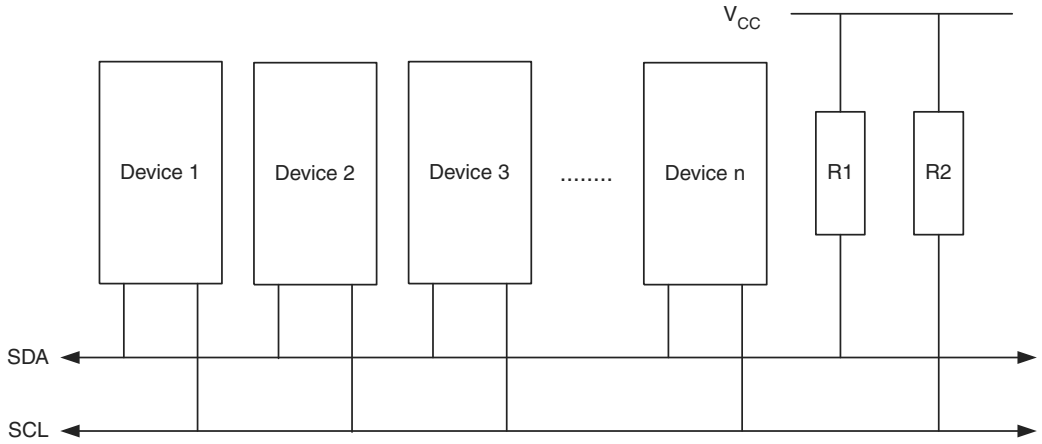
## 18. Two-Wire Serial Interface

The Two-Wire Interface (TWI) is a bi-directional 2-wire serial communication standard. It is designed primarily for simple but efficient integrated circuit (IC) control. The system is comprised of two lines, SCL (Serial Clock) and SDA (Serial Data) that carry information between the ICs connected to them. The only external hardware needed to implement the bus is a single pull-up resistor for each of the TWI bus lines. All devices connected to the bus have individual addresses, and mechanisms for resolving bus contention are inherent in the TWI protocol. The serial data transfer is limited to 400Kbit/s in standard mode. Various communication configurations can be designed using this bus. Figure 18-1 shows a typical 2-wire bus configuration. Any of the devices connected to the bus can be master or slave.

The Two-Wire Interface on the AT89LP provides the following features:

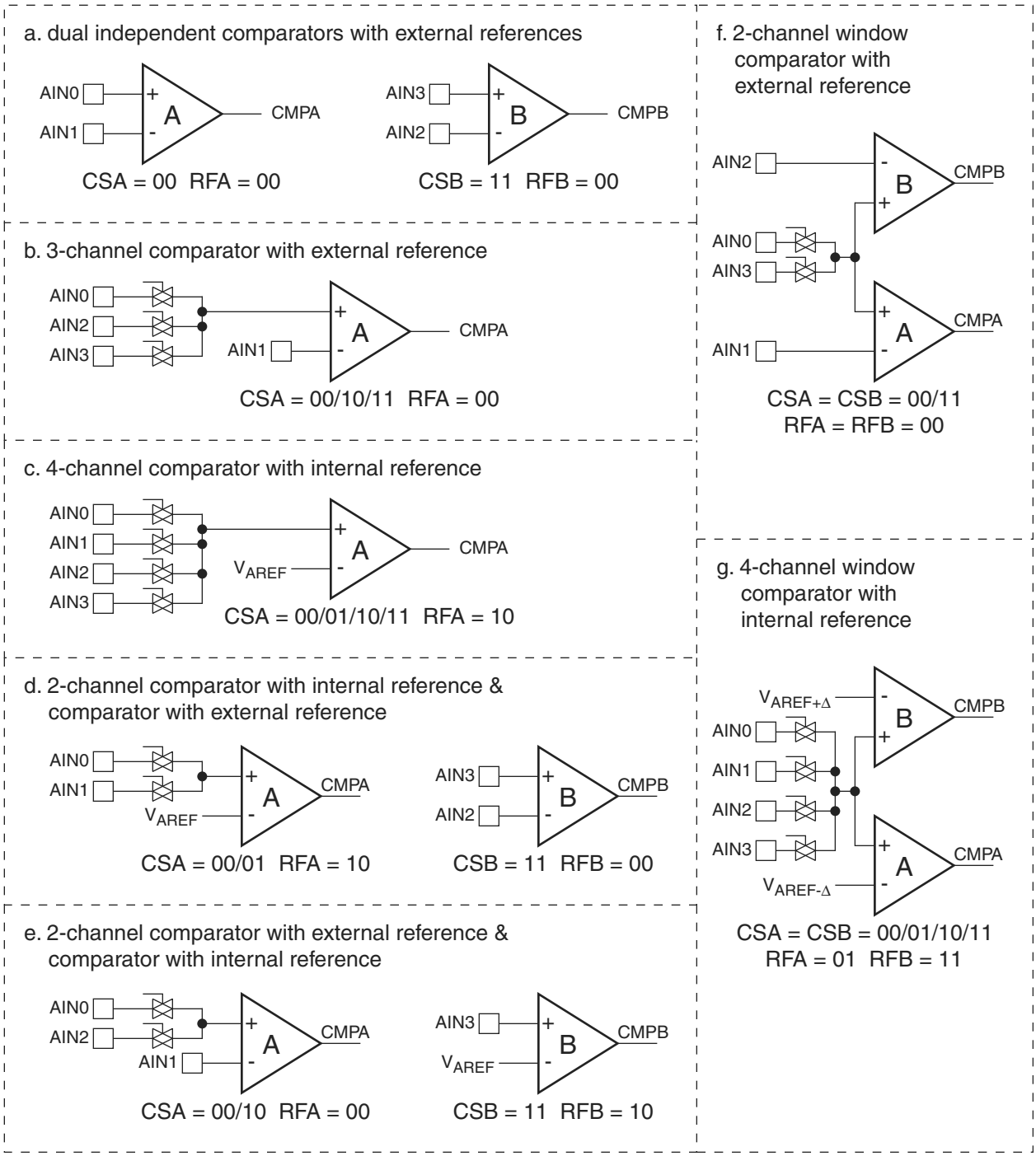
- Simple Yet Powerful and Flexible Communication Interface, only two Bus Lines Needed
- Both Master and Slave Operation Supported
- Device can Operate as Transmitter or Receiver
- 7-bit Address Space Allows up to 128 Different Slave Addresses
- Multi-master Arbitration Support
- Up to 400 kHz Data Transfer Speed
- Fully Programmable Slave Address with General Call Support

**Figure 18-1.** Two-Wire Bus Configuration




As depicted in Figure 18-1, both bus lines are connected to the positive supply voltage through pull-up resistors. The bus drivers of all TWI-compliant devices are open-drain or open-collector. This implements a wired-AND function which is essential to the operation of the interface. A low level on a TWI bus line is generated when one or more TWI devices output a zero. A high level is output when all TWI devices tristate their outputs, allowing the pull-up resistors to pull the line high. Note that all AT89LP devices connected to the TWI bus must be powered in order to allow any bus operation. The number of devices that can be connected to the bus is only limited by the bus capacitance limit of 400 pF and the 7-bit slave address space.

**Figure 19-4.** Dual Comparator Configuration Examples



- The ISP interface uses the SPI clock mode 0 (CPOL = 0, CPHA = 0) exclusively with a maximum frequency of 5 MHz.
- The AT89LP3240/6440 will enter programming mode only when its reset line ($\overline{RST}$) is active (low). To simplify this operation, it is recommended that the target reset can be controlled by the In-System programmer. To avoid problems, the In-System programmer should be able to keep the entire target system reset for the duration of the programming cycle. The target system should never attempt to drive the four SPI lines while reset is active.
- The $\overline{RST}$ input may be disabled to gain an extra I/O pin. In these cases the $\overline{RST}$ pin will always function as a reset during power up. To enter programming the $\overline{RST}$ pin must be driven low prior to the end of Power-On Reset (POR). After POR has completed the device will remain in ISP mode until $\overline{RST}$ is brought high. Once the initial ISP session has ended, the power to the target device must be cycled OFF and ON to enter another session.
- The $\overline{SS}$ pin should not be left floating during reset if ISP is enabled.
- The ISP Enable Fuse must be set to allow programming during any reset period. If the ISP Fuse is disabled, ISP may only be entered at POR.
- For standalone programmers, $\overline{RST}$ may be tied directly to GND to ensure correct entry into Programming mode regardless of the device settings.

## 25.2 Memory Organization

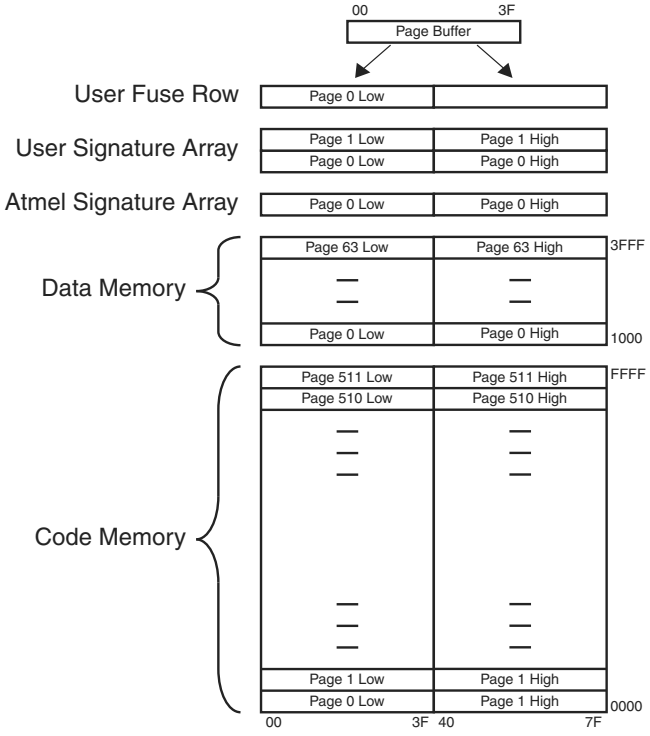
The AT89LP3240/6440 offers 64K bytes of In-System Programmable (ISP) nonvolatile Flash code memory and 8K bytes of nonvolatile Flash data memory. In addition, the device contains a 256-byte User Signature Array and a 128-byte read-only Atmel Signature Array. The memory organization is shown in Table 25-1 and Figure 25-3. The memory is divided into pages of 128 bytes each. A single read or write command may only access half a page (64 bytes) in the memory; however, write with auto-erase commands will erase an entire 128-byte page even though they can only write one half page. Each memory type resides in its own address space and is accessed by commands specific to that memory. However, all memory types share the same page size.

User configuration fuses are mapped as a row in the memory, with each byte representing one fuse. From a programming standpoint, fuses are treated the same as normal code bytes except they are not affected by Chip Erase. Fuses can be enabled at any time by writing 00h to the appropriate locations in the fuse row. However, to disable a fuse, i.e. set it to FFh, the **entire** fuse row must be erased and then reprogrammed. The programmer should read the state of all the fuses into a temporary location, modify those fuses which need to be disabled, then issue a Fuse Write with Auto-Erase command using the temporary data. Lock bits are treated in a similar manner to fuses except they may only be erased (unlocked) by Chip Erase.

**Table 25-1.** AT89LP3240/6440 Memory Organization

| Memory | Capacity | Page Size | # Pages | Address Range |
|---|---|---|---|---|
| CODE | 32KB (AT89LP3240) | 128 bytes | 256 | 0000H – 7FFFH |
| | 64KB (AT89LP6440) | 128 bytes | 512 | 0000H – FFFFH |
| DATA | 8192 bytes | 128 bytes | 64 | 1000H – 3FFFH |
| User Signature | 256 bytes | 128 bytes | 2 | 0000H – 00FFH |
| Atmel Signature | 128 bytes | 128 bytes | 1 | 0000H – 007FH |

**Figure 25-3.** AT89LP6440 Memory Organization




## 25.3 Command Format

Programming commands consist of an opcode byte, two address bytes, and zero or more data bytes. In addition, all command packets must start with a two-byte preamble of AAH and 55H. The preamble increases the noise immunity of the programming interface by making it more difficult to issue unintentional commands. Figure 25-4 on page 161 shows a simplified flow chart of a command sequence.

A sample command packet is shown in Figure 25-5 on page 161. The $\overline{SS}$ pin defines the packet frame. $\overline{SS}$ must be brought low before the first byte in a command is sent and brought back high after the final byte in the command has been sent. The command is not complete until $\overline{SS}$ returns high. Command bytes are issued serially on MOSI. Data output bytes are received serially on MISO. Packets of variable length are supported by returning $\overline{SS}$ high when the final required byte has been transmitted. In some cases command bytes have a don't care value. Don't care bytes in the middle of a packet must be transmitted. Don't care bytes at the end of a packet may be ignored.

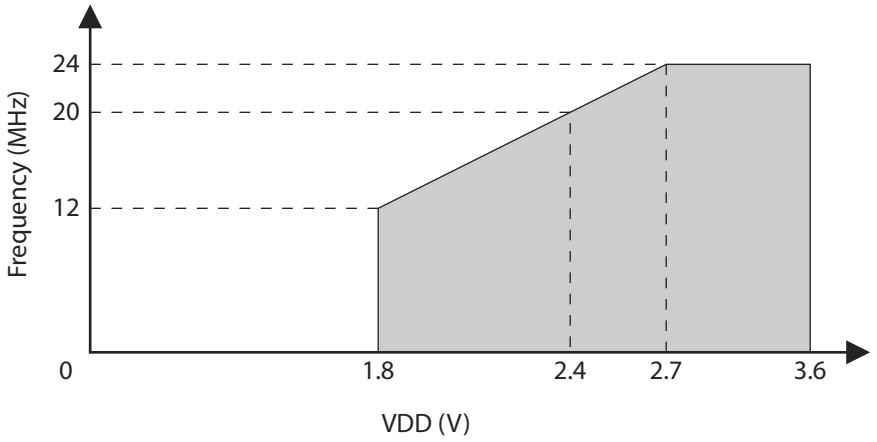
Page oriented instructions always include a full 16-bit address. The higher order bits select the page and the lower order bits select the byte within that page. The AT89LP3240/6440 allocates 6 bits for byte address, 1 bit for low/high half page selection and 9 bits for page address. The half page to be accessed is always fixed by the page address and half select as transmitted. The byte address specifies the starting address for the first data byte. After each data byte has been transmitted, the byte address is incremented to point to the next data byte. This allows a page command to linearly sweep the bytes within a page. If the byte address is incremented past the last byte in the half page, the byte address will roll over to the first byte in the same half page. While loading bytes into the page buffer, overwriting previously loaded bytes will result in data corruption.

## 26.3 Safe Operating Conditions

### 26.3.1 Speed

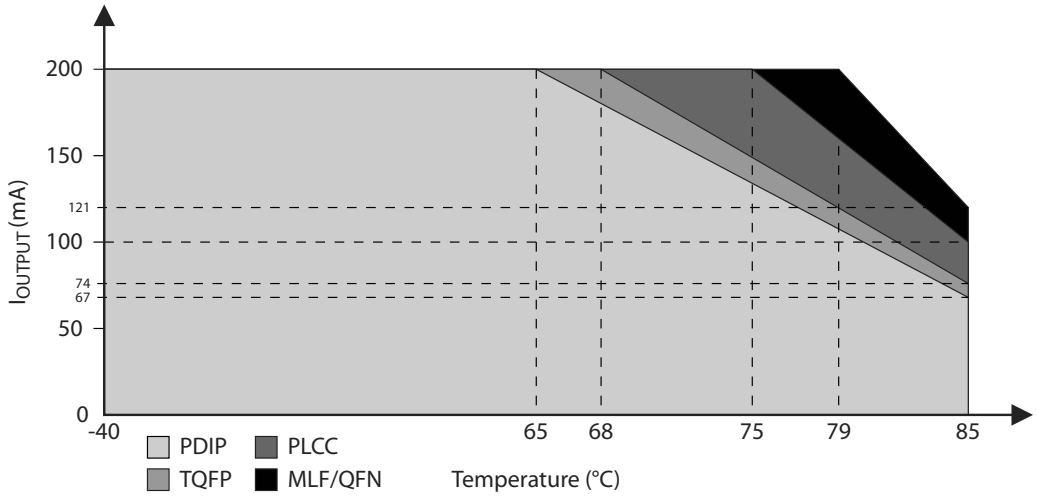
Figure 26-1 shows the safe operating frequencies for the AT89LP3240/6440 versus supply voltage. The device is only gauranteed to operate correctly within this area. Note that the on-chip Brown-out Detector (BOD) has a minimum threshold of 1.8V. Systems that rely on this BOD to prevent incorrect operation due to power loss should only operate at 12 MHz or below. Systems at higher frequencies may require an external BOD.

**Figure 26-1.** Operating Frequency vs. $V_{DD}$




### 26.3.2 Power Dissipation

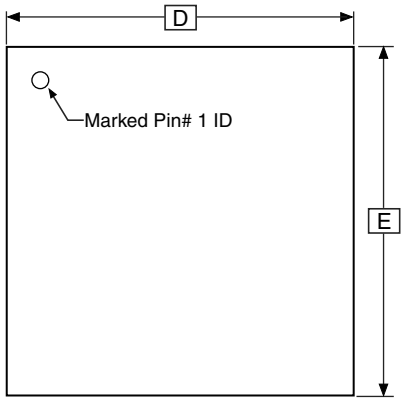
**Figure 26-2.** Maximum Operating Current vs. Temperature ($V_{DD}$ = 3.3V)



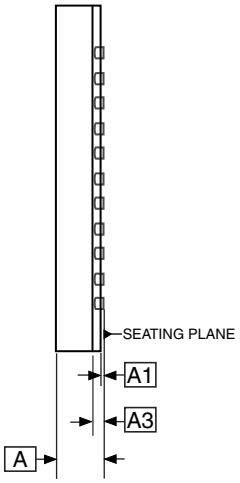

## 26.4 Typical Characteristics

The following charts show typical behavior. These figures are not tested during manufacturing. All current consumption measurements are performed with all I/O pins configured as quasi-bidirectional (with internal pull-ups). A square wave generator with rail-to-rail output is used as an external clock source for consumption versus frequency measurements.

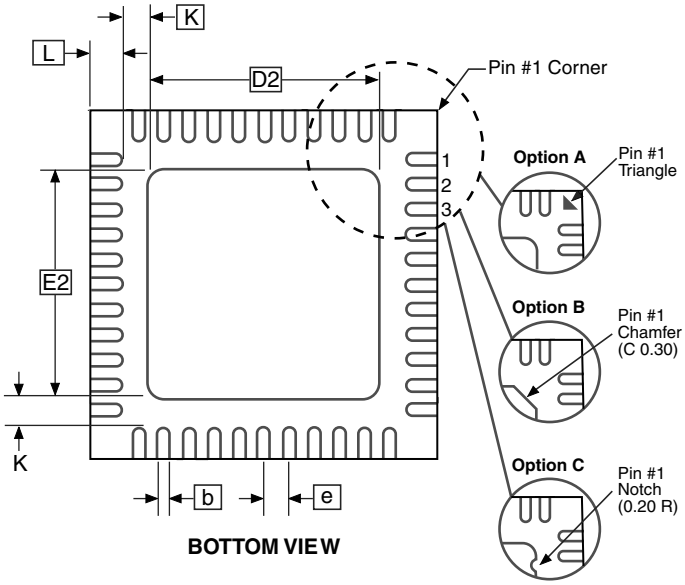
## 28.4 44M1 – VQFN/MLF




TOP VIEW




SIDE VIEW




BOTTOM VIEW

Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 | |
| A1 | – | 0.02 | 0.05 | |
| A3 | | 0.20 REF | | |
| b | 0.18 | 0.23 | 0.30 | |
| D | 6.90 | 7.00 | 7.10 | |
| D2 | 5.00 | 5.20 | 5.40 | |
| E | 6.90 | 7.00 | 7.10 | |
| E2 | 5.00 | 5.20 | 5.40 | |
| e | | 0.50 BSC | | |
| L | 0.59 | 0.64 | 0.69 | |
| K | 0.20 | 0.26 | 0.41 | |

9/26/08

| Package Drawing Contact: packagedrawings@atmel.com | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| | **44M1,** 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.20 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN) | ZWS | 44M1 | H |

## 29. Revision History

| Revision No. | History |
|---|---|
| Revision A – September 2009 | • Initial Release |
| Revision B– September 2010 | • Removed Preliminary status<br>• Updated “DC Characteristics” on page 170<br>• Updated “Typical Characteristics” on page 171<br>• Renamed AVDD to VDD |
| Revision C– February 2011 | • Added section “System Configuration” on page 8<br>• Added the AT89LP3240 device<br>• Updated oscillator connection diagram, Figure 6-1 on page 31 |