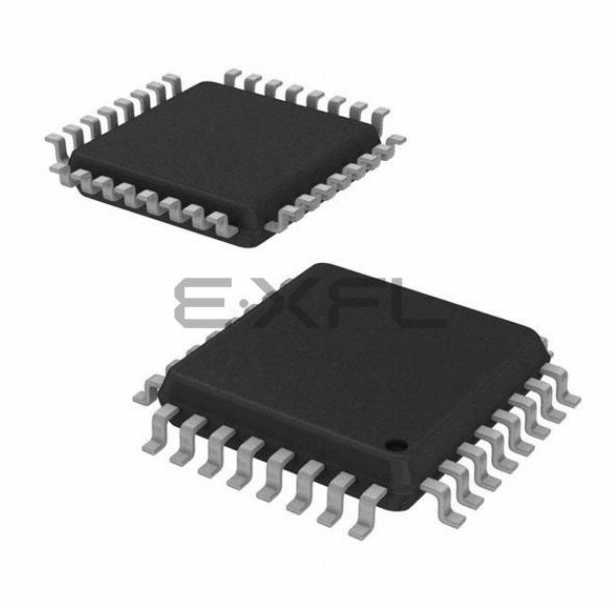

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vr16f0clc

1.4.4 Main External Oscillator (XOSCLCP)

- Loop control Pierce oscillator using 4 MHz to 20 MHz crystal
  - Current gain control on amplitude output
  - Signal with low harmonic distortion
  - Low power
  - Good noise immunity
  - Eliminates need for external current limiting resistor
  - Transconductance sized for optimum start-up margin for typical crystals
  - Oscillator pins shared with GPIO functionality

1.4.5 Internal RC Oscillator (IRC)

- Factory trimmed internal reference clock
  - 1 MHz internal RC oscillator with ±1.3% accuracy over rated temperature range

1.4.6 Internal Phase-Locked Loop (IPLL)

- Phase-locked-loop clock frequency multiplier
  - No external components required
  - Reference divider and multiplier allow large variety of clock rates
  - Automatic bandwidth control mode for low-jitter operation
  - Automatic frequency lock detector
  - Configurable option to spread spectrum for reduced EMC radiation (frequency modulation)
  - Reference clock sources:
    - Internal 1 MHz RC oscillator (IRC)

1.4.7 Clock and Power Management Unit (CPMU)

- Real time interrupt (RTI)
- Clock monitor (CM)
- System reset generation

1.4.8 System Integrity Support

- Power-on reset (POR)
- Illegal address detection with reset
- Low-voltage detection with interrupt or reset
- Computer operating properly (COP) watchdog with option to run on internal RC oscillator
  - Configurable as window COP for enhanced failure detection
  - Can be initialized out of reset using option bits located in flash memory

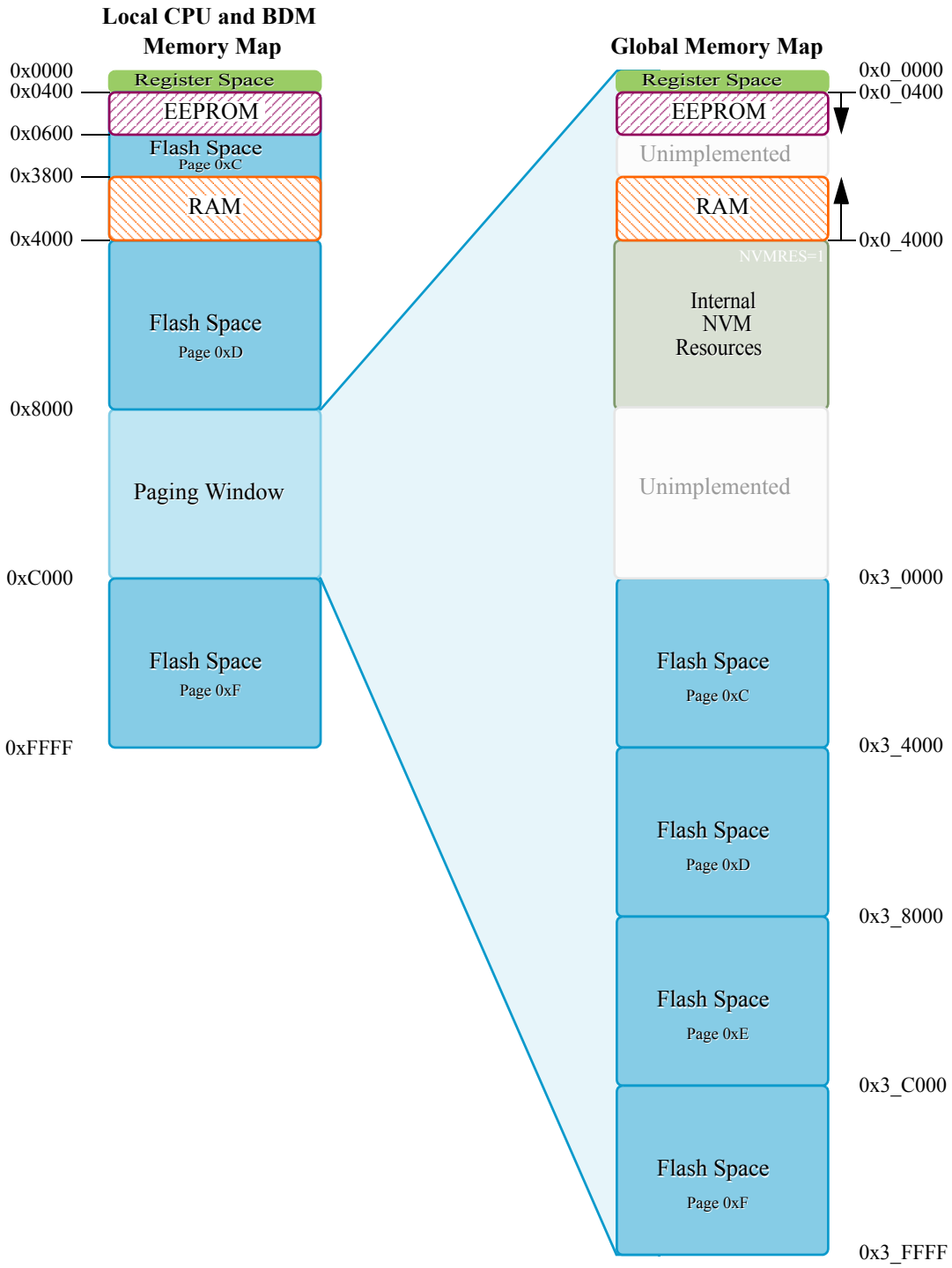


Figure 1-2. MC9S12VR-Family Global Memory Map.

1.7.6 Pinout 32-pin LQFP [1]

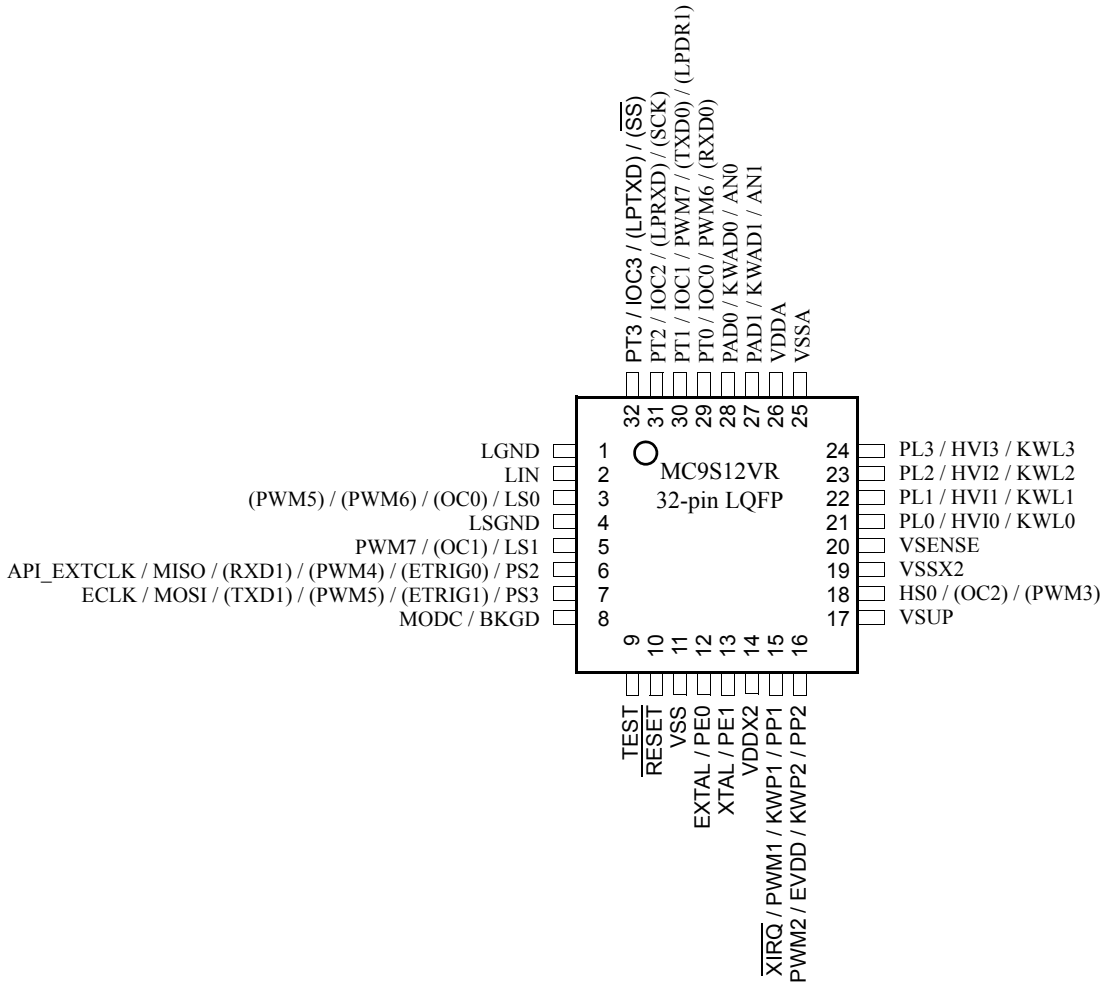


Figure 1-4. MC9S12VR 32-pin LQFP pinout

1. SPI and SCI1 functionality on PS2, PS3, PT2 and PT3 is not available on MC9S12VR32/16.

1.8 Modes of Operation

The MCU can operate in different modes. These are described in 1.8.1 Chip Configuration Summary.

The MCU can operate in different power modes to facilitate power saving when full system performance is not required. These are described in 1.8.2 Low Power Operation.

Some modules feature a software programmable option to freeze the module status whilst the background debug module is active to facilitate debugging.

1.8.1 Chip Configuration Summary

The different modes and the security state of the MCU affect the debug features (enabled or disabled).

The operating mode out of reset is determined by the state of the MODC signal during reset (see Table 1-8). The MODC bit in the MODE register shows the current operating mode and provides limited mode switching during operation. The state of the MODC signal is latched into this bit on the rising edge of $\overline{\text{RESET}}$.

Table 1-8. Chip Modes

Chip Modes	MODC
Normal single chip	1
Special single chip	0

1.8.1.1 Normal Single-Chip Mode

This mode is intended for normal device operation. The opcode from the on-chip memory is being executed after reset (requires the reset vector to be programmed correctly). The processor program is executed from internal memory.

1.8.1.2 Special Single-Chip Mode

This mode is used for debugging single-chip operation, boot-strapping, or security related operations. The background debug module BDM is active in this mode. The CPU executes a monitor program located in an on-chip ROM. BDM firmware waits for additional serial commands through the BKGD pin.

1.8.2 Low Power Operation

The MC9S12VR-Family has two dynamic-power modes (run and wait) and two static low-power modes stop and pseudo stop). For a detailed description refer to Section Chapter 1 S12 Clock, Reset and Power Management Unit (S12CPMU_UHV).

- Dynamic power mode: Run
  - Run mode is the main full performance operating mode with the entire device clocked. The user can configure the device operating speed through selection of the clock source and the phase locked loop (PLL) frequency. To save power, unused peripherals must not be enabled.

Port	Pin Name	Pin Function & Priority[1]	I/O	Description	Pin Function after Reset
P	**PP5**	**$\overline{\text{IRQ}}$**	**I**	**Maskable level- or falling edge-sensitive interrupt**	GPIO
		PWM5	**O**	**Pulse Width Modulator channel 5**	
		ETRIG1	**I**	**ADC external trigger input**	
		PTP[5]/ KWP[5]	**I/O**	**General-purpose; with pin interrupt and wakeup**	
	PP4	**PWM4**	**O**	**Pulse Width Modulator channel 4**	
		ETRIG0	**I**	**ADC external trigger input**	
		PTP[4]/ KWP[4]	**I/O**	**General-purpose; with pin interrupt and wakeup**	
	PP3	**PWM3**	**O**	**Pulse Width Modulator channel 3**	
		PTP[3]/ KWP[3]	**I/O**	**General-purpose; with pin interrupt and wakeup**	
	PP2[3]	PWM2	O	Pulse Width Modulator channel 2	
		PTP[2]/ KWP[2]/ EVDD	I/O	General-purpose; with pin interrupt and wakeup	
	PP1[4]	$\overline{\text{XIRQ}}$	I	Non-maskable level-sensitive interrupt	
		PWM1	O	Pulse Width Modulator channel 1	
		PTP[1]/ KWP[1]	I/O	General-purpose; with interrupt and wakeup	
	PP0[4]	**PWM0**	**O**	**Pulse Width Modulator channel 0**	
		PTP[0]/ KWP[0]	**I/O**	**General-purpose; with interrupt and wakeup**	
L	PL3-0	PTL[3:0]/ KWL[3:0]	I	General-purpose high-voltage input (HVI); with interrupt and wakeup; optional ADC link	GPI (HVI)
AD	**PAD5-2**	**AN[5:2]**	**I**	**ADC analog**	GPIO
		PTAD[5:2]/ KWAD[5:2]	**I/O**	**General-purpose; with interrupt and wakeup**	
	PAD1-0	AN[1:0]	I	ADC analog	
		PTAD[1:0]/ KWAD[1:0]	I/O	General-purpose; with interrupt and wakeup	

1 Signals in parentheses denote alternative module routing pins. Signals in **bold underlined** are only available on S12VR64/48.

2 Function active when $\overline{\text{RESET}}$ asserted

3 High current capable high-side output (20mA) with over-current interrupt and protection for all sources (see 2.4.4.3/2-112)

4 High-current capable output (10 mA)

2.3 Memory Map and Register Definition

This section provides a detailed description of all PIM registers.

4.3 Memory Map and Registers

This section provides a detailed description of all registers accessible in the S12CPMU_UHV_V8.

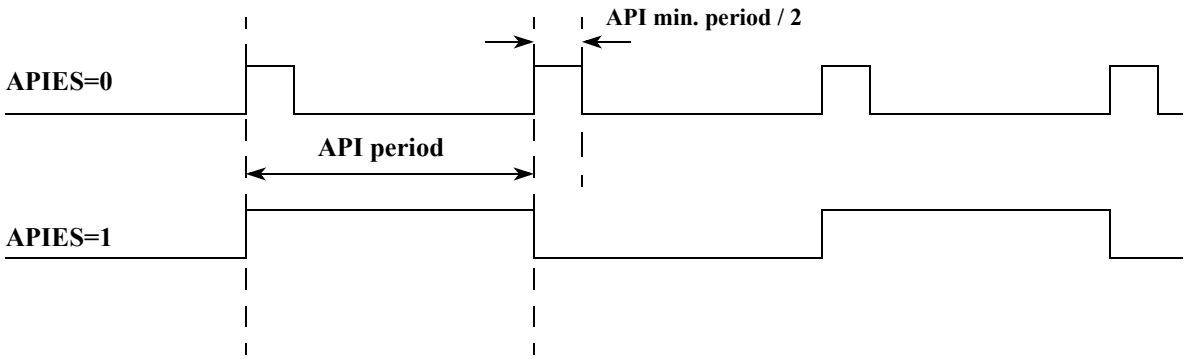
4.3.1 Module Memory Map

The S12CPMU_UHV_V8 registers are shown in Figure 4-3.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0034	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0035	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0036	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0037	CPMUFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	OSCIF	UPOSC
		W								
0x0038	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	**PMRF**
		W								
0x0039	CPMUCLKS	R	PLLSEL	PSTP	CSAD	COP OSCSEL1	PRE	PCE	RTI OSCSEL	COP OSCSEL0
		W								
0x003A	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
0x003B	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x003C	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x003D	RESERVED CPMUTEST0	R	0	0	0	0	0	0	0	0
		W								
0x003E	RESERVED CPMUTEST1	R	0	0	0	0	0	0	0	0
		W								
0x003F	CPMU ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02F0	CPMU HTCTL	R	0	0	VSEL	0	HTE	HTDS	HTIE	HTIF
		W								
0x02F1	CPMU LVCTL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								
0x02F2	CPMU APICTL	R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
		W								
			= Unimplemented or Reserved							

Figure 4-3. CPMU Register Summary[1]

Figure 4-20. Waveform selected on API_EXTCLK pin (APIEA=1, APIFE=1)



4.3.2.19 High Temperature Trimming Register (CPMUHTTR)

The CPMUHTTR register configures the trimming of the S12CPMU_UHV_V8 temperature sense.

0x02F7

	7	6	5	4	3	2	1	0
R	HTOE	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
W								
Reset	0	0	0	0	F	F	F	F

After de-assert of System Reset a trim value is automatically loaded from the Flash memory. See Device specification for details.

= Unimplemented or Reserved

Figure 4-25. High Temperature Trimming Register (CPMUHTTR)

Read: Anytime

Write: Anytime

Table 4-24. CPMUHTTR Field Descriptions

Field	Description
7 HTOE	**High Temperature Offset Enable Bit** — If set the temperature sense offset is enabled. 0 The temperature sense offset is disabled. HTTR[3:0] bits don't care. 1 The temperature sense offset is enabled. HTTR[3:0] select the temperature offset.
3–0 HTTR[3:0]	**High Temperature Trimming Bits** — See Table 4-25 for trimming effects.

Table 4-25. Trimming Effect of HTTR

HTTR[3:0]	Temperature sensor voltage V_{HT}	Interrupt threshold temperatures T_{HTIA} and T_{HTID}
0000	lowest	highest
0001	increasing	decreasing
....		
1110		
1111	highest	lowest

4.7.2 Application information for COP and API usage

In many applications the COP is used to check that the program is running and sequencing properly. Often the COP is kept running during Stop Mode and periodic wake-up events are needed to service the COP on time and maybe to check the system status.

For such an application it is recommended to use the ACLK as clock source for both COP and API. This guarantees lowest possible IDD current during Stop Mode. Additionally it eases software implementation using the same clock source for both, COP and API.

The Interrupt Service Routine (ISR) of the Autonomous Periodic Interrupt API should contain the write instruction to the CPMUARMCOP register. The value (byte) written is derived from the “main routine” (alternating sequence of $55 and $AA) of the application software.

Using this method, then in the case of a runtime or program sequencing issue the application “main routine” is not executed properly anymore and the alternating values are not provided properly. Hence the COP is written at the correct time (due to independent API interrupt request) but the wrong value is written (alternating sequence of $55 and $AA is no longer maintained) which causes a COP reset.

If the COP is stopped during any Stop Mode it is recommended to service the COP shortly before Stop Mode is entered.

for a valid match. Similarly the SZE and SZ bits allow the size of access (word or byte) to be considered in the compare. Only comparators A and B feature SZE and SZ.

The TAG bit in each comparator control register is used to determine the match condition. By setting TAG, the comparator qualifies a match with the output of opcode tracking logic and a state sequencer transition occurs when the tagged instruction reaches the CPU execution stage. Whilst tagging the RW, RWE, SZE, and SZ bits and the comparator data registers are ignored; the comparator address register must be loaded with the exact opcode address.

If the TAG bit is clear (forced type match) a comparator match is generated when the selected address appears on the system address bus. If the selected address is an opcode address, the match is generated when the opcode is fetched from the memory, which precedes the instruction execution by an indefinite number of cycles due to instruction pipelining. For a comparator match of an opcode at an odd address when TAG = 0, the corresponding even address must be contained in the comparator register. Thus for an opcode at odd address (n), the comparator register must contain address (n–1).

Once a successful comparator match has occurred, the condition that caused the original match is not verified again on subsequent matches. Thus if a particular data value is verified at a given address, this address may not still contain that data value when a subsequent match occurs.

Match[0, 1, 2] map directly to Comparators [A, B, C] respectively, except in range modes (see Section 6.3.2.4, “Debug Control Register2 (DBGC2)). Comparator channel priority rules are described in the priority section (Section 6.4.3.4, “Channel Priorities).

6.4.2.1 Single Address Comparator Match

With range comparisons disabled, the match condition is an exact equivalence of address bus with the value stored in the comparator address registers. Further qualification of the type of access (R/W, word/byte) and databus contents is possible, depending on comparator channel.

6.4.2.1.1 Comparator C

Comparator C offers only address and direction (R/W) comparison. The exact address is compared, thus with the comparator address register loaded with address (n) a word access of address (n–1) also accesses (n) but does not cause a match.

Table 6-32. Comparator C Access Considerations

Condition For Valid Match	Comp C Address	RWE	RW	Examples
Read and write accesses of ADDR[n]	ADDR[n][1]	0	X	LDAA ADDR[n] STAA #$BYTE ADDR[n]
Write accesses of ADDR[n]	ADDR[n]	1	0	STAA #$BYTE ADDR[n]
Read accesses of ADDR[n]	ADDR[n]	1	1	LDAA #$BYTE ADDR[n]

1 A word access of ADDR[n-1] also accesses ADDR[n] but does not generate a match.
The comparator address register must contain the exact address from the code.

Clock Source = bus clock, where bus clock= 10 MHz (100 ns period)

PPOLx = 0

PWMPERx = 4

PWMDTYx = 1

PWMx Frequency = 10 MHz/8 = 1.25 MHz

PWMx Period = 800 ns

PWMx Duty Cycle = 3/4 *100% = 75%

Shown in Figure 9-20 is the output waveform generated.

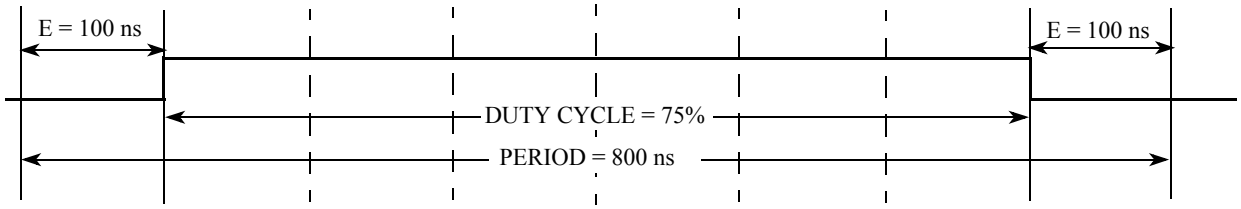


Figure 9-20. PWM Center Aligned Output Example Waveform

9.4.2.7 PWM 16-Bit Functions

The scalable PWM timer also has the option of generating up to 8-channels of 8-bits or 4-channels of 16-bits for greater PWM resolution. This 16-bit channel option is achieved through the concatenation of two 8-bit channels.

The PWMCTL register contains four control bits, each of which is used to concatenate a pair of PWM channels into one 16-bit channel. Channels 6 and 7 are concatenated with the CON67 bit, channels 4 and 5 are concatenated with the CON45 bit, channels 2 and 3 are concatenated with the CON23 bit, and channels 0 and 1 are concatenated with the CON01 bit.

NOTE

Change these bits only when both corresponding channels are disabled.

When channels 6 and 7 are concatenated, channel 6 registers become the high order bytes of the double byte channel, as shown in Figure 9-21. Similarly, when channels 4 and 5 are concatenated, channel 4 registers become the high order bytes of the double byte channel. When channels 2 and 3 are concatenated, channel 2 registers become the high order bytes of the double byte channel. When channels 0 and 1 are concatenated, channel 0 registers become the high order bytes of the double byte channel.

When using the 16-bit concatenated mode, the clock source is determined by the low order 8-bit channel clock select control bits. That is channel 7 when channels 6 and 7 are concatenated, channel 5 when channels 4 and 5 are concatenated, channel 3 when channels 2 and 3 are concatenated, and channel 1 when channels 0 and 1 are concatenated. The resulting PWM is output to the pins of the corresponding low order 8-bit channel as also shown in Figure 9-21. The polarity of the resulting PWM output is controlled by the PPOLx bit of the corresponding low order 8-bit channel as well.

10.3.2.6 SCI Control Register 2 (SCICR2)

	7	6	5	4	3	2	1	0
R W	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset	0	0	0	0	0	0	0	0

Figure 10-9. SCI Control Register 2 (SCICR2)

Read: Anytime

Write: Anytime

Table 10-10. SCICR2 Field Descriptions

Field	Description
7 TIE	**Transmitter Interrupt Enable Bit** — TIE enables the transmit data register empty flag, TDRE, to generate interrupt requests. 0 TDRE interrupt requests disabled 1 TDRE interrupt requests enabled
6 TCIE	**Transmission Complete Interrupt Enable Bit** — TCIE enables the transmission complete flag, TC, to generate interrupt requests. 0 TC interrupt requests disabled 1 TC interrupt requests enabled
5 RIE	**Receiver Full Interrupt Enable Bit** — RIE enables the receive data register full flag, RDRF, or the overrun flag, OR, to generate interrupt requests. 0 RDRF and OR interrupt requests disabled 1 RDRF and OR interrupt requests enabled
4 ILIE	**Idle Line Interrupt Enable Bit** — ILIE enables the idle line flag, IDLE, to generate interrupt requests. 0 IDLE interrupt requests disabled 1 IDLE interrupt requests enabled
3 TE	**Transmitter Enable Bit** — TE enables the SCI transmitter and configures the TXD pin as being controlled by the SCI. The TE bit can be used to queue an idle preamble. 0 Transmitter disabled 1 Transmitter enabled
2 RE	**Receiver Enable Bit** — RE enables the SCI receiver. 0 Receiver disabled 1 Receiver enabled
1 RWU	**Receiver Wakeup Bit** — Standby state 0 Normal operation. 1 RWU enables the wakeup function and inhibits further receiver interrupt requests. Normally, hardware wakes the receiver by automatically clearing RWU.
0 SBK	**Send Break Bit** — Toggling SBK sends one break character (10 or 11 logic 0s, respectively 13 or 14 logics 0s if BRK13 is set). Toggling implies clearing the SBK bit before the break character has finished transmitting. As long as SBK is set, the transmitter continues to send complete break characters (10 or 11 bits, respectively 13 or 14 bits). 0 No break characters 1 Transmit break characters

To determine the value of a data bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 10-18 summarizes the results of the data bit samples.

Table 10-18. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

NOTE

The RT8, RT9, and RT10 samples do not affect start bit verification. If any or all of the RT8, RT9, and RT10 start bit samples are logic 1s following a successful start bit verification, the noise flag (NF) is set and the receiver assumes that the bit is a start bit (logic 0).

To verify a stop bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 10-19 summarizes the results of the stop bit samples.

Table 10-19. Stop Bit Recovery

RT8, RT9, and RT10 Samples	Framing Error Flag	Noise Flag
000	1	0
001	1	1
010	1	1
011	0	1
100	1	1
101	0	1
110	0	1
111	0	0

The activation of the LSE0 or LSE1 bits enable the related low-side driver. The driver is controlled by the selected source in the Port Integration Module (see PIM chapter).

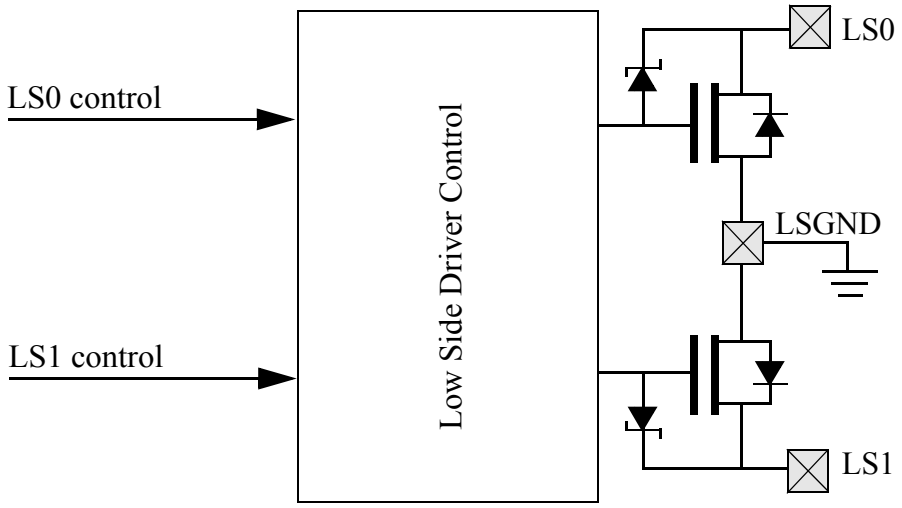
2. MCU stop mode

   During stop mode operation the low-side drivers are shut down, i.e. the low-side drivers are disabled and their drivers are turned off. The bits in the data register which control the drivers (LSDRx) are cleared automatically. After returning from stop mode the drivers are re-enabled. If the data register bits (LSDRx) were chosen as source in PIM module, then the respective low-side driver stays turned off until the software sets the associated bit in the data register (LSDRx). When the timer or PWM were chosen as source, the respective low-side driver is controlled by the timer or PWM without further handling. When it is required that the driver stays turned off after the stop mode for this case (PWM or timer), the software must take the appropriate action to turn off the driver before entering stop mode.

15.1.3 Block Diagram

Figure 15-1 shows a block diagram of the LSDRV module. The module consists of a control and an output stage. Internal functions can be routed to control the low-side drivers. See PIM chapter for routing options.

Figure 15-1. LSDRV Block Diagram



16.3.2.6 LIN Status Register (LPSR)

Module Base + Address 0x0005 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	LPDT	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 16-8. LIN Status Register (LPSR)

[1] Read: Anytime
Write: Never, writes to this register have no effect

Table 16-7. LPSR Field Description

Field	Description
7 LPDT	**LIN Transmitter TxD-dominant timeout Status Bit** — This read-only bit signals that the LPTxD pin is still dominant after a TxD-dominant timeout. As long as the LPTxD is dominant after the timeout the LIN transmitter is shut down and the LPTDIF is set again after attempting to clear it. 0 If there was a TxD-dominant timeout, LPTxD has ceased to be dominant after the timeout. 1 LPTxD is still dominant after a TxD-dominant timeout.

Table 18-7. FCLKDIV Field Descriptions (continued)

Field	Description
6 FDIVLCK	**Clock Divider Locked** 0 FDIV field is open for writing 1 FDIV value is locked and cannot be changed. Once the lock bit is set high, only reset can clear this bit and restore writability to the FDIV field in normal mode.
5–0 FDIV[5:0]	**Clock Divider Bits** — FDIV[5:0] must be set to effectively divide BUSCLK down to 1 MHz to control timed events during Flash program and erase algorithms. Table 18-8 shows recommended values for FDIV[5:0] based on the BUSCLK frequency. Please refer to Section 18.4.4, "Flash Command Operations," for more information.

Table 18-8. FDIV values for various BUSCLK Frequencies

BUSCLK Frequency (MHz)		FDIV[5:0]	BUSCLK Frequency (MHz)		FDIV[5:0]
MIN[1]	MAX[2]		MIN[1]	MAX[2]	
1.0	1.6	0x00	16.6	17.6	0x10
1.6	2.6	0x01	17.6	18.6	0x11
2.6	3.6	0x02	18.6	19.6	0x12
3.6	4.6	0x03	19.6	20.6	0x13
4.6	5.6	0x04	20.6	21.6	0x14
5.6	6.6	0x05	21.6	22.6	0x15
6.6	7.6	0x06	22.6	23.6	0x16
7.6	8.6	0x07	23.6	24.6	0x17
8.6	9.6	0x08	24.6	25.6	0x18
9.6	10.6	0x09			
10.6	11.6	0x0A			
11.6	12.6	0x0B			
12.6	13.6	0x0C			
13.6	14.6	0x0D			
14.6	15.6	0x0E			
15.6	16.6	0x0F			

1 BUSCLK is Greater Than this value.

2 BUSCLK is Less Than or Equal to this value.

18.3.2.2 Flash Security Register (FSEC)

The FSEC register holds all bits associated with the security of the MCU and Flash module.

Table 19-17. FPROT Field Descriptions (continued)

Field	Description
2 FPLDIS	**Flash Protection Lower Address Range Disable** — The FPLDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory beginning with global address 0x3_8000. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
1–0 FPLS[1:0]	**Flash Protection Lower Address Size** — The FPLS bits determine the size of the protected/unprotected area in P-Flash memory as shown in Table 19-20. The FPLS bits can only be written to while the FPLDIS bit is set.

Table 19-18. P-Flash Protection Function

FPOPEN	FPHDIS	FPLDIS	Function[1]
1	1	1	No P-Flash Protection
1	1	0	Protected Low Range
1	0	1	Protected High Range
1	0	0	Protected High and Low Ranges
0	1	1	Full P-Flash Memory Protected
0	1	0	Unprotected Low Range
0	0	1	Unprotected High Range
0	0	0	Unprotected High and Low Ranges

1 For range sizes, refer to Table 19-19 and Table 19-20.

Table 19-19. P-Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0x3_F800–0x3_FFFF	2 Kbytes
01	0x3_F000–0x3_FFFF	4 Kbytes
10	0x3_E000–0x3_FFFF	8 Kbytes
11	0x3_C000–0x3_FFFF	16 Kbytes

Table 19-20. P-Flash Protection Lower Address Range

FPLS[1:0]	Global Address Range	Protected Size
00	0x3_8000–0x3_83FF	1 Kbyte
01	0x3_8000–0x3_87FF	2 Kbytes
10	0x3_8000–0x3_8FFF	4 Kbytes
11	0x3_8000–0x3_9FFF	8 Kbytes

All possible P-Flash protection scenarios are shown in Figure 19-14Although the protection scheme is loaded from the Flash memory at global address 0x3_FF0C during the reset sequence, it can be changed by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in Normal Single Chip Mode while providing as much protection as possible if reprogramming is not required.

Table I-2. Static Electrical Characteristics - Supply Voltage Sense - (BATS).

Characteristics noted under conditions 5.5V ≤ VSUP ≤ 18 V, -40°C ≤ T_J ≤ 150°C[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C[2] under nominal conditions unless otherwise noted. All parameters in this table assume a in series connected R_{VSENSE_R} at VSENSE pin unless otherwise noted and are valid on input voltage of R_{VSENSE_R} and not on VSENSE pin.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
9	VSENSE Series Resistor Required to be placed externally at VSENSE pin.	R_{VSENSE_R}	9.5	10	10.5	kΩ
10	VSENSE Impedance If path to ground is enabled. Value at VSENSE pin. R_{VSENSE_R} is excluded.	R_{VSEN_IMP}	–	350	–	kΩ
11	VSENSE Input Capacitance	C_{VSEN_IN}	–	8	–	pF

1 T_J: Junction Temperature

2 T_A: Ambient Temperature

3 V_{ADC}: Voltage accessible at the ATD input channel

I.3 Dynamic Electrical Characteristics

Table I-3. Dynamic Electrical Characteristics - Supply Voltage Sense - (BATS).

Characteristics noted under conditions 5.5V ≤ VSUP ≤ 18 V, -40°C ≤ T_J ≤ 150°C[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C[2] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Enable Stabilisation Time	T_{EN_UNC}	–	1	–	µs
2	Voltage Warning Low Pass Filter	f_{VWLP_filter}	–	0.5	–	MHz

1 T_J: Junction Temperature

2 T_A: Ambient Temperature

P.13 0x0070-0x009F Analog to Digital Converter 10-Bit 6-Channel (ATD) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0074	ATDCTL4	R	SMP2	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		W								
0x0075	ATDCTL5	R	0	SC	SCAN	MULT	CD	CC	CB	CA
		W								
0x0076	ATDSTAT0	R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
		W								
0x0077	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0078	ATDCMPEH	R	0	0	0	0	0	0	0	0
		W								
0x0079	ATDCMPEL	R	0]	0	CMPE[5:0]					
		W								
0x007A	ATDSTAT2H	R								
		W								
0x007B	ATDSTAT2L	R	0	0	CCF[5:0]					
		W								
0x007C	ATDDIENH	R	0	0	0	0	0	0	0	0
		W								
0x007D	ATDDIENL	R	0	0	IEN[5:0]					
		W								
0x007E	ATDCMPHTH	R	0	0	0	0	0	0	0	0
		W								
0x007F	ATDCMPHTL	R	0	0	CMPHT[5:0]					
		W								
0x0080	ATDDR0H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0081	ATDDR0L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x0082	ATDDR1H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0083	ATDDR1L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x0084	ATDDR2H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0085	ATDDR2L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x0086	ATDDR3H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0087	ATDDR3L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x0088	ATDDR4H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0089	ATDDR4L	R	Bit7	Bit6	0	0	0	0	0	0
		W								

P.19 0x0100-0x0113 NVM Contol Register (FTMRG) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0111	FRSV5	R	0	0	0	0	0	0	0	0
		W								
0x0112	FRSV6	R	0	0	0	0	0	0	0	0
		W								
0x0113	FRSV7	R	0	0	0	0	0	0	0	0
		W								

P.20 0x0114-0x011F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0114-0x011F	Reserved	R	0	0	0	0	0	0	0	0
		W								

P.21 0x0120 Interrupt Vector Base Register

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0120	IVBR	R W	IVB_ADDR[7:0]							

P.22 0x0121-0x013F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0121-0x013F	Reserved	R	0	0	0	0	0	0	0	0
		W								