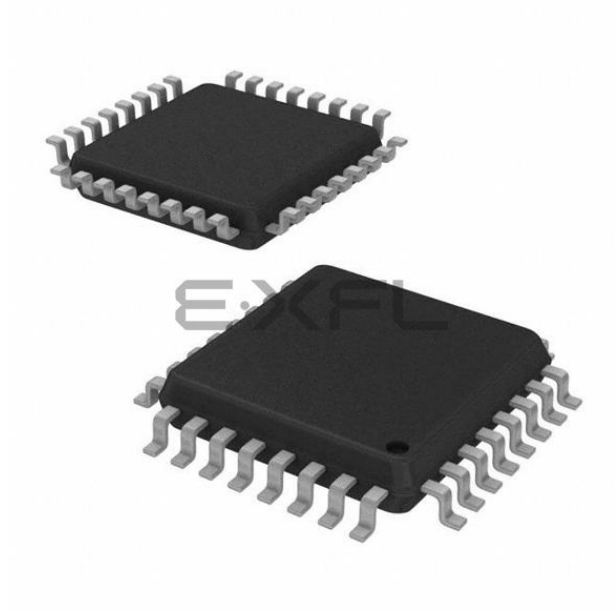

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Program Memory Type	FLASH
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RAM Size	2K x 8
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Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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Supplier Device Package	32-LQFP (7x7)
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Chapter 7
Interrupt Module (S12SINTV1)

Chapter 8
Analog-to-Digital Converter (ADC12B6CV2)

1.7.2.15.4 MOSI Signal

This signal is associated with the MOSI functionality of the serial peripheral interface SPI. This signal acts as master output during master mode or as slave input during slave mode

1.7.2.16 LINPHY Signals

1.7.2.16.1 VLINSUP — Positive Power Supply

This is the power supply to the LINPHY. The VLINSUP is connected to VSUP.

1.7.2.16.2 LPTXD Signal

This signal is the LINPHY transmit input. See Figure 2-22

1.7.2.16.3 LPRXD Signal

This signal is the LINPHY receive output. See Figure 2-22

1.7.2.17 SCI Signals

1.7.2.17.1 RXD[1:0] Signals

Those signals are associated with the receive functionality of the serial communication interfaces SCI1-0.

1.7.2.17.2 TXD[1:0] Signals

Those signals are associated with the transmit functionality of the serial communication interfaces SCI1-0.

1.7.2.18 PWM[7:0] Signals

The signals PWM[7:0] are associated with the PWM module outputs.

1.7.2.19 Internal Clock outputs

1.7.2.19.1 ECLK

This signal is associated with the output of the divided bus clock (ECLK).

NOTE

This feature is only intended for debug purposes at room temperature.
It must not be used for clocking external devices in an application.

1.7.2.20 ETRIG[1:0]

These signals are inputs to the Analog-to-Digital Converter. Their purpose is to trigger ADC conversions.

Table 2-7. ECLKCTL Register Field Descriptions

Field	Description
7 NECLK	**No ECLK** — Disable ECLK output This bit controls the availability of a free-running clock on the ECLK pin. This clock has a fixed rate equivalent to the internal bus clock. 1 ECLK disabled 0 ECLK enabled

2.3.7 PIM Miscellaneous Register (PIMMISC)

Address 0x001D — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	OCPE	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-5. PIM Miscellaneous Register (PIMMISC)

[1] Read: Anytime
Write: Anytime

Table 2-8. PIMMISC Register Field Descriptions

Field	Description
7 OCPE	**Over-Current Protection Enable**— Activate over-current detector on PP2 Refer to Section 2.5.3, “Over-Current Protection on EVDD” 1 PP2 over-current detector enabled 0 PP2 over-current detector disabled

2.3.8 IRQ Control Register (IRQCR)[1]

Address 0x001E (S12VR64/48) — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	IRQE	IRQEN	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-6. IRQ Control Register (IRQCR)

[1] Read: Anytime
Write:
IRQE: Once in normal mode, anytime in special mode
IRQEN: Anytime

1. This register is applicable for S12VR64 and S12VR48 in 48 pin package

2.3.21 Port S Data Direction Register (DDRS)

Address 0x024A (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-22. Port S Data Direction Register (DDRS - S12VR64/48)

1 Read: Anytime
Write: Anytime

Address 0x024A (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	DDRS3	DDRS2	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-23. Port S Data Direction Register (DDRS - S12VR32/16)

1 Read: Anytime
Write: Anytime

Table 2-19. DDRS Register Field Descriptions

Field	Description
5 DDRS	**Data Direction Register port S —** This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
4 DDRS	**Data Direction Register port S —** This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
3 DDRS	**Data Direction Register port S —** This bit determines whether the associated pin is an input or output. The ECLK output function, routed SCI1 and routed PWM function forces the I/O state to output if enabled. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. In these cases the data direction bit will not change. The routed ETRIG function has no effect on the I/O state. 1 Associated pin is configured as output 0 Associated pin is configured as input

2.3.45 Port AD Polarity Select Register (PPS1AD)

Address 0x027B (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PPS1AD5	PPS1AD4	PPS1AD3	PPS1AD2	PPS1AD1	PPS1AD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-64. Port AD Polarity Select Register (PPS1AD - S12VR64/48)

1 Read: Anytime
Write: Anytime

Address 0x027B (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PPS1AD1	PPS1AD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-65. Port AD Polarity Select Register (PPS1AD - S12VR32/16)

1 Read: Anytime
Write: Anytime

Table 2-45. PPS1AD Register Field Descriptions

Field	Description
5-0 PPS1AD	**Pull device Polarity Select register 1 port AD** — Configure pull device polarity and pin interrupt edge polarity on input pin This bit selects a pullup or a pulldown device if enabled on the associated port input pin. This bit also selects the polarity of the active pin interrupt edge. 1 A pulldown device is selected; rising edge selected 0 A pullup device is selected; falling edge selected

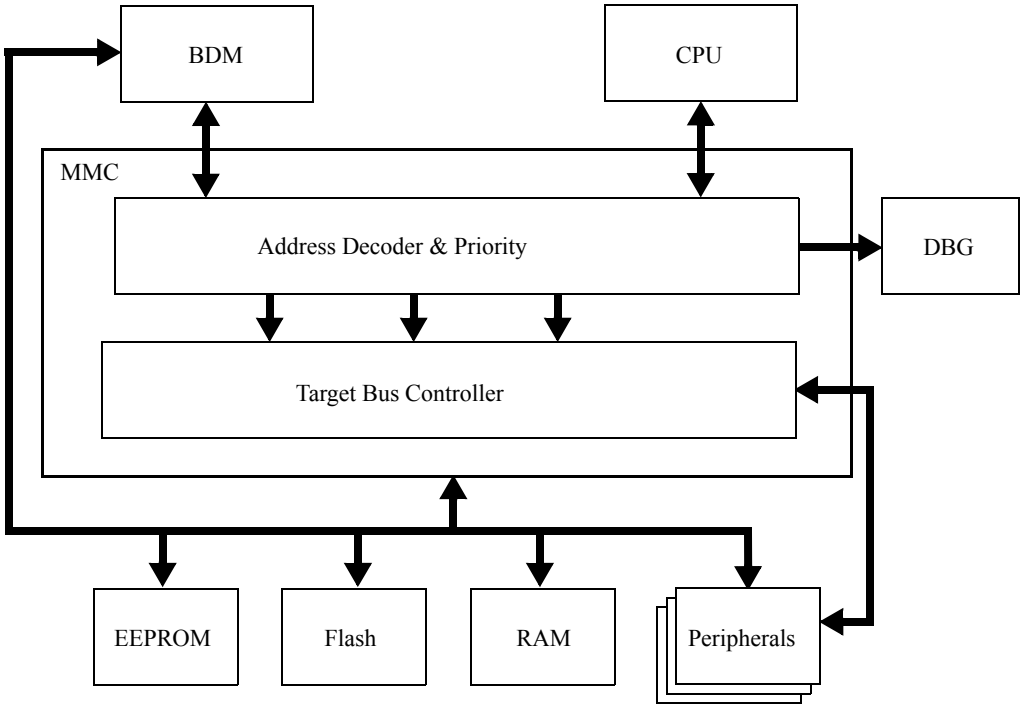


Figure 3-1. S12GMMC Block Diagram

3.2 External Signal Description

The S12GMMC uses two external pins to determine the devices operating mode: RESET and MODC (Figure 3-3) See Device User Guide (DUG) for the mapping of these signals to device pins.

Table 3-3. External System Pins Associated With S12GMMC

Pin Name	Pin Functions	Description
$\overline{\text{RESET}}$ (See Section Device Overview)	$\overline{\text{RESET}}$	The $\overline{\text{RESET}}$ pin is used the select the MCU's operating mode.
$\overline{\text{MODC}}$ (See Section Device Overview)	MODC	The MODC pin is captured at the rising edge of the $\overline{\text{RESET}}$ pin. The captured value determines the MCU's operating mode.

3.3 Memory Map and Registers

3.3.1 Module Memory Map

A summary of the registers associated with the S12GMMC block is shown in Figure 3-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

VDDX has to be connected externally to VDDA.

4.2.6 VSS— Ground Pin

VSS is the ground pin for the core logic. On the board VSSX, VSSA and VSS need to be connected together to the application ground.

4.2.7 API_EXTCLK — API external clock output pin

This pin provides the signal selected via APIES and is enabled with APIEA bit. See the device specification if this clock output is available on this device and to which pin it might be connects.

4.2.8 VDD— Internal Regulator Output Supply (Core Logic)

Node VDD is a device internal supply output of the voltage regulator that provides the power supply for the core logic.

This supply domain is monitored by the Low Voltage Reset circuit.

4.2.9 VDDF— Internal Regulator Output Supply (NVM Logic)

Node VDDF is a device internal supply output of the voltage regulator that provides the power supply for the NVM logic.

This supply domain is monitored by the Low Voltage Reset circuit.

4.2.10 TEMPSENSE — Internal Temperature Sensor Output Voltage

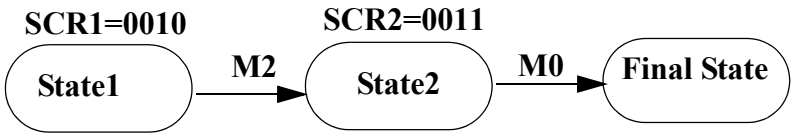
Depending on the VSEL setting either the voltage level generated by the temperature sensor or the VREG bandgap voltage is driven to a special channel input of the ADC Converter. See device level specification for connectivity of ADC special channels.

A trigger is generated if a given sequence of 2 code events is executed, whereby the first event is entry into a range (COMPA,COMPB configured for range mode). M1 is disabled in range modes.

Figure 6-29. Scenario 2b

A trigger is generated if a given sequence of 2 code events is executed, whereby the second event is entry into a range (COMPA,COMPB configured for range mode)

Figure 6-30. Scenario 2c

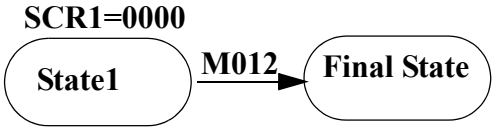


All 3 scenarios 2a,2b,2c are possible with the S12SDBGV1 SCR encoding

6.5.4 Scenario 3

A trigger is generated immediately when one of up to 3 given events occurs

Figure 6-31. Scenario 3



Scenario 3 is possible with S12SDBGV1 SCR encoding

6.5.5 Scenario 4

Trigger if a sequence of 2 events is carried out in an incorrect order. Event A must be followed by event B and event B must be followed by event A. 2 consecutive occurrences of event A without an intermediate

8.3.2.10 ATD Input Enable Register (ATDDIEN)

Module Base + 0x000C

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	1	1	1	1	1	1	1	1	1	1	IEN[5:0]					
W																
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-12. ATD Input Enable Register (ATDDIEN)

Read: Anytime

Write: Anytime

Table 8-19. ATDDIEN Field Descriptions

Field	Description
5–0 IEN[5:0]	**ATD Digital Input Enable on channel *x* (*x*= 5, 4, 3, 2, 1, 0)** — This bit controls the digital input buffer from the analog input pin (AN*x*) to the digital data register. 0 Disable digital input buffer to AN*x* pin 1 Enable digital input buffer on AN*x* pin. **Note:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

8.3.2.11 ATD Compare Higher Than Register (ATDCMPHT)

Writes to this register will abort current conversion sequence.

Read: Anytime

Write: Anytime

Module Base + 0x000E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	CMPHT[5:0]					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-13. ATD Compare Higher Than Register (ATDCMPHT)

Table 8-20. ATDCMPHT Field Descriptions

Field	Description
5–0 CMPHT[5:0]	**Compare Operation Higher Than Enable for conversion number *n* (*n*= 5, 4, 3, 2, 1, 0) of a Sequence (*n conversion number, NOT channel number!)*** — This bit selects the operator for comparison of conversion results. 0 If result of conversion *n* is **lower or same than** compare value in ATDDR*n*, this is flagged in ATDSTAT2 1 If result of conversion *n* is **higher than** compare value in ATDDR*n*, this is flagged in ATDSTAT2

Table 9-2. PWME Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7 PWME7	**Pulse Width Channel 7 Enable** 0 Pulse width channel 7 is disabled. 1 Pulse width channel 7 is enabled. The pulse modulated signal becomes available at PWM output bit 7 when its clock source begins its next cycle.
6 PWME6	**Pulse Width Channel 6 Enable** 0 Pulse width channel 6 is disabled. 1 Pulse width channel 6 is enabled. The pulse modulated signal becomes available at PWM output bit 6 when its clock source begins its next cycle. If CON67=1, then bit has no effect and PWM output line 6 is disabled.
5 PWME5	**Pulse Width Channel 5 Enable** 0 Pulse width channel 5 is disabled. 1 Pulse width channel 5 is enabled. The pulse modulated signal becomes available at PWM output bit 5 when its clock source begins its next cycle.
4 PWME4	**Pulse Width Channel 4 Enable** 0 Pulse width channel 4 is disabled. 1 Pulse width channel 4 is enabled. The pulse modulated signal becomes available at PWM, output bit 4 when its clock source begins its next cycle. If CON45 = 1, then bit has no effect and PWM output line 4 is disabled.
3 PWME3	**Pulse Width Channel 3 Enable** 0 Pulse width channel 3 is disabled. 1 Pulse width channel 3 is enabled. The pulse modulated signal becomes available at PWM, output bit 3 when its clock source begins its next cycle.
2 PWME2	**Pulse Width Channel 2 Enable** 0 Pulse width channel 2 is disabled. 1 Pulse width channel 2 is enabled. The pulse modulated signal becomes available at PWM, output bit 2 when its clock source begins its next cycle. If CON23 = 1, then bit has no effect and PWM output line 2 is disabled.
1 PWME1	**Pulse Width Channel 1 Enable** 0 Pulse width channel 1 is disabled. 1 Pulse width channel 1 is enabled. The pulse modulated signal becomes available at PWM, output bit 1 when its clock source begins its next cycle.
0 PWME0	**Pulse Width Channel 0 Enable** 0 Pulse width channel 0 is disabled. 1 Pulse width channel 0 is enabled. The pulse modulated signal becomes available at PWM, output bit 0 when its clock source begins its next cycle. If CON01 = 1, then bit has no effect and PWM output line 0 is disabled.

9.3.2.2 PWM Polarity Register (PWMPOL)

The starting polarity of each PWM channel waveform is determined by the associated PPOLx bit in the PWMPOL register. If the polarity bit is one, the PWM channel output is high at the beginning of the cycle and then goes low when the duty count is reached. Conversely, if the polarity bit is zero, the output starts low and then goes high when the duty count is reached.

9.3.2.6 PWM Control Register (PWMCTL)

The PWMCTL register provides for various control of the PWM module.

	7	6	5	4	3	2	1	0
R	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-8. PWM Control Register (PWMCTL)

Read: Anytime

Write: Anytime

There are up to four control bits for concatenation, each of which is used to concatenate a pair of PWM channels into one 16-bit channel. If the corresponding channels do not exist on a particular derivative, then writes to these bits have no effect and reads will return zeroes. When channels 6 and 7are concatenated, channel 6 registers become the high order bytes of the double byte channel. When channels 4 and 5 are concatenated, channel 4 registers become the high order bytes of the double byte channel. When channels 2 and 3 are concatenated, channel 2 registers become the high order bytes of the double byte channel. When channels 0 and 1 are concatenated, channel 0 registers become the high order bytes of the double byte channel.

See Section 9.4.2.7, “PWM 16-Bit Functions” for a more detailed description of the concatenation PWM Function.

NOTE

Change these bits only when both corresponding channels are disabled.

Table 9-10. PWMCTL Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7 CON67	**Concatenate Channels 6 and 7** 0 Channels 6 and 7 are separate 8-bit PWMs. 1 Channels 6 and 7 are concatenated to create one 16-bit PWM channel. Channel 6 becomes the high order byte and channel 7 becomes the low order byte. Channel 7 output pin is used as the output for this 16-bit PWM (bit 7 of port PWMP). Channel 7 clock select control-bit determines the clock source, channel 7 polarity bit determines the polarity, channel 7 enable bit enables the output and channel 7 center aligned enable bit determines the output mode.
6 CON45	**Concatenate Channels 4 and 5** 0 Channels 4 and 5 are separate 8-bit PWMs. 1 Channels 4 and 5 are concatenated to create one 16-bit PWM channel. Channel 4 becomes the high order byte and channel 5 becomes the low order byte. Channel 5 output pin is used as the output for this 16-bit PWM (bit 5 of port PWMP). Channel 5 clock select control-bit determines the clock source, channel 5 polarity bit determines the polarity, channel 5 enable bit enables the output and channel 5 center aligned enable bit determines the output mode.

NOTE

Care must be taken when expecting data from a master while the slave is in wait or stop mode. Even though the shift register will continue to operate, the rest of the SPI is shut down (i.e., a SPIF interrupt will **not** be generated until exiting stop or wait mode). Also, the byte from the shift register will not be copied into the SPIDR register until after the slave SPI has exited wait or stop mode. In slave mode, a received byte pending in the receive shift register will be lost when entering wait or stop mode. An SPIF flag and SPIDR copy is generated only if wait mode is entered or exited during a tranmission. If the slave enters wait mode in idle mode and exits wait mode in idle mode, neither a SPIF nor a SPIDR copy will occur.

11.4.7.3 SPI in Stop Mode

Stop mode is dependent on the system. The SPI enters stop mode when the module clock is disabled (held high or low). If the SPI is in master mode and exchanging data when the CPU enters stop mode, the transmission is frozen until the CPU exits stop mode. After stop, data to and from the external SPI is exchanged correctly. In slave mode, the SPI will stay synchronized with the master.

The stop mode is not dependent on the SPISWAI bit.

11.4.7.4 Reset

The reset values of registers and signals are described in Section 11.3, “Memory Map and Register Definition”, which details the registers and their bit fields.

- If a data transmission occurs in slave mode after reset without a write to SPIDR, it will transmit garbage, or the data last received from the master before the reset.
- Reading from the SPIDR after reset will always read zeros.

11.4.7.5 Interrupts

The SPI only originates interrupt requests when SPI is enabled (SPE bit in SPICR1 set). The following is a description of how the SPI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt priority are chip dependent.

The interrupt flags MODF, SPIF, and SPTEF are logically ORed to generate an interrupt request.

11.4.7.5.1 MODF

MODF occurs when the master detects an error on the $\overline{SS}$ pin. The master SPI must be configured for the MODF feature (see Table 11-3). After MODF is set, the current transfer is aborted and the following bit is changed:

- MSTR = 0, The master bit in SPICR1 resets.

The MODF interrupt is reflected in the status register MODF flag. Clearing the flag will also clear the interrupt. This interrupt will stay active while the MODF flag is set. MODF has an automatic clearing process which is described in Section 11.3.2.4, “SPI Status Register (SPISR)”.

resistor of 1 kΩ must be placed in parallel between VLINSUP and the LIN Bus pin, with a diode between VLINSUP and the resistor. The fall time from recessive to dominant and the rise time from dominant to recessive is selectable and controlled to guarantee communication quality and reduce EMC emissions. The symmetry between both slopes is guaranteed.

16.1.2 Modes of Operation

The LIN Physical Layer can operate in the following four modes:

1. **Shutdown Mode**

   The LIN Physical Layer is fully disabled. No wake-up functionality is available. The internal pullup resistor is replaced by a high ohmic one (330 kΩ) to maintain the LIN Bus pin in the recessive state. All registers are accessible.

2. **Normal Mode**

   The full functionality is available. Both receiver and transmitter are enabled.

3. **Receive Only Mode**

   The transmitter is disabled and the receiver is running in full performance mode.

4. **Standby Mode**

   The transmitter of the LIN Physical Layer is disabled. If the wake-up feature is enabled, the internal pullup resistor can be selected (330 kΩ or 34 kΩ). The receiver enters a low power mode and optionally it can pass wake-up events to the Serial Communication Interface (SCI). If the wake-up feature is enabled and if the LIN Bus pin is driven with a dominant level longer than t_{WUFR} followed by a rising edge, the LIN Physical Layer sends a wake-up pulse to the SCI, which requests a wake-up interrupt. (This feature is only available if the LIN Physical Layer is routed to the SCI).

16.1.3 Block Diagram

Figure 16-1 shows the block diagram of the LIN Physical Layer. The module consists of a receiver with wake-up control, a transmitter with slope and timeout control, a current sensor with overcurrent protection as well as a registers control block.

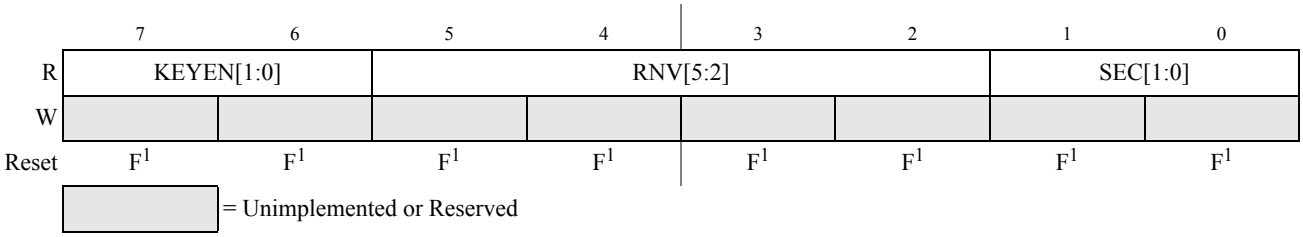


Figure 18-5. Flash Security Register (FSEC)

1 Loaded from IFR Flash configuration field, during reset sequence.

All bits in the FSEC register are readable but not writable.

During the reset sequence, the FSEC register is loaded with the contents of the Flash security byte in the Flash configuration field at global address 0x3_FF0F located in P-Flash memory (see Table 18-4) as indicated by reset condition F in Figure 18-5. If a double bit fault is detected while reading the P-Flash phrase containing the Flash security byte during the reset sequence, all bits in the FSEC register will be set to leave the Flash module in a secured state with backdoor key access disabled.

Table 18-9. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	**Backdoor Key Security Enable Bits** — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 18-10.
5–2 RNV[5:2]	**Reserved Nonvolatile Bits** — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	**Flash Security Bits** — The SEC[1:0] bits define the security state of the MCU as shown in Table 18-11. If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 18-10. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED[1]
10	ENABLED
11	DISABLED

1 Preferred KEYEN state to disable backdoor key access.

Table 18-11. Flash Security States

SEC[1:0]	Status of Security
00	SECURED
01	SECURED[1]
10	UNSECURED
11	SECURED

1 Preferred SEC state to set MCU to secured state.

The security function in the Flash module is described in Section 18.5 Security.

Address & Name		7	6	5	4	3	2	1	0
FRSV0	R	0	0	0	0	0	0	0	0
	W								
FCNFG	R	CCIE	0	0	IGNSF	0	0	FDFD	FSFD
	W								
FERCNFG	R	0	0	0	0	0	0	DFDIE	SFDIE
	W								
FSTAT	R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT1	MGSTAT0
	W								
FERSTAT	R	0	0	0	0	0	0	DFDIF	SFDIF
	W								
FPROT	R	FPOPEN	RNV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
	W								
EEPROT	R	DPOPEN	0	0	0	0	0	DPS1	DPS0
	W								
FCCOBHI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
FCCOBLO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
FRSV1	R	0	0	0	0	0	0	0	0
	W								
FRSV2	R	0	0	0	0	0	0	0	0
	W								
FRSV3	R	0	0	0	0	0	0	0	0
	W								
FRSV4	R	0	0	0	0	0	0	0	0
	W								
FOPT	R	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
	W								

Figure 19-4. FTMRG32K128 Register Summary (continued)

Table 19-36. Erase Verify P-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x03	Global address [17:16] of a P-Flash block
001	Global address [15:0] of the first phrase to be verified	
010	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 19-37. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 19-27)
		Set if an invalid global address [17:0] is supplied see Table 19-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
		Set if the requested section crosses a the P-Flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

19.4.6.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash. The Read Once field is programmed using the Program Once command described in Section 19.4.6.6 Program Once Command. The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 19-38. Read Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x04	Not Required
001	Read Once phrase index (0x0000 - 0x0007)	
010	Read Once word 0 value	
011	Read Once word 1 value	
100	Read Once word 2 value	
101	Read Once word 3 value	

A.1.5 Operating Conditions

This section describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE

Please refer to the temperature rating of the device with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation calculations refer to Section A.1.6, "Power Dissipation and Thermal Characteristics".

Table A-5. Operating Conditions

Num	Rating	Symbol	Min	Typ	Max	Unit
1	Voltage regulator and LINPHY supply voltage	V_{SUP}/ V_{LINUP}	3.5	12	40[1]	V
2	High side driver supply voltage	V_{SUPHS}	7	12	40[1]	V
3	Voltage difference V_{DDX} to V_{DDA}	Δ_{VDDX}	-0.1	—	0.1	V
4	Voltage difference V_{SSX} to V_{SSA}	Δ_{VSSX}	-0.1	—	0.1	V
5	Oscillator	f_{osc}	4	—	20	MHz
6	Bus frequency	f_{bus}	see Footnote[2]	—	25	MHz
7	Operating junction temperature range Operating ambient temperature range[3]	T_J T_A	–40 –40	— —	150 125	°C

1 Normal operating range is 6V - 18V. Continous operation at 40V is not allowed. Only Transient Conditions (Load Dump) single pulse t_{max}<400ms

2 Minimum bus frequency for ADC module refer to Table C-1., "ATD Operating Characteristics and for Flash Module refer to Table M-1., "NVM Timing Characteristics

3 Please refer to Section A.1.6, "Power Dissipation and Thermal Characteristics" for more details about the relation between ambient temperature T_A and device junction temperature T_J.

NOTE

Operation is guaranteed when powering down until low voltage reset assertion.

A.1.6 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

J.2 Pin Interrupt Characteristics

Table J-3. Pin Interrupt Characteristics

Characteristics are 5.5V ≤ VSUP ≤ 18 V, -40°C ≤ T_J ≤ 150°C[1] junction temperature from –40°C to +150°C unless otherwise noted.						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Port L, P, AD interrupt input pulse filtered (STOP)[2]	t_{P_MASK}	—	—	3	µs
2	Port L, P, AD interrupt input pulse passed (STOP)[2]	t_{P_PASS}	10	—	—	µs
3	Port L, P, AD interrupt input pulse filtered ($\overline{STOP}$) in number of bus clock cycles of period $1/f_{bus}$	n_{P_MASK}	—	—	3	
4	Port L, P, AD interrupt input pulse passed ($\overline{STOP}$) in number of bus clock cycles of period $1/f_{bus}$	n_{P_PASS}	4	—	—	
5	$\overline{IRQ}$ pulse width, edge-sensitive mode ($\overline{STOP}$) in number of bus clock cycles of period $1/f_{bus}$	n_{IRQ}	1	—	—	

1 T_J: Junction Temperature

2 Parameter only applies in stop or pseudo stop mode.

P.9 0x0020-0x002F Debug Module (S12SDBG) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x002B	DBGXAL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002C	DBGADH	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002D	DBGADL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002E	DBGADHM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002F	DBGADLM	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

1 This represents the contents if the Comparator A or C control register is blended into this address

2 This represents the contents if the Comparator B or D control register is blended into this address

3 This represents the contents if the Comparator B or D control register is blended into this address

P.10 0x0030-0x0033 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0030	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0031	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0032	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0033	Reserved	R	0	0	0	0	0	0	0	0
		W								

P.11 0x0034-0x003F Clock Reset and Power Management (CPMU) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0034	CPMUSYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0035	CPMUREFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0036	CPMUPOSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0037	CPMUFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	OSCIF	UPOSC
		W								
0x0038	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	**PMRF**[1]
		W								
0x0039	CPMUCLKS	R	PLLSEL	PSTP	0	COPOSCSEL1	PRE	PCE	RTIOSCSEL	COPOSCSEL0
		W								