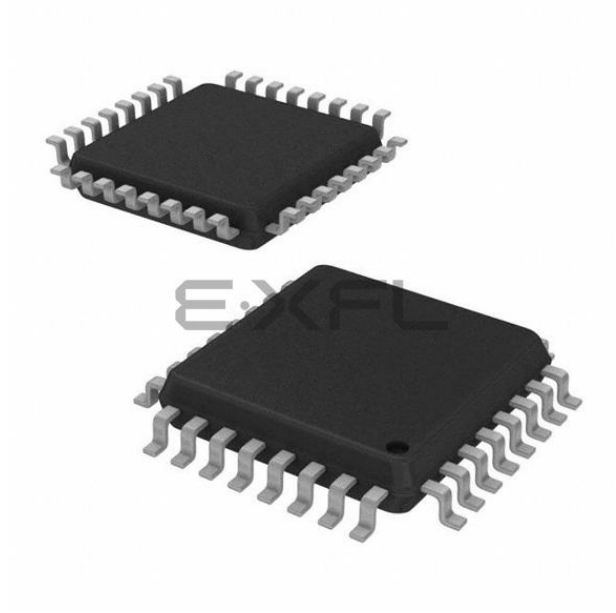

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vr16f0vlcr

— Optional HVI to ADC link

A standard port pin has the following minimum features:

- Input/output selection
- 5 V output drive
- 5 V digital and analog input
- Input with selectable pullup or pulldown device

Optional features supported on dedicated pins:

- Two selectable output drive strengths
- Open drain for wired-or connections
- Interrupt input with glitch filtering
- High-voltage input
- 10 mA high-current output
- 20 mA high-current output with over-current protection for use as Hall sensor supply

2.2 External Signal Description

This section lists and describes the signals that do connect off-chip.

Table 2-2 shows all the pins and their functions that are controlled by the PIM. Routing options are denoted in parenthesis.

NOTE

If there is more than one function associated with a pin, the **output** priority is indicated by the position in the table from top (highest priority) to bottom (lowest priority).

Table 2-2. Pin Functions and Priorities[1]

Port	Pin Name	Pin Function & Priority[1]	I/O	Description	Pin Function after Reset
-	BKGD	MODC[2]	I	MODC input during $\overline{\text{RESET}}$	BKGD
		BKGD	I/O	BDM communication pin	
E	PE1	XTAL	-	CPMU OSC signal	GPIO
		PTE[1]	I/O	General-purpose	
	PE0	EXTAL	-	CPMU OSC signal	
		PTE[0]	I/O	General-purpose	

Port	Pin Name	Pin Function & Priority[1]	I/O	Description	Pin Function after Reset
P	**PP5**	**$\overline{\text{IRQ}}$**	**I**	**Maskable level- or falling edge-sensitive interrupt**	GPIO
		PWM5	**O**	**Pulse Width Modulator channel 5**	
		ETRIG1	**I**	**ADC external trigger input**	
		PTP[5]/ KWP[5]	**I/O**	**General-purpose; with pin interrupt and wakeup**	
	PP4	**PWM4**	**O**	**Pulse Width Modulator channel 4**	
		ETRIG0	**I**	**ADC external trigger input**	
		PTP[4]/ KWP[4]	**I/O**	**General-purpose; with pin interrupt and wakeup**	
	PP3	**PWM3**	**O**	**Pulse Width Modulator channel 3**	
		PTP[3]/ KWP[3]	**I/O**	**General-purpose; with pin interrupt and wakeup**	
	PP2[3]	PWM2	O	Pulse Width Modulator channel 2	
		PTP[2]/ KWP[2]/ EVDD	I/O	General-purpose; with pin interrupt and wakeup	
	PP1[4]	$\overline{\text{XIRQ}}$	I	Non-maskable level-sensitive interrupt	
		PWM1	O	Pulse Width Modulator channel 1	
		PTP[1]/ KWP[1]	I/O	General-purpose; with interrupt and wakeup	
	PP0[4]	**PWM0**	**O**	**Pulse Width Modulator channel 0**	
		PTP[0]/ KWP[0]	**I/O**	**General-purpose; with interrupt and wakeup**	
L	PL3-0	PTL[3:0]/ KWL[3:0]	I	General-purpose high-voltage input (HVI); with interrupt and wakeup; optional ADC link	GPI (HVI)
AD	**PAD5-2**	**AN[5:2]**	**I**	**ADC analog**	GPIO
		PTAD[5:2]/ KWAD[5:2]	**I/O**	**General-purpose; with interrupt and wakeup**	
	PAD1-0	AN[1:0]	I	ADC analog	
		PTAD[1:0]/ KWAD[1:0]	I/O	General-purpose; with interrupt and wakeup	

1 Signals in parentheses denote alternative module routing pins. Signals in **bold underlined** are only available on S12VR64/48.

2 Function active when $\overline{\text{RESET}}$ asserted

3 High current capable high-side output (20mA) with over-current interrupt and protection for all sources (see 2.4.4.3/2-112)

4 High-current capable output (10 mA)

2.3 Memory Map and Register Definition

This section provides a detailed description of all PIM registers.

Table 2-10. PTT Register Field Descriptions (continued)

Field	Description
1 PTT	**PorT data register port T** — General-purpose input/output data, TIM input/output, routed SCI0, LPDR[LPDR1] When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read. • The routed SCI0 or LPDR[LPDR1] takes precedence over the TIM output function and the general-purpose I/O function if enabled. • The TIM function takes precedence over the general-purpose I/O function if enabled.
0 PTT	**PorT data register port T** — General-purpose input/output data, TIM input/output, routed SCI0 When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read. • The routed SCI0 takes precedence over the TIM output function and the general-purpose I/O function if enabled. • The TIM function takes precedence over the general-purpose I/O function if enabled.

2.3.12 Port T Input Register (PTIT)

Address 0x0241 Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PTIT3	PTIT2	PTIT1	PTIT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-10. Port T Input Register (PTIT)

[1] Read: Anytime
Write:Never

Table 2-11. PTIT Register Field Descriptions

Field	Description
3-0 PTIT	**PorT Input data register port T** — A read always returns the synchronized input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.3.13 Port T Data Direction Register (DDRT)

Address 0x0242 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	DDRT3	DDRT2	DDRT1	DDRT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-11. Port T Data Direction Register (DDRT)

Table 2-19. DDRS Register Field Descriptions (continued)

Field	Description
2 DDRS	**Data Direction Register port S —** This bit determines whether the associated pin is an input or output. The enabled API_EXTCLK function forces the I/O state to output. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. The routed SCI1 function forces the I/O state to input if enabled. The routed PWM function forces the I/O state to output if enabled. In these cases the data direction bit will not change. The routed ETRIG function has no effect on the I/O state. 1 Associated pin is configured as output 0 Associated pin is configured as input
1 DDRS	**Data Direction Register port S —** This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SCI the I/O state will be forced to be input or output. The enabled routed LINPHY forces the I/O state to be an output (LPDR[LPDR1]). In these cases the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
0 DDRS	**Data Direction Register port S —** This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SCI the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input

2.3.22 Port S Pull Device Enable Register (PERS)

Address 0x024C (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
W								
Reset	0	0	1	1	1	1	1	1

Figure 2-24. Port S Pull Device Enable Register (PERS - S12VR64/48)

1 Read: Anytime
Write: Anytime

Address 0x024C (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PERS3	PERS2	0	0
W								
Reset	0	0	0	0	1	1	0	0

Figure 2-25. Port S Pull Device Enable Register (PERS - S12VR32/16)

1 Read: Anytime
Write: Anytime

Table 4-6. CPMUCLKS Descriptions (continued)

Field	Description
1 RTIOSCSEL	**RTI Clock Select**— RTIOSCSEL selects the clock source to the RTI. Either IRCCLK or OSCCLK. Changing the RTIOSCSEL bit re-starts the RTI time-out period. RTIOSCSEL can only be set to 1, if UPOSC=1. UPOSC= 0 clears the RTIOSCSEL bit. 0 RTI clock source is IRCCLK. 1 RTI clock source is OSCCLK.
0 COP OSCSEL0	**COP Clock Select 0** — COPOSCSEL0 and COPOSCSEL1 combined determine the clock source to the COP (see also Table 4-7) If COPOSCSEL1 = 1, COPOSCSEL0 has no effect regarding clock select and changing the COPOSCSEL0 bit does not re-start the COP time-out period. When COPOSCSEL1=0,COPOSCSEL0 selects the clock source to the COP to be either IRCCLK or OSCCLK. Changing the COPOSCSEL0 bit re-starts the COP time-out period. COPOSCSEL0 can only be set to 1, if UPOSC=1. UPOSC= 0 clears the COPOSCSEL0 bit. 0 COP clock source is IRCCLK. 1 COP clock source is OSCCLK

Table 4-7. COPOSCSEL1, COPOSCSEL0 clock source select description

COPOSCSEL1	COPOSCSEL0	COP clock source
0	0	IRCCLK
0	1	OSCCLK
1	x	ACLK

Write: All modes through BDM operation when not secured

NOTE

When BDM is made active, the CPU stores the content of its CCR register in the BDMCCR register. However, out of special single-chip reset, the BDMCCR is set to 0xD8 and not 0xD0 which is the reset value of the CCR register in this CPU mode. Out of reset in all other modes the BDMCCR register is read zero.

When entering background debug mode, the BDM CCR holding register is used to save the condition code register of the user's program. It is also used for temporary storage in the standard BDM firmware mode. The BDM CCR holding register can be written to modify the CCR value.

5.3.2.2 BDM Program Page Index Register (BDMPPR)

Register Global Address 0x3_FF08

	7	6	5	4	3	2	1	0
R	BPAE	0	0	0	BPP3	BPP2	BPP1	BPP0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented, Reserved

Figure 5-5. BDM Program Page Register (BDMPPR)

Read: All modes through BDM operation when not secured

Write: All modes through BDM operation when not secured

Table 5-4. BDMPPR Field Descriptions

Field	Description
7 BPAE	**BDM Program Page Access Enable Bit** — BPAE enables program page access for BDM hardware and firmware read/write instructions The BDM hardware commands used to access the BDM registers (READ_BD and WRITE_BD) can not be used for program page accesses even if the BPAE bit is set. 0 BDM Program Paging disabled 1 BDM Program Paging enabled
3–0 BPP[3:0]	**BDM Program Page Index Bits 3–0** — These bits define the selected program page. For more detailed information regarding the program page window scheme, please refer to the device MMC description.

5.3.3 Family ID Assignment

The family ID is an 8-bit value located in the BDM ROM in active BDM (at global address: 0x3_FF0F). The read-only value is a unique family ID which is 0xC2 for devices with an HCS12S core.

5.4 Functional Description

The BDM receives and executes commands from a host via a single wire serial interface. There are two types of BDM commands: hardware and firmware commands.

If an interrupt is pending when a TRACE1 command is issued, the interrupt stacking operation occurs but no user instruction is executed. Once back in standard BDM firmware execution, the program counter points to the first instruction in the interrupt service routine.

Be aware when tracing through the user code that the execution of the user code is done step by step but all peripherals are free running. Hence possible timing relations between CPU code execution and occurrence of events of other peripherals no longer exist.

Do not trace the CPU instruction BGND used for soft breakpoints. Tracing over the BGND instruction will result in a return address pointing to BDM firmware address space.

When tracing through user code which contains stop or wait instructions the following will happen when the stop or wait instruction is traced:

The CPU enters stop or wait mode and the TRACE1 command can not be finished before leaving the low power mode. This is the case because BDM active mode can not be entered after CPU executed the stop instruction. However all BDM hardware commands except the BACKGROUND command are operational after tracing a stop or wait instruction and still being in stop or wait mode. If system stop mode is entered (all bus masters are in stop mode) no BDM command is operational.

As soon as stop or wait mode is exited the CPU enters BDM active mode and the saved PC value points to the entry of the corresponding interrupt service routine.

In case the handshake feature is enabled the corresponding ACK pulse of the TRACE1 command will be discarded when tracing a stop or wait instruction. Hence there is no ACK pulse when BDM active mode is entered as part of the TRACE1 command after CPU exited from stop or wait mode. All valid commands sent during CPU being in stop or wait mode or after CPU exited from stop or wait mode will have an ACK pulse. The handshake feature becomes disabled only when system stop mode has been reached. Hence after a system stop mode the handshake feature must be enabled again by sending the ACK_ENABLE command.

5.4.11 Serial Communication Time Out

The host initiates a host-to-target serial transmission by generating a falling edge on the BKGD pin. If BKGD is kept low for more than 128 target clock cycles, the target understands that a SYNC command was issued. In this case, the target will keep waiting for a rising edge on BKGD in order to answer the SYNC request pulse. If the rising edge is not detected, the target will keep waiting forever without any time-out limit.

Consider now the case where the host returns BKGD to logic one before 128 cycles. This is interpreted as a valid bit transmission, and not as a SYNC request. The target will keep waiting for another falling edge marking the start of a new bit. If, however, a new falling edge is not detected by the target within 512 clock cycles since the last falling edge, a time-out occurs and the current command is discarded without affecting memory or the operating mode of the MCU. This is referred to as a soft-reset.

If a read command is issued but the data is not retrieved within 512 serial clock cycles, a soft-reset will occur causing the command to be disregarded. The data is not available for retrieval after the time-out has occurred. This is the expected behavior if the handshake protocol is not enabled. In order to allow the data to be retrieved even with a large clock frequency mismatch (between BDM and CPU) when the hardware

6.3.2.7.1 Debug State Control Register 1 (DBGSCR1)

Address: 0x0027

	7	6	5	4	3	2	1	0
R	0	0	0	0	SC3	SC2	SC1	SC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-9. Debug State Control Register 1 (DBGSCR1)

Read: If COMRV[1:0] = 00

Write: If COMRV[1:0] = 00 and DBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 00. The state control register 1 selects the targeted next state whilst in State1. The matches refer to the match channels of the comparator match control logic as depicted in Figure 6-1 and described in Section 6.3.2.8.1, “Debug Comparator Control Register (DBGXCTL). Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 6-15. DBGSCR1 Field Descriptions

Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State1, based upon the match event.

Table 6-16. State1 Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0000	Any match to Final State
0001	Match1 to State3
0010	Match2 to State2
0011	Match1 to State2
0100	Match0 to State2..... Match1 to State3
0101	Match1 to State3.....Match0 to Final State
0110	Match0 to State2..... Match2 to State3
0111	Either Match0 or Match1 to State2
1000	Reserved
1001	Match0 to State3
1010	Reserved
1011	Reserved
1100	Reserved
1101	Either Match0 or Match2 to Final State.....Match1 to State2
1110	Reserved
1111	Reserved

The priorities described in Table 6-36 dictate that in the case of simultaneous matches, a match leading to final state has priority followed by the match on the lower channel number (0,1,2). Thus with SC[3:0]=1101 a simultaneous match0/match1 transitions to final state.

9.3.2.6 PWM Control Register (PWMCTL)

The PWMCTL register provides for various control of the PWM module.

	7	6	5	4	3	2	1	0
R	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-8. PWM Control Register (PWMCTL)

Read: Anytime

Write: Anytime

There are up to four control bits for concatenation, each of which is used to concatenate a pair of PWM channels into one 16-bit channel. If the corresponding channels do not exist on a particular derivative, then writes to these bits have no effect and reads will return zeroes. When channels 6 and 7are concatenated, channel 6 registers become the high order bytes of the double byte channel. When channels 4 and 5 are concatenated, channel 4 registers become the high order bytes of the double byte channel. When channels 2 and 3 are concatenated, channel 2 registers become the high order bytes of the double byte channel. When channels 0 and 1 are concatenated, channel 0 registers become the high order bytes of the double byte channel.

See Section 9.4.2.7, “PWM 16-Bit Functions” for a more detailed description of the concatenation PWM Function.

NOTE

Change these bits only when both corresponding channels are disabled.

Table 9-10. PWMCTL Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7 CON67	**Concatenate Channels 6 and 7** 0 Channels 6 and 7 are separate 8-bit PWMs. 1 Channels 6 and 7 are concatenated to create one 16-bit PWM channel. Channel 6 becomes the high order byte and channel 7 becomes the low order byte. Channel 7 output pin is used as the output for this 16-bit PWM (bit 7 of port PWMP). Channel 7 clock select control-bit determines the clock source, channel 7 polarity bit determines the polarity, channel 7 enable bit enables the output and channel 7 center aligned enable bit determines the output mode.
6 CON45	**Concatenate Channels 4 and 5** 0 Channels 4 and 5 are separate 8-bit PWMs. 1 Channels 4 and 5 are concatenated to create one 16-bit PWM channel. Channel 4 becomes the high order byte and channel 5 becomes the low order byte. Channel 5 output pin is used as the output for this 16-bit PWM (bit 5 of port PWMP). Channel 5 clock select control-bit determines the clock source, channel 5 polarity bit determines the polarity, channel 5 enable bit enables the output and channel 5 center aligned enable bit determines the output mode.

12.3.2.3 Timer Count Register (TCNT)

	15	14	13	12	11	10	9	9
R W	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
Reset	0	0	0	0	0	0	0	0

Figure 12-6. Timer Count Register High (TCNTH)

	7	6	5	4	3	2	1	0
R W	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
Reset	0	0	0	0	0	0	0	0

Figure 12-7. Timer Count Register Low (TCNTL)

The 16-bit main timer is an up counter.

A full access for the counter register should take place in one clock cycle. A separate read/write for high byte and low byte will give a different result than accessing them as a word.

Read: Anytime

Write: Has no meaning or effect in the normal mode; only writable in special modes .

The period of the first count after a write to the TCNT registers may be a different size because the write is not synchronized with the prescaler clock.

12.3.2.4 Timer System Control Register 1 (TSCR1)

	7	6	5	4	3	2	1	0
R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 12-8. Timer System Control Register 1 (TSCR1)

Read: Anytime

Write: Anytime

12.3.2.13 Output Compare Pin Disconnect Register(OCPD)

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	OCPD3	OCPD2	OCPD1	OCPD0
Reset	0	0	0	0	0	0	0	0

Figure 12-20. Output Compare Pin Disconnect Register (OCPD)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 12-15. OCPD Field Description

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 OCPD[3:0]	**Output Compare Pin Disconnect Bits** 0 Enables the timer channel port. Output Compare action will occur on the channel pin. These bits do not affect the input capture . 1 Disables the timer channel port. Output Compare action will not occur on the channel pin, but the output compare flag still become set.

12.3.2.14 Precision Timer Prescaler Select Register (PTPSR)

	7	6	5	4	3	2	1	0
R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
Reset	0	0	0	0	0	0	0	0

Figure 12-21. Precision Timer Prescaler Select Register (PTPSR)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 12-16. PTPSR Field Descriptions

Field	Description
7:0 PTPS[7:0]	**Precision Timer Prescaler Select Bits** — These eight bits specify the division rate of the main Timer prescaler. These are effective only when the PRNT bit of TSCR1 is set to 1. Table 12-17 shows some selection examples in this case. The newly selected prescale factor will not take effect until the next synchronized edge where all prescale counter stages equal zero.

The Prescaler can be calculated as follows depending on logical value of the PTPS[7:0] and PRNT bit:

PRNT = 1 : Prescaler = PTPS[7:0] + 1

NOTE

The open-load detection is only active if the selected source (e.g. PWM, Timer, HSDR[HSDR0]) for the high-side driver is turned off.

14.4.3 Over-Current Shutdown

The high-side driver has an over-current shutdown feature with a current threshold of I_{OCTHSX}.

If an over-current is detected the interrupt flag is set in the HSDRV Interrupt Flag Register (HSIF). As long as the over-current interrupt flag remains set, the high-side driver is turned off to protect the circuit.

Clearing the related over-current interrupt flag returns back the control to the selected source in the PIM module.The over-current detection and driver shutdown can be masked for an initial T_{HSOCM} after switching the driver on. This can be achieved by setting the HSCR[HSOCME0] register bit. HSCR[HSOCME0] is only writable while the driver is disabled (HSCR[HSE0]=0).

14.4.4 Interrupts

This section describes the interrupt generated by HSDRV1C module. The interrupt is only available in MCU run mode. Entering and exiting MCU stop mode has no effect on the interrupt flags.

The interrupt generated by HSDRV1C module is shown in Table 14-11. Vector addresses and interrupt priorities are defined at MCU level.

14.4.4.1 HSDRV1C Over Current Interrupt (HSOCI)

Table 14-11. HSDRV1C Interrupt Sources

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
HSDRV1C Interrupt (HSI)	HSDRV1C Over-Current Interrupt (HSOCI)	HSOCIE = 1

If an over-current is detected the related interrupt flag HSOCIFx asserts. Depending on the setting of the HSDRV1C Error Interrupt Enable (HSOCIE) bit an interrupt is requested.

15.4 Functional Description

15.4.1 General

The LSDRV module provides two low-side drivers able to drive inductive loads (relays). The driver can be controlled directly through register bits or alternatively by dedicated timer or PWM channels. See PIM section for routing details.

Both drivers feature an open-load and over-current detection described in the following sub-sections. In addition to this an active clamp (for driving relays) is protecting each driver stage. The active clamp will turn on a low-side FET if the voltage on a pin exceeds V_{CLAMP} when the driver is turned off.

15.4.2 Open-Load Detection

A “High-load resistance Open Load Detection” can be enabled for each driver by setting the corresponding LSOLEx bit (refer to Section 15.3.4, “LSDRV Configuration Register (LSCR)”. This detection will only be executed when the driver is enabled and it is not being driven (LSDRx = 0). That is because the measurement point is between the load and the driver, and the current should not go through the driver. To detect an open-load condition the voltage will be observed at the output from the driver. Then if the driving pin LSx stays at low voltage which is approximately LSGND, there is no load for the corresponding low-side driver.

An open-load condition is flagged with bits LSOL0 and LSOL1 in the LSDRV Status Register (LSSR).

15.4.3 Over-Current Detection

Each low-side driver has an over-current detection while enabled with a current threshold of I_{LIMLSX}.

If over-current is detected the related interrupt flag (LSOCIF1 or LSOCIF0) is set in the LSDRV Interrupt Flag Register (LSIF). As long as the over-current interrupt flag remains set the related low-side driver is turned off to protect the circuit.Clearing the related over-current interrupt flag returns back the control of the driver to the selected source in the PIM module.

NOTE

The open-load detection is only active if the selected source (e.g. PWM, Timer, LSDRx) for the low-side driver is turned off.

15.4.4 Interrupts

This section describes the interrupt generated by LSDRV module. The interrupt is only available in MCU run mode. Entering and exiting MCU stop mode has no effect on the interrupt flags.

The LSDRV interrupt vector is named in Table 15-9. Vector addresses and interrupt priorities are defined at MCU level.

If LPWUE is set the receiver is able to pass wake-up events to the SCI (Serial Communication Interface). If the LIN Physical Layer receives a dominant level longer than t_{WUFR} followed by a rising edge, it sends a pulse to the SCI which can generate a wake-up interrupt.

Once the device exits stop mode, the LIN Physical Layer returns to normal or receive only mode depending on the status of the RXONLY bit.

NOTE

Since the wake-up interrupt is requested by the SCI, the wake-up feature is not available if the SCI is not used.

The internal pullup resistor is selectable only if LPWUE = 1 (wake-up enabled). If LPWUE = 0, the internal pullup resistor is not selectable and remains at 330 kΩ regardless of the state of the LPPUE bit.

If LPWUE = 1, selecting the 330 kΩ pullup resistor (LPPUE = 0) reduces the current consumption in standby mode.

NOTE

When using the LIN wake-up feature in combination with other non-LIN device wake-up features (like a periodic time interrupt), some care must be taken.

If the device leaves stop mode while the LIN bus is dominant, the LIN Physical Layer returns to normal or receive only mode and the LIN bus is re-routed to the RXD pin of the SCI and triggers the edge detection interrupt (if the interrupt's priority of the hardware that awakes the MCU is less than the priority of the SCI interrupt, then the SCI interrupt will execute first). It is up to the software to decide what to do in this case because the LIN Physical Layer can not guarantee it was a valid wake-up pulse.

Table 18-41. Program P-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 18-27)
		Set if an invalid global address [17:0] is supplied see)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the global address [17:0] points to a protected area
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

18.4.6.6 Program Once Command

The Program Once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in P-Flash. The Program Once reserved field can be read using the Read Once command as described in Section 18.4.6.4 Read Once Command. The Program Once command must only be issued once since the nonvolatile information register in P-Flash cannot be erased. The Program Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 18-42. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x07	Not Required
001	Program Once phrase index (0x0000 - 0x0007)	
010	Program Once word 0 value	
011	Program Once word 1 value	
100	Program Once word 2 value	
101	Program Once word 3 value	

Upon clearing CCIF to launch the Program Once command, the Memory Controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The CCIF flag will remain clear, setting only after the Program Once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash will return invalid data.

Table 18-46. Erase Flash Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x09	Global address [17:16] to identify Flash block
001	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table 18-47. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 18-27)
		Set if an invalid global address [17:16] is supplied
		Set if the supplied P-Flash address is not phrase-aligned or if the EEPROM address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

18.4.6.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 18-48. Erase P-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0A	Global address [17:16] to identify P-Flash block to be erased
001	Global address [15:0] anywhere within the sector to be erased. Refer to Section 18.1.2.1 P-Flash Features for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

Table 19-52. Verify Backdoor Access Key Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0C	Not required
001	Key 0	
010	Key 1	
011	Key 2	
100	Key 3	

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0x3_FF00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 19-53. Verify Backdoor Access Key Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 100 at command launch
		Set if an incorrect backdoor key is supplied
		Set if backdoor key access has not been enabled (KEYEN[1:0] != 10, see Section 19.3.2.2 Flash Security Register (FSEC))
		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

19.4.6.12 Set User Margin Level Command

The Set User Margin Level command causes the Memory Controller to set the margin level for future read operations of the P-Flash or EEPROM block.

Table 19-54. Set User Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0D	Flash block selection code [1:0]. See Table 19-34
001	Margin level setting.	

Upon clearing CCIF to launch the Set User Margin Level command, the Memory Controller will set the user margin level for the targeted block and then set the CCIF flag.

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.

3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70029A	REV: D
LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	CASE NUMBER: 873A-03	19 MAY 2005
	STANDARD: JEDEC MS-026 BBA	

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	DOCUMENT NO: 98ASH00962A	REV: G
	CASE NUMBER: 932–03	14 APR 2005
	STANDARD: JEDEC MS–026–BBC	

P.31 0x0240 -0x027F Port Integration Module[1] (PIM) Map 4 of 4

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0260-0 x0268	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0269	PTIL	R	0	0	0	0	PTIL3	PTIL2	PTIL1	PTIL0
		W								
0x026A	DDRL	R	0	0	0	0	DDRL3	DDRL2	DDRL1	DDRL0
		W								
0x026B	PTAL	R	0	0	0	0	PTAENL	0	PTAL1	PTAL0
		W								
0x026C	PIRL	R	0	0	0	0	PIRL3	PIRL2	PIRL1	PIRL0
		W								
0x026D	PPSL	R	0	0	0	0	PPSL3	PPSL2	PPSL1	PPSL0
		W								
0x026E	PIEL	R	0	0	0	0	PIEL3	PIEL2	PIEL1	PIEL0
		W								
0x026F	PIFL	R	0	0	0	0	PIFL3	PIFL2	PIFL1	PIFL0
		W								
0x0270	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0271	PT1AD	R	0	0	**PT1AD5**	**PT1AD4**	**PT1AD3**	**PT1AD2**	PT1AD1	PT1AD0
		W								
0x0272	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0273	PTI1AD	R	0	0	**PTI1AD5**	**PTI1AD4**	**PTI1AD3**	**PTI1AD2**	PTI1AD1	PTI1AD0
		W								
0x0274	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0275	DDR1AD	R	0	0	**DDR1AD5**	**DDR1AD4**	**DDR1AD3**	**DDR1AD2**	DDR1AD1	DDR1AD0
		W								
0x0276-0 x0278	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0279	PER1AD	R	0	0	**PER1AD5**	**PER1AD4**	**PER1AD3**	**PER1AD2**	PER1AD1	PER1AD0
		W								
0x027A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x027B	PPS1AD	R	0	0	**PPS1AD5**	**PPS1AD4**	**PPS1AD3**	**PPS1AD2**	PPS1AD1	PPS1AD0
		W								
0x027C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x027D	PIE1AD	R	0	0	**PIE1AD5**	**PIE1AD4**	**PIE1AD3**	**PIE1AD2**	PIE1AD1	PIE1AD0
		W								
0x027E	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x027F	PIF1AD	R	0	0	**PIF1AD5**	**PIF1AD4**	**PIF1AD3**	**PIF1AD2**	PIF1AD1	PIF1AD0
		W								

[1] Register and register bits in **bold underlined** are only available on S12VR64/48. On S12VR32/16 these locations read 0 and write is not implemented.