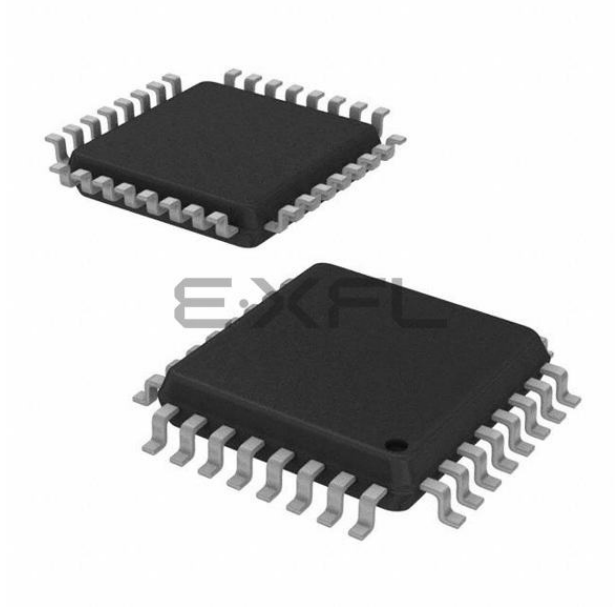

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vr32f0clc

Chapter 13
High-Side Drivers - HSDRV (S12HSDRVV2) for S12VR64

Chapter 14
High-Side Driver - HSDRV1C (HSDRV1CV3) for S12VR32

Chapter 19
32 KByte Flash Module (S12FTMRG32K128V1) for S12VR32

Appendix A
MCU Electrical Specifications

Appendix I
BATS Electrical Specifications

Appendix J
PIM Electrical Specifications

Appendix K
SPI Electrical Specifications for S12VR64

Appendix L
XOSCLCP Electrical Specifications

Appendix M
FTMRG Electrical Specifications

Appendix N
Package Information

Appendix O
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Appendix P
Detailed Register Address Map

1.4.13 Serial Communication Interface Module (SCI)

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 16-bit baud rate selection
- Programmable character length
- Programmable polarity for transmitter and receiver
- Active edge receive wake-up
- Break detect and transmit collision detect supporting LIN

1.4.14 Analog-to-Digital Converter Module (ATD)

- Up to 6-channel, 10-bit analog-to-digital converter
  - 8-/10-bit resolution
  - 3 us, 10-bit single conversion time
  - Left or right justified result data
  - Internal oscillator for conversion in stop modes
  - Continuous conversion mode
  - Multiple channel scans
- Pins can also be used as digital I/O
- Up to 6 pins can be used as keyboard wake-up interrupt (KWI)
- Internal voltages monitored with the ATD module
  - V_{SUP}, V_{SENSE}, chip temperature sensor, high voltage inputs,V_{RH}, V_{RL}, V_{DDF}

1.4.15 Supply Voltage Sense (BATS)

- VSENSE & VSUP pin low or a high voltage interrupt
- VSENSE & VSUP pin can be routed via an internal divider to the internal ADC

1.4.16 On-Chip Voltage Regulator system (VREG)

- Voltage regulator
  - Linear voltage regulator directly supplied by VSUP (protected VBAT)
  - Low-voltage detect with low-voltage interrupt on VSUP
  - Capable of supplying both the MCU internally and providing additional external current (approximately 20mA) to supply other components within the electronic control unit.
  - Over-temperature interrupt
- Internal Voltage regulator
  - Linear voltage regulator with bandgap reference
  - Low-voltage detect with low-voltage interrupt on VDDA

1.7.5 Pinout 48-pin LQFP

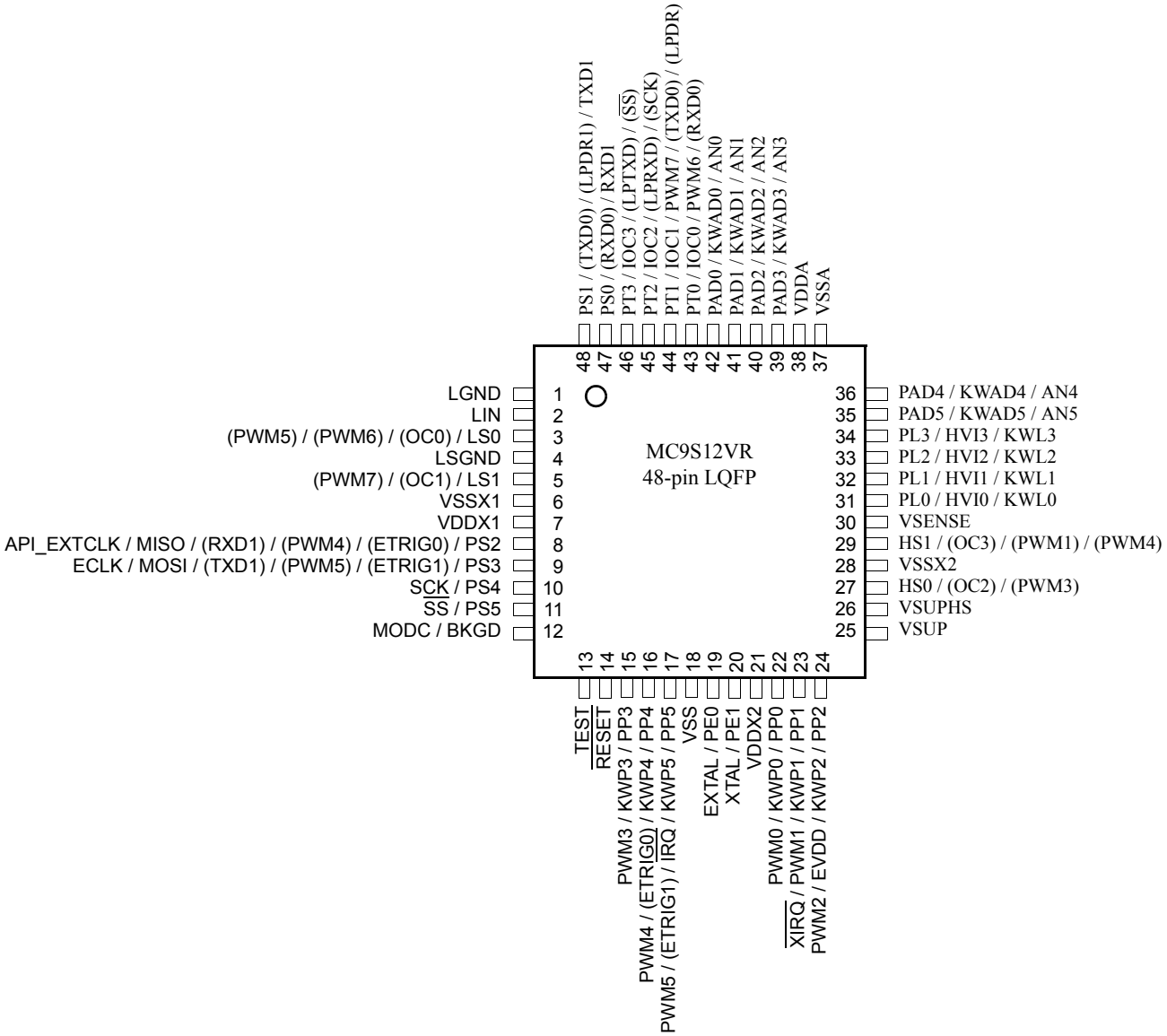

Figure 1-3. MC9S12VR 48-pin LQFP pinout

Table 2-9. IRQCR Register Field Descriptions

Field	Description
7 IRQE	**IRQ select Edge sensitive only** — 1 $\overline{\text{IRQ}}$ pin configured to respond only to falling edges. Falling edges on the $\overline{\text{IRQ}}$ pin will be detected anytime IRQE=1 and will be cleared only upon a reset or the servicing of the $\overline{\text{IRQ}}$ interrupt. 0 $\overline{\text{IRQ}}$ pin configured for low level recognition
6 IRQEN	**IRQ ENable** — 1 $\overline{\text{IRQ}}$ pin is connected to interrupt logic 0 $\overline{\text{IRQ}}$ pin is disconnected from interrupt logic

2.3.9 Reserved Register

Address 0x001E (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-7. Reserved Register

[1] Read: Anytime
Write:Never

2.3.10 Reserved Register

Address 0x001F Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 2-8. Reserved Register

[1] Read: Anytime
Write: Only in special mode

NOTE

These reserved registers are designed for factory test purposes only and are not intended for general user access. Writing to these registers when in special modes can alter the module's functionality.

Table 2-26. PTIP Register Field Descriptions

Field	Description
5-0 PTIP	**PorT Input data register port P —** A read always returns the synchronized input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.3.28 Port P Data Direction Register (DDRP)

Address 0x025A (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-37. Port P Data Direction Register (DDRP - S12VR64/48)

[1] Read: Anytime
Write: Anytime

Address 0x025A (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	DDRP2	DDRP1	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-38. Port P Data Direction Register (DDRP - S12VR32/16)

[1] Read: Anytime
Write: Anytime

Table 2-27. DDRP Register Field Descriptions

Field	Description
5 DDRP	**Data Direction Register port P —** This bit determines whether the associated pin is an input or output. The enabled IRQ function forces the I/O state to be an input if enabled. In this case the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
4-2 DDRP	**Data Direction Register port P —** This bit determines whether the associated pin is an input or output. 1 Associated pin is configured as output 0 Associated pin is configured as input

5.1.3 Block Diagram

A block diagram of the BDM is shown in Figure 5-1.

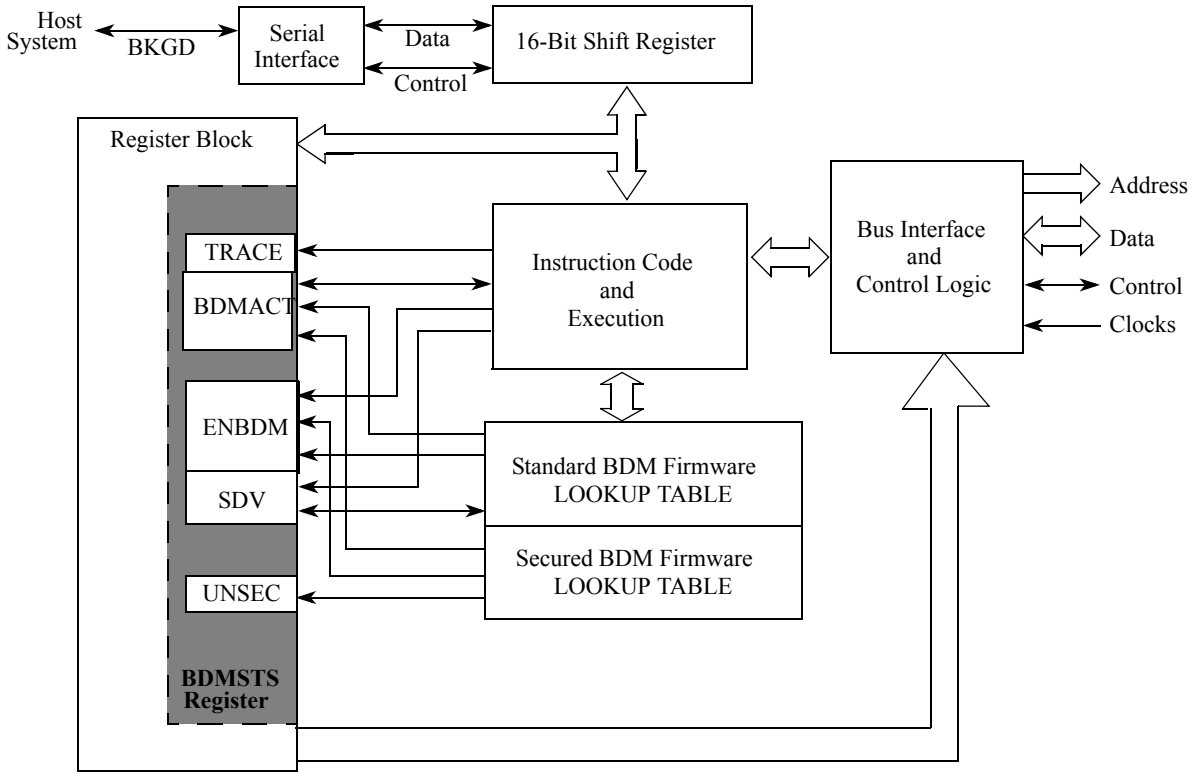

Figure 5-1. BDM Block Diagram

5.2 External Signal Description

A single-wire interface pin called the background debug interface (BKGD) pin is used to communicate with the BDM system. During reset, this pin is a mode select input which selects between normal and special modes of operation. After reset, this pin becomes the dedicated serial interface pin for the background debug mode. The communication rate of this pin is always the BDM clock frequency defined at device level (refer to device overview section). When modifying the VCO clock please make sure that the communication rate is adapted accordingly and a communication time-out (BDM soft reset) has occurred.

5.3 Memory Map and Register Definition

5.3.1 Module Memory Map

Table 5-2 shows the BDM memory map when BDM is active.

6.3.2.8.2 Debug Comparator Address High Register (DBGXAH)

Address: 0x0029

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	Bit 17	Bit 16
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-16. Debug Comparator Address High Register (DBGXAH)

The DBGC1_COMRV bits determine which comparator address registers are visible in the 8-byte window from 0x0028 to 0x002F as shown in Section Table 6-24., “Comparator Address Register Visibility

Table 6-24. Comparator Address Register Visibility

COMRV	Visible Comparator
00	DBGAAH, DBGAAM, DBGAAL
01	DBGBAH, DBGBAM, DBGBAL
10	DBGCAH, DBGCAM, DBGCAL
11	None

Read: Anytime. See Table 6-24 for visible register encoding.

Write: If DBG not armed. See Table 6-24 for visible register encoding.

Table 6-25. DBGXAH Field Descriptions

Field	Description
1–0 Bit[17:16]	**Comparator Address High Compare Bits** — The Comparator address high compare bits control whether the selected comparator compares the address bus bits [17:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

6.3.2.8.3 Debug Comparator Address Mid Register (DBGXAM)

Address: 0x002A

	7	6	5	4	3	2	1	0
R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
Reset	0	0	0	0	0	0	0	0

Figure 6-17. Debug Comparator Address Mid Register (DBGXAM)

Read: Anytime. See Table 6-24 for visible register encoding.

Write: If DBG not armed. See Table 6-24 for visible register encoding.

8.3.2.4 ATD Control Register 3 (ATDCTL3)

Writes to this register will abort current conversion sequence.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R W	DJM	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-6. ATD Control Register 3 (ATDCTL3)

Read: Anytime

Write: Anytime

Table 8-8. ATDCTL3 Field Descriptions

Field	Description
7 DJM	**Result Register Data Justification** — Result data format is always unsigned. This bit controls justification of conversion data in the result registers. 0 Left justified data in the result registers. 1 Right justified data in the result registers. Table 8-9 gives example ATD results for an input signal range between 0 and 5.12 Volts.
6–3 S8C, S4C, S2C, S1C	**Conversion Sequence Length** — These bits control the number of conversions per sequence. Table 8-10 shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 family.
2 FIFO	**Result Register FIFO Mode** — If this bit is zero (non-FIFO mode), the A/D conversion results map into the result registers based on the conversion sequence; the result of the first conversion appears in the first result register (ATDDR0), the second result in the second result register (ATDDR1), and so on. If this bit is one (FIFO mode) the conversion counter is not reset at the beginning or end of a conversion sequence; sequential conversion results are placed in consecutive result registers. In a continuously scanning conversion sequence, the result register counter will wrap around when it reaches the end of the result register file. The conversion counter value (CC3-0 in ATDSTAT0) can be used to determine where in the result register file, the current conversion result will be placed. Aborting a conversion or starting a new conversion clears the conversion counter even if FIFO=1. So the first result of a new conversion sequence, started by writing to ATDCTL5, will always be place in the first result register (ATDDDR0). Intended usage of FIFO mode is continuos conversion (SCAN=1) or triggered conversion (ETRIG=1). Which result registers hold valid data can be tracked using the conversion complete flags. Fast flag clear mode may be useful in a particular application to track valid data. If this bit is one, automatic compare of result registers is always disabled, that is ADC12B6CV2 will behave as if ACMPIE and all CPME[*n*] were zero. 0 Conversion results are placed in the corresponding result register up to the selected sequence length. 1 Conversion results are placed in consecutive result registers (wrap around at end).
1–0 FRZ[1:0]	**Background Debug Freeze Enable** — When debugging an application, it is useful in many cases to have the ATD pause when a breakpoint (Freeze Mode) is encountered. These 2 bits determine how the ATD will respond to a breakpoint as shown in Table 8-11. Leakage onto the storage node and comparator reference capacitors may compromise the accuracy of an immediately frozen conversion depending on the length of the freeze period.

9.4.2.6 Center Aligned Outputs

For center aligned output mode selection, set the CAEx bit (CAEx = 1) in the PWMCAE register and the corresponding PWM output will be center aligned.

The 8-bit counter operates as an up/down counter in this mode and is set to up whenever the counter is equal to $00. The counter compares to two registers, a duty register and a period register as shown in the block diagram in Figure 9-16. When the PWM counter matches the duty register, the output flip-flop changes state, causing the PWM waveform to also change state. A match between the PWM counter and the period register changes the counter direction from an up-count to a down-count. When the PWM counter decrements and matches the duty register again, the output flip-flop changes state causing the PWM output to also change state. When the PWM counter decrements and reaches zero, the counter direction changes from a down-count back to an up-count and a load from the double buffer period and duty registers to the associated registers is performed, as described in Section 9.4.2.3, “PWM Period and Duty”. The counter counts from 0 up to the value in the period register and then back down to 0. Thus the effective period is PWMPERx*2.

NOTE

Changing the PWM output mode from left aligned to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

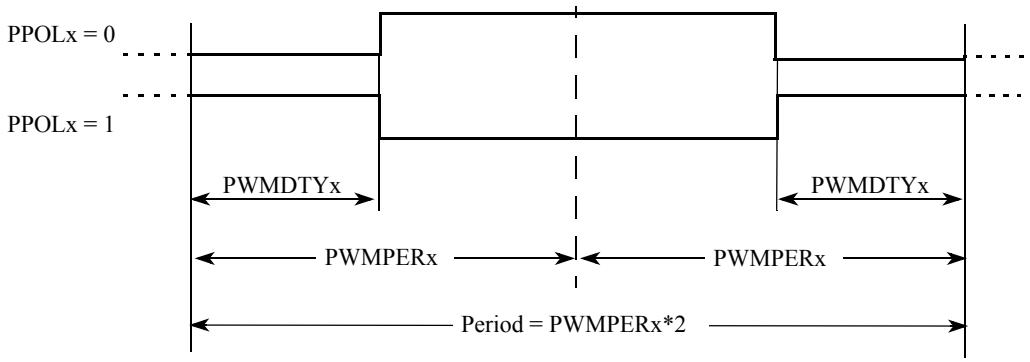

Figure 9-19. PWM Center Aligned Output Waveform

To calculate the output frequency in center aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB) and divide it by twice the value in the period register for that channel.

- PWMx Frequency = Clock (A, B, SA, or SB) / (2*PWMPERx)
- PWMx Duty Cycle (high time as a% of period):
  - Polarity = 0 (PPOLx = 0)
    Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  - Polarity = 1 (PPOLx = 1)
    Duty Cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a center aligned output, consider the following case:

10.3.2.5 SCI Alternative Control Register 2 (SCIACR2)

	7	6	5	4	3	2	1	0
R	IREN	TNP1	TNP0	0	0	BERRM1	BERRM0	BKDFE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-8. SCI Alternative Control Register 2 (SCIACR2)

Read: Anytime, if AMAP = 1

Write: Anytime, if AMAP = 1

Table 10-7. SCIACR2 Field Descriptions

Field	Description
7 IREN	**Infrared Enable Bit** — This bit enables/disables the infrared modulation/demodulation submodule. 0 IR disabled 1 IR enabled
6:5 TNP[1:0]	**Transmitter Narrow Pulse Bits** — These bits enable whether the SCI transmits a 1/16, 3/16, 1/32 or 1/4 narrow pulse. See Table 10-8.
2:1 BERRM[1:0]	**Bit Error Mode** — Those two bits determines the functionality of the bit error detect feature. See Table 10-9.
0 BKDFE	**Break Detect Feature Enable** — BKDFE enables the break detect circuitry. 0 Break detect circuit disabled 1 Break detect circuit enabled

Table 10-8. IRSCI Transmit Pulse Width

TNP[1:0]	Narrow Pulse Width
11	1/4
10	1/32
01	1/16
00	3/16

Table 10-9. Bit Error Mode Coding

BERRM1	BERRM0	Function
0	0	Bit error detect circuit is disabled
0	1	Receive input sampling occurs during the 9th time tick of a transmitted bit (refer to Figure 10-19)
1	0	Receive input sampling occurs during the 13th time tick of a transmitted bit (refer to Figure 10-19)
1	1	Reserved

Table 12-14. TRLG2 Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to bit 7 of TFLG2 register while the TEN bit of TSCR1 is set to one .

12.3.2.12 Timer Input Capture/Output Compare Registers High and Low 0– 3(TCxH and TCxL)

	15	14	13	12	11	10	9	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 12-18. Timer Input Capture/Output Compare Register x High (TCxH)

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 12-19. Timer Input Capture/Output Compare Register x Low (TCxL)

[1] This register is available only when the corresponding channel exists and is reserved if that channel does not exist. Writes to a reserved register have no functional effect. Reads from a reserved register return zeroes.

Depending on the TIOS bit for the corresponding channel, these registers are used to latch the value of the free-running counter when a defined transition is sensed by the corresponding input capture edge detector or to trigger an output action for output compare.

Read: Anytime

Write: Anytime for output compare function.Writes to these registers have no meaning or effect during input capture. All timer input capture/output compare registers are reset to 0x0000.

NOTE

Read/Write access in byte mode for high byte should take place before low byte otherwise it will give a different result.

15.3.4 LSDRV Configuration Register (LSCR)

Module Base + 0x0001 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	LSOLE1	LSOLE0	LSE1	LSE0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 15-3. LSDRV Configuration Register (LSCR)

[1] Read: Anytime
Write: Anytime

Table 15-5. LSCR Register Field Descriptions

Field	Description
3-2 LSOLEx	**LSDRV High-Load Resistance Open-Load Detection Enable** These bits enable the measurement function to detect an open-load condition on the related low-side driver operating on high-load resistance loads. If the low-side driver is enabled and is not being driven by the selected source, then the high-load resistance detection circuit is activated when this bit is set to '1'. 0 high-load resistance open-load detection is disabled 1 high-load resistance open-load detection is enabled
1-0 LSEx	**LSDRV Enable** These bits control the bias of the related low-side driver circuit. 0 Low-side driver is disabled. 1 Low-side driver is enabled. **NOTE** After enabling the low-side driver (write "1" to LSEx) a settling time $t_{LS\_settling}$ is required before the low-side driver is allowed to be turned on (e.g. by writing LSDRx bits).

Please note that if the bit time is smaller than the parameter t_{OCLIM} (please refer to electricals), then no overcurrent is reported nor does an overcurrent shutdown occur. However, the current limitation is always engaged in case of a failure.

16.4.3 Modes

Figure 16-11 shows the possible mode transitions depending on control bits, stop mode, and error conditions.

16.4.3.1 Shutdown Mode

The LIN Physical Layer is fully disabled. No wake-up functionality is available. The internal pullup resistor is high ohmic only (330 kΩ) to maintain the LIN Bus pin in the recessive state. LPTxD is not monitored in this mode for a TxD-dominant timeout. All the registers are accessible.

Setting LPE causes the module to leave the shutdown mode and to enter the normal mode or receive only mode (if RXONLY bit is set).

Clearing LPE causes the module to leave the normal or receive only modes and go back to shutdown mode.

16.4.3.2 Normal Mode

The full functionality is available. Both receiver and transmitter are enabled. The internal pullup resistor can be chosen to be high ohmic (330 kΩ) if LPPUE = 0, or LIN compliant (34 kΩ) if LPPUE = 1.

If RXONLY is set, the module leaves normal mode to enter receive only mode.

If the MCU enters stop mode, the LIN Physical Layer enters standby mode.

16.4.3.3 Receive Only Mode

Entering this mode disables the transmitter and immediately stops any on-going transmission. LPTxD is not monitored in this mode for a TxD-dominant timeout.

The receiver is running in full performance mode in all cases.

To return to normal mode, the RXONLY bit must be cleared.

If the device enters stop mode, the module leaves receive only mode to enter standby mode.

16.4.3.4 Standby Mode with Wake-Up Feature

The transmitter of the LIN Physical Layer is disabled and the receiver enters a low power mode.

NOTE

Before entering standby mode, ensure no transmissions are ongoing.

If LPWUE is not set, no wake up feature is available and the standby mode has the same electrical properties as the shutdown mode. This allows a low-power consumption of the device in stop mode if the wake-up feature is not needed.

Table A-11. Peripheral Configurations for Run & Wait Current Measurement

Peripheral	Configuration
SCI	continuously transmit data (0x55) at speed of 19200 baud
SPI	configured to master mode, continuously transmit data (0x55) at 1Mbit/s
PWM	configured to toggle its pins at the rate of 40kHz
ADC	the peripheral is configured to operate at its maximum specified frequency and to continuously convert voltages on all input channels in sequence.
DBG	the module is enabled and the comparators are configured to trigger in outside range.The range covers all the code executed by the core.
TIM	the peripheral is configured to output compare mode, pulse accumulator and modulus counter enabled.
COP & RTI	enabled
HSDRV 1 & 2	module is enabled but output driver disabled
LSDRV 1 & 2	module is enabled but output driver disabled
BATS	enabled
LINPHY	connected to SCI and continuously transmit data (0x55) at speed of 19200 baud

Table A-12. Run and Wait Current Characteristics

Conditions are: V_{SUP}=V_{SUPHS}=18V, T_A=105°C, see Table A-10 and Table A-9						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Run Current	I_{SUPR}		15	22	mA
2	Wait Current	I_{SUPW}		10	15	mA

Appendix M
FTMRG Electrical Specifications

M.1 Timing Parameters

The time base for all NVM program or erase operations is derived from the bus clock using the FCLKDIV register. The frequency of this derived clock must be set within the limits specified as f_{NVMOP}. The NVM module does not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. When attempting to program or erase the NVM module at a lower frequency, a full program or erase transition is not assured.

All timing parameters are a function of the bus clock frequency, f_{NVMBUS}. All program and erase times are also a function of the NVM operating frequency, f_{NVMOP}. A summary of key timing parameters can be found in **Table M-1.** and **Table M-2.**

Table M-1. Operating frequency

	Symbol	Min	Typ	Max	Unit
Bus Frequency	f_{NVMBUS}	1	25	25	MHz
Operating Frequency	f_{NVMOP}	0,8	1	1.05	MHz

Table M-2. NVM Timing Characteristics for S12FTMRG64K512

#	Command	f_{NVMOP} cycle	f_{NVMBUS} cycle	Symbol	Min[1]	Typ[2]	Max[3]	Lfmax[4]	Unit
1	Erase Verify All Blocks	0	17169	t_{RD1ALL}	0.69	0.69	1.37	34.34	ms
2	Erase Verify Block (Pflash)	0	16924	t_{RD1BLK_P}	0.68	0.68	1.35	33.85	ms
3	Erase Verify Block (EEPROM)	0	744	t_{RD1BLK_D}	0.03	0.03	0.06	1.49	ms
4	Erase Verify P-Flash Section	0	476	t_{RD1SEC}	19.04	19.04	38.08	952.00	us
5	Read Once	0	445	t_{RDONCE}	17.80	17.80	17.80	445.00	us
6	Program P-Flash (4 Word)	164	2896	t_{PGM_4}	0.27	0.28	0.63	11.79	ms
7	Program Once	164	2859	$t_{PGMONCE}$	0.27	0.28	0.28	3.06	ms
8	Erase All Blocks	100066	17505	t_{ERSALL}	96.00	100.77	101.47	160.09	ms
9	Erase Flash Block (Pflash)	100060	17150	t_{ERSBLK_P}	95.98	100.75	101.43	159.38	ms
10	Erase Flash Block (EEPROM)	100060	1033	t_{ERSBLK_D}	95.34	100.10	100.14	127.14	ms

P.14 0x00A0-0x00C7 Pulse Width Modulator 6-Channels (PWM) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00B0	PWMCNT4	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00B1	PWMCNT5	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00B2	PWMCNT6	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00B3	PWMCNT7	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00B4	PWMPER0	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00B5	PWMPER1	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00B6	PWMPER2	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00B7	PWMPER3	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00B8	PWMPER4	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00B9	PWMPER5	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00BA	PWMPER6	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00BB	PWMPER7	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00BC	PWMDTY0	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00BD	PWMDTY1	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00BE	PWMDTY2	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00BF	PWMDTY3	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00C0	PWMDTY4	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00C1	PWMDTY5	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00C2	PWMDTY6	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00C3	PWMDTY7	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00C4-0 x00C7	Reserved	R	0	0	0	0	0	0	0	0
		W								

P.23 0x0140-0x0147 High Side Drivers

P.23.1 S12HSDRVV2 on MC9S12VR64/48

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0140	HSDR	R	0	0	0	0	0	0	HSDR1	HSDR0
		W								
0x0141	HSCR	R	0	0	HSOCME1	HSOCME0	0	0	HSE1	HSE0
		W								
0x0142	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0143	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0144	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0145	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0146	HSIE	R	HSOCIE	0	0	0	0	0	0	0
		W								
0x0147	HSIF	R	0	0	0	0	0	0	HSOCIF1	HSOCIF0
		W								

P.23.2 S12HSDRV1CV3 on MC9S12VR32/16

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0140	HSDR	R	0	0	0	0	0	0	0	HSDR0
		W								
0x0141	HSCR	R	0	0	0	HSOCME0	0	HSOLE0	0	HSE0
		W								
0x0142	HSSLR	R	0	0	0	0	0	HSSLCU0	0	HSSLEN0
		W								
0x0143	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0144	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0145	Reserved	R	0	0	0	0	0	0	0	HSOL0
		W								
0x0146	HSIE	R	HSOCIE	0	0	0	0	0	0	0
		W								
0x0147	HSIF	R	0	0	0	0	0	0	0	HSOCIF0
		W								