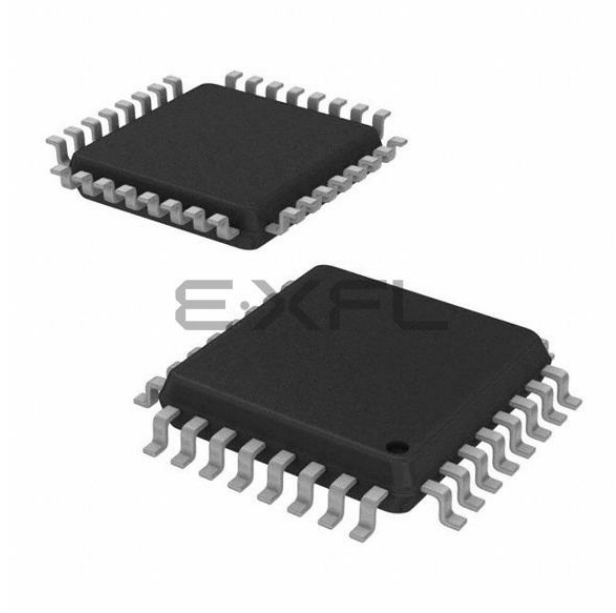

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Details	
Product Status	Active
Core Processor	12V1
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Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vr32f0clcr

Chapter 9
Pulse-Width Modulator (S12PWM8B8CV2)

Chapter 10
Serial Communication Interface (S12SCIV6)

Table 2-19. DDRS Register Field Descriptions (continued)

Field	Description
2 DDRS	**Data Direction Register port S —** This bit determines whether the associated pin is an input or output. The enabled API_EXTCLK function forces the I/O state to output. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. The routed SCI1 function forces the I/O state to input if enabled. The routed PWM function forces the I/O state to output if enabled. In these cases the data direction bit will not change. The routed ETRIG function has no effect on the I/O state. 1 Associated pin is configured as output 0 Associated pin is configured as input
1 DDRS	**Data Direction Register port S —** This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SCI the I/O state will be forced to be input or output. The enabled routed LINPHY forces the I/O state to be an output (LPDR[LPDR1]). In these cases the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
0 DDRS	**Data Direction Register port S —** This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SCI the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input

2.3.22 Port S Pull Device Enable Register (PERS)

Address 0x024C (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
W								
Reset	0	0	1	1	1	1	1	1

Figure 2-24. Port S Pull Device Enable Register (PERS - S12VR64/48)

1 Read: Anytime
Write: Anytime

Address 0x024C (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PERS3	PERS2	0	0
W								
Reset	0	0	0	0	1	1	0	0

Figure 2-25. Port S Pull Device Enable Register (PERS - S12VR32/16)

1 Read: Anytime
Write: Anytime

2.3.33 Port P Interrupt Flag Register (PIFP)

Address 0x025F (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	OCIF	0	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-47. Port P Interrupt Flag Register (PIFP - S12VR64/48)

[1] Read: Anytime
Write: Anytime, write 1 to clear

Address 0x025F (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	OCIF	0	0	0	0	PIFP2	PIFP1	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-48. Port P Interrupt Flag Register (PIFP - S12VR32/16)

[1] Read: Anytime
Write: Anytime, write 1 to clear

Table 2-32. PIFP Register Field Descriptions

Field	Description
7 OCIF	**Over-Current Interrupt Flag** register port P — This flag asserts if an over-current condition is detected on PP2 (Section 2.4.4.3, “Over-Current Interrupt and Protection”). 1 PP2 Over-current event occurred 0 No PP2 over-current event occurred
5-0 PIFP	**Pin Interrupt Flag** register port P — This flag asserts after a valid active edge was detected on the related pin (Section 2.4.4, “Interrupts”). This can be a rising or a falling edge based on the state of the polarity select register. An interrupt will occur if the associated interrupt enable bit is set. 1 Active edge on the associated bit has occurred 0 No active edge occurred

voltage divider can be bypassed (PTAL[PTADIRL]=1). Additionally in latter case the impedance converter in the ADC signal path can be configured to be used or bypassed in direct input mode (PTAL[PTABYPL]).

Out of reset the digital input buffer of the selected pin is disabled to avoid shoot-through current. Pin interrupts can only be generated if DIENL[x]=1.

In stop mode the digital input buffer is enabled if DIENL[x]=1 or if the PTAL[PTTEL] bit is set to support wakeup functionality.

Table 2-49 shows the HVI input configuration depending on register bits and operation mode.

Table 2-49. HVI Input Configurations

Mode	DIENL	PTAENL	Digital Input	Analog Input	Resulting Function
Run/Wait	0	0	off	off	Input disabled (Reset)
	0	1	off[1]	enabled	Analog input, interrupt not supported
	1	0	enabled	off	Digital input, interrupt supported
	1	1	off[1]	enabled	Analog input, interrupt not supported
Stop	0	X	off	off	If PTAL[PTTEL] is set: input enabled, wakeup from stop supported. If PTAL[PTTEL] is cleared: input disabled, wakeup from stop not supported.
	1	X	enabled	off	Digital input, wakeup from stop supported

[1] Enabled if (PTAL[PTTEL]=1 & PTAL[PTADIRL]=0)

NOTE

An external resistor R_{EXT_HVI} must always be connected to the high-voltage inputs to protect the device pins from fast transients and to achieve the specified pin input divider ratios when using the HVI in analog mode.

2.4.3.7 Port AD

This port is associated with the ADC.

Port AD pins can be used for either general-purpose I/O, or with the ADC subsystem.

2.4.4 Interrupts

This section describes the interrupts generated by the PIM and their individual sources. Vector addresses and interrupt priorities are defined at MCU level.

Table 2-50. PIM Interrupt Sources

Module Interrupt Sources	Local Enable (S12VR64/48)	Local Enable (S12VR32/16)
$\overline{\text{XIRQ}}$	None	None

Read: Anytime.

Write: Only if a transition is allowed (see Figure 3-4).

The MODC bit of the MODE register is used to select the MCU's operating mode.

Table 3-4. MODE Field Descriptions

Field	Description
7 MODC	**Mode Select Bit** — This bit controls the current operating mode during $\overline{\text{RESET}}$ high (inactive). The external mode pin MODC determines the operating mode during $\overline{\text{RESET}}$ low (active). The state of the pin is registered into the respective register bit after the $\overline{\text{RESET}}$ signal goes inactive (see Figure 3-4). Write restrictions exist to disallow transitions between certain modes. Figure 3-4 illustrates all allowed mode changes. Attempting non authorized transitions will not change the MODE bit, but it will block further writes to the register bit except in special modes. Write accesses to the MODE register are blocked when the device is secured.

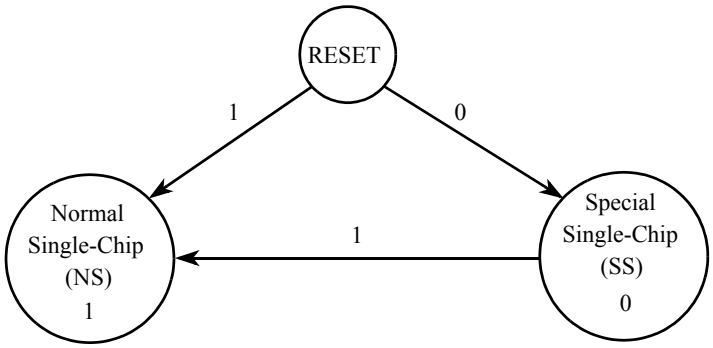

Figure 3-4. Mode Transition Diagram when MCU is Unsecured

3.3.2.2 Direct Page Register (DIRECT)

Address: 0x0011

	7	6	5	4	3	2	1	0
R W	DP15	DP14	DP13	DP12	DP11	DP10	DP9	DP8
Reset	0	0	0	0	0	0	0	0

Figure 3-5. Direct Register (DIRECT)

Read: Anytime

Write: anytime in special SS, write-once in NS.

This register determines the position of the 256 Byte direct page within the memory map.It is valid for both global and local mapping scheme.

Table 4-27. TC trimming of the frequency of the IRC1M at ambient temperature

TCTRIM[4:0]	IRC1M Indicative relative TC variation	IRC1M indicative frequency drift for relative TC variation
00000	0 (nominal TC of the IRC)	0%
00001	-0.27%	-0.5%
00010	-0.54%	-0.9%
00011	-0.81%	-1.3%
00100	-1.08%	-1.7%
00101	-1.35%	-2.0%
00110	-1.63%	-2.2%
00111	-1.9%	-2.5%
01000	-2.20%	-3.0%
01001	-2.47%	-3.4%
01010	-2.77%	-3.9%
01011	-3.04	-4.3%
01100	-3.33%	-4.7%
01101	-3.6%	-5.1%
01110	-3.91%	-5.6%
01111	-4.18%	-5.9%
10000	0 (nominal TC of the IRC)	0%
10001	+0.27%	+0.5%
10010	+0.54%	+0.9%
10011	+0.81%	+1.3%
10100	+1.07%	+1.7%
10101	+1.34%	+2.0%
10110	+1.59%	+2.2%
10111	+1.86%	+2.5%
11000	+2.11%	+3.0%
11001	+2.38%	+3.4%
11010	+2.62%	+3.9%
11011	+2.89%	+4.3%
11100	+3.12%	+4.7%
11101	+3.39%	+5.1%
11110	+3.62%	+5.6%
11111	+3.89%	+5.9%

NOTE

Since the IRC1M frequency is not a linear function of the temperature, but more like a parabola, the above relative variation is only an indication and should be considered with care.

NOTE

The ACK pulse does not provide a time out. This means for the GO_UNTIL command that it can not be distinguished if a stop or wait has been executed (command discarded and ACK not issued) or if the “UNTIL” condition (BDM active) is just not reached yet. Hence in any case where the ACK pulse of a command is not issued the possible pending command should be aborted before issuing a new command. See the handshake abort procedure described in Section 5.4.8, “Hardware Handshake Abort Procedure”.

5.4.8 Hardware Handshake Abort Procedure

The abort procedure is based on the SYNC command. In order to abort a command, which had not issued the corresponding ACK pulse, the host controller should generate a low pulse in the BKGD pin by driving it low for at least 128 serial clock cycles and then driving it high for one serial clock cycle, providing a speedup pulse. By detecting this long low pulse in the BKGD pin, the target executes the SYNC protocol, see Section 5.4.9, “SYNC — Request Timed Reference Pulse”, and assumes that the pending command and therefore the related ACK pulse, are being aborted. Therefore, after the SYNC protocol has been completed the host is free to issue new BDM commands. For BDM firmware READ or WRITE commands it can not be guaranteed that the pending command is aborted when issuing a SYNC before the corresponding ACK pulse. There is a short latency time from the time the READ or WRITE access begins until it is finished and the corresponding ACK pulse is issued. The latency time depends on the firmware READ or WRITE command that is issued and on the selected bus clock rate. When the SYNC command starts during this latency time the READ or WRITE command will not be aborted, but the corresponding ACK pulse will be aborted. A pending GO, TRACE1 or GO_UNTIL command can not be aborted. Only the corresponding ACK pulse can be aborted by the SYNC command.

Although it is not recommended, the host could abort a pending BDM command by issuing a low pulse in the BKGD pin shorter than 128 serial clock cycles, which will not be interpreted as the SYNC command. The ACK is actually aborted when a negative edge is perceived by the target in the BKGD pin. The short abort pulse should have at least 4 clock cycles keeping the BKGD pin low, in order to allow the negative edge to be detected by the target. In this case, the target will not execute the SYNC protocol but the pending command will be aborted along with the ACK pulse. The potential problem with this abort procedure is when there is a conflict between the ACK pulse and the short abort pulse. In this case, the target may not perceive the abort pulse. The worst case is when the pending command is a read command (i.e., READ_BYTE). If the abort pulse is not perceived by the target the host will attempt to send a new command after the abort pulse was issued, while the target expects the host to retrieve the accessed memory byte. In this case, host and target will run out of synchronism. However, if the command to be aborted is not a read command the short abort pulse could be used. After a command is aborted the target assumes the next negative edge, after the abort pulse, is the first bit of a new BDM command.

NOTE

The details about the short abort pulse are being provided only as a reference for the reader to better understand the BDM internal behavior. It is not recommended that this procedure be used in a real application.

8.3.2.7 ATD Status Register 0 (ATDSTAT0)

This register contains the Sequence Complete Flag, overrun flags for external trigger and FIFO mode, and the conversion counter.

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-9. ATD Status Register 0 (ATDSTAT0)

Read: Anytime

Write: Anytime (No effect on (CC3, CC2, CC1, CC0))

Table 8-16. ATDSTAT0 Field Descriptions

Field	Description
7 SCF	**Sequence Complete Flag** — This flag is set upon completion of a conversion sequence. If conversion sequences are continuously performed (SCAN=1), the flag is set after each one is completed. This flag is cleared when one of the following occurs: A) Write “1” to SCF B) Write to ATDCTL5 (a new conversion sequence is started) C) If AFFC=1 and a result register is read 0 Conversion sequence not completed 1 Conversion sequence has completed
5 ETORF	**External Trigger Overrun Flag** — While in edge sensitive mode (ETRIGLE=0), if additional active edges are detected while a conversion sequence is in process the overrun flag is set. This flag is cleared when one of the following occurs: A) Write “1” to ETORF B) Write to ATDCTL0,1,2,3,4, ATDCMPE or ATDCMPHT (a conversion sequence is aborted) C) Write to ATDCTL5 (a new conversion sequence is started) 0 No External trigger overrun error has occurred 1 External trigger overrun error has occurred
4 FIFOR	**Result Register Overrun Flag** — This bit indicates that a result register has been written to before its associated conversion complete flag (CCF) has been cleared. This flag is most useful when using the FIFO mode because the flag potentially indicates that result registers are out of sync with the input channels. However, it is also practical for non-FIFO modes, and indicates that a result register has been overwritten before it has been read (i.e. the old data has been lost). This flag is cleared when one of the following occurs: A) Write “1” to FIFOR B) Write to ATDCTL0,1,2,3,4, ATDCMPE or ATDCMPHT (a conversion sequence is aborted) C) Write to ATDCTL5 (a new conversion sequence is started) 0 No overrun has occurred 1 Overrun condition exists (result register has been written while associated CCFx flag was still set)

Table 8-16. ATDSTAT0 Field Descriptions (continued)

Field	Description
3–0 CC[3:0]	**Conversion Counter** — These 4 read-only bits are the binary value of the conversion counter. The conversion counter points to the result register that will receive the result of the current conversion. E.g. CC3=0, CC2=1, CC1=1, CC0=0 indicates that the result of the current conversion will be in ATD Result Register 6. If in non-FIFO mode (FIFO=0) the conversion counter is initialized to zero at the beginning and end of the conversion sequence. If in FIFO mode (FIFO=1) the register counter is not initialized. The conversion counter wraps around when its maximum value is reached. Aborting a conversion or starting a new conversion clears the conversion counter even if FIFO=1.

8.3.2.8 ATD Compare Enable Register (ATDCMPE)

Writes to this register will abort current conversion sequence.

Read: Anytime

Write: Anytime

Module Base + 0x0008

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	CMPE[5:0]					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-10. ATD Compare Enable Register (ATDCMPE)

Table 8-17. ATDCMPE Field Descriptions

Field	Description
5–0 CMPE[5:0]	**Compare Enable for Conversion Number *n* (*n*= 5, 4, 3, 2, 1, 0) of a Sequence (*n conversion number, NOT channel number!)*** — These bits enable automatic compare of conversion results individually for conversions of a sequence. The sense of each comparison is determined by the CMPHT[*n*] bit in the ATDCMPHT register. For each conversion number with CMPE[*n*]=1 do the following: 1) Write compare value to ATDDR*n* result register 2) Write compare operator with CMPHT[*n*] in ATDCPMHT register CCF[*n*] in ATDSTAT2 register will flag individual success of any comparison. 0 No automatic compare 1 Automatic compare of results for conversion *n* of a sequence is enabled.

12.3.2.7 Timer Control Register 3/Timer Control Register 4 (TCTL3 and TCTL4)

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Figure 12-12. Timer Control Register 3 (TCTL3)

	7	6	5	4	3	2	1	0
R W	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
Reset	0	0	0	0	0	0	0	0

Figure 12-13. Timer Control Register 4 (TCTL4)

Read: Anytime

Write: Anytime.

Table 12-8. TCTL3/TCTL4 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 EDGnB EDGnA	**Input Capture Edge Control** — These four pairs of control bits configure the input capture edge detector circuits.

Table 12-9. Edge Detector Circuit Configuration

EDGnB	EDGnA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

12.3.2.8 Timer Interrupt Enable Register (TIE)

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	C3I	C2I	C1I	C0I
Reset	0	0	0	0	0	0	0	0

Figure 12-14. Timer Interrupt Enable Register (TIE)

Read: Anytime

12.3.2.13 Output Compare Pin Disconnect Register(OCPD)

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	OCPD3	OCPD2	OCPD1	OCPD0
Reset	0	0	0	0	0	0	0	0

Figure 12-20. Output Compare Pin Disconnect Register (OCPD)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 12-15. OCPD Field Description

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 OCPD[3:0]	**Output Compare Pin Disconnect Bits** 0 Enables the timer channel port. Output Compare action will occur on the channel pin. These bits do not affect the input capture . 1 Disables the timer channel port. Output Compare action will not occur on the channel pin, but the output compare flag still become set.

12.3.2.14 Precision Timer Prescaler Select Register (PTPSR)

	7	6	5	4	3	2	1	0
R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
Reset	0	0	0	0	0	0	0	0

Figure 12-21. Precision Timer Prescaler Select Register (PTPSR)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 12-16. PTPSR Field Descriptions

Field	Description
7:0 PTPS[7:0]	**Precision Timer Prescaler Select Bits** — These eight bits specify the division rate of the main Timer prescaler. These are effective only when the PRNT bit of TSCR1 is set to 1. Table 12-17 shows some selection examples in this case. The newly selected prescale factor will not take effect until the next synchronized edge where all prescale counter stages equal zero.

The Prescaler can be calculated as follows depending on logical value of the PTPS[7:0] and PRNT bit:

PRNT = 1 : Prescaler = PTPS[7:0] + 1

Table 17-5. BATIF Register Field Descriptions

Field	Description
1 BVHIF	**BATS Interrupt Flag High Detect** — The flag is set to 1 when BVHC status bit changes. 0 No change of the BVHC status bit since the last clearing of the flag. 1 BVHC status bit has changed since the last clearing of the flag.
0 BVLIF	**BATS Interrupt Flag Low Detect** — The flag is set to 1 when BVLC status bit changes. 0 No change of the BVLC status bit since the last clearing of the flag. 1 BVLC status bit has changed since the last clearing of the flag.

17.3.2.5 Reserved Register

Module Base + 0x0006
Module Base + 0x0007

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 17-8. Reserved Register

[1] Read: Anytime
Write: Only in special mode

NOTE

These reserved registers are designed for factory test purposes only and are not intended for general user access. Writing to these registers when in special mode can alter the module's functionality.

17.4 Functional Description

17.4.1 General

The BATS module allows measuring voltages on the VSENSE and VSUP pins. The VSENSE pin is implemented to allow measurement of the supply Line (Battery) Voltage V_{BAT} directly. By bypassing the device supply capacitor and the external reversed battery protection diode this pin allows to detect under/over voltage conditions without delay. A series resistor (R_{VSENSE_R}) is required to protect the VSENSE pin from fast transients.

The voltage at the VSENSE or VSUP pin can be routed via an internal voltage divider to an internal Analog to Digital Converter Channel. Also the BATS module can be configured to generate a low and high voltage interrupt based on VSENSE or VSUP. The trigger level of the high and low interrupt are selectable.

In a typical application, the module could be used as follows: The voltage at VSENSE is observed via usage of the interrupt feature (BSESE=1, BVHIE=1), while the VSUP pin voltage is routed to the ADC to allow regular measurement (BSUAE=1).

18.4.4.4 P-Flash Commands

Table 18-28 summarizes the valid P-Flash commands along with the effects of the commands on the P-Flash block and other resources within the Flash module.

Table 18-28. P-Flash Commands

FCMD	Command	Function on P-Flash Memory
0x01	Erase Verify All Blocks	Verify that all P-Flash (and EEPROM) blocks are erased.
0x02	Erase Verify Block	Verify that a P-Flash block is erased.
0x03	Erase Verify P-Flash Section	Verify that a given number of words starting at the address provided are erased.
0x04	Read Once	Read a dedicated 64 byte field in the nonvolatile information register in P-Flash block that was previously programmed using the Program Once command.
0x06	Program P-Flash	Program a phrase in a P-Flash block.
0x07	Program Once	Program a dedicated 64 byte field in the nonvolatile information register in P-Flash block that is allowed to be programmed only once.
0x08	Erase All Blocks	Erase all P-Flash (and EEPROM) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the DPOPEN bit in the EEPROT register are set prior to launching the command.
0x09	Erase Flash Block	Erase a P-Flash (or EEPROM) block. An erase of the full P-Flash block is only possible when FPLDIS, FPHDIS and FPOPEN bits in the FPROT register are set prior to launching the command.
0x0A	Erase P-Flash Sector	Erase all bytes in a P-Flash sector.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all P-Flash (and EEPROM) blocks and verifying that all P-Flash (and EEPROM) blocks are erased.
0x0C	Verify Backdoor Access Key	Supports a method of releasing MCU security by verifying a set of security keys.
0x0D	Set User Margin Level	Specifies a user margin read level for all P-Flash blocks.
0x0E	Set Field Margin Level	Specifies a field margin read level for all P-Flash blocks (special modes only).

18.4.4.5 EEPROM Commands

Table 18-29 summarizes the valid EEPROM commands along with the effects of the commands on the EEPROM block.

Table 18-29. EEPROM Commands

FCMD	Command	Function on EEPROM Memory
0x01	Erase Verify All Blocks	Verify that all EEPROM (and P-Flash) blocks are erased.
0x02	Erase Verify Block	Verify that the EEPROM block is erased.

Table 18-46. Erase Flash Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x09	Global address [17:16] to identify Flash block
001	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table 18-47. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 18-27)
		Set if an invalid global address [17:16] is supplied
		Set if the supplied P-Flash address is not phrase-aligned or if the EEPROM address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

18.4.6.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 18-48. Erase P-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0A	Global address [17:16] to identify P-Flash block to be erased
001	Global address [15:0] anywhere within the sector to be erased. Refer to Section 18.1.2.1 P-Flash Features for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

Table 19-7. FCLKDIV Field Descriptions (continued)

Field	Description
6 FDIVLCK	**Clock Divider Locked** 0 FDIV field is open for writing 1 FDIV value is locked and cannot be changed. Once the lock bit is set high, only reset can clear this bit and restore writability to the FDIV field in normal mode.
5–0 FDIV[5:0]	**Clock Divider Bits** — FDIV[5:0] must be set to effectively divide BUSCLK down to 1 MHz to control timed events during Flash program and erase algorithms. Table 19-8 shows recommended values for FDIV[5:0] based on the BUSCLK frequency. Please refer to Section 19.4.4, "Flash Command Operations," for more information.

Table 19-8. FDIV values for various BUSCLK Frequencies

BUSCLK Frequency (MHz)		FDIV[5:0]	BUSCLK Frequency (MHz)		FDIV[5:0]
MIN[1]	MAX[2]		MIN[1]	MAX[2]	
1.0	1.6	0x00	16.6	17.6	0x10
1.6	2.6	0x01	17.6	18.6	0x11
2.6	3.6	0x02	18.6	19.6	0x12
3.6	4.6	0x03	19.6	20.6	0x13
4.6	5.6	0x04	20.6	21.6	0x14
5.6	6.6	0x05	21.6	22.6	0x15
6.6	7.6	0x06	22.6	23.6	0x16
7.6	8.6	0x07	23.6	24.6	0x17
8.6	9.6	0x08	24.6	25.6	0x18
9.6	10.6	0x09			
10.6	11.6	0x0A			
11.6	12.6	0x0B			
12.6	13.6	0x0C			
13.6	14.6	0x0D			
14.6	15.6	0x0E			
15.6	16.6	0x0F			

1 BUSCLK is Greater Than this value.

2 BUSCLK is Less Than or Equal to this value.

19.3.2.2 Flash Security Register (FSEC)

The FSEC register holds all bits associated with the security of the MCU and Flash module.

Upon clearing CCIF to launch the Set Field Margin Level command, the Memory Controller will set the

Table 19-57. Set Field Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0E	Flash block selection code [1:0]. See Table 19-34
001	Margin level setting.	

field margin level for the targeted block and then set the CCIF flag.

NOTE

When the EEPROM block is targeted, the EEPROM field margin levels are applied only to the EEPROM reads. However, when the P-Flash block is targeted, the P-Flash field margin levels are applied to both P-Flash and EEPROM reads. It is not possible to apply field margin levels to the P-Flash block only.

Valid margin level settings for the Set Field Margin Level command are defined in Table 19-58.

Table 19-58. Valid Set Field Margin Level Settings

CCOB (CCOBIX=001)	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level[1]
0x0002	User Margin-0 Level[2]
0x0003	Field Margin-1 Level[1]
0x0004	Field Margin-0 Level[2]

1 Read margin to the erased state

2 Read margin to the programmed state

Table 19-59. Set Field Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 19-27)
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied (See Table 19-34)
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

Table I-2. Static Electrical Characteristics - Supply Voltage Sense - (BATS).

Characteristics noted under conditions 5.5V ≤ VSUP ≤ 18 V, -40°C ≤ T_J ≤ 150°C[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C[2] under nominal conditions unless otherwise noted. All parameters in this table assume a in series connected R_{VSENSE_R} at VSENSE pin unless otherwise noted and are valid on input voltage of R_{VSENSE_R} and not on VSENSE pin.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
9	VSENSE Series Resistor Required to be placed externally at VSENSE pin.	R_{VSENSE_R}	9.5	10	10.5	kΩ
10	VSENSE Impedance If path to ground is enabled. Value at VSENSE pin. R_{VSENSE_R} is excluded.	R_{VSEN_IMP}	–	350	–	kΩ
11	VSENSE Input Capacitance	C_{VSEN_IN}	–	8	–	pF

1 T_J: Junction Temperature

2 T_A: Ambient Temperature

3 V_{ADC}: Voltage accessible at the ATD input channel

I.3 Dynamic Electrical Characteristics

Table I-3. Dynamic Electrical Characteristics - Supply Voltage Sense - (BATS).

Characteristics noted under conditions 5.5V ≤ VSUP ≤ 18 V, -40°C ≤ T_J ≤ 150°C[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C[2] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Enable Stabilisation Time	T_{EN_UNC}	–	1	–	µs
2	Voltage Warning Low Pass Filter	f_{VWLP_filter}	–	0.5	–	MHz

1 T_J: Junction Temperature

2 T_A: Ambient Temperature

P.24 0x0150-0x0157 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0148-0x014F	Reserved	R	0	0	0	0	0	0	0	0
		W								

P.25 0x0150-0x0157 Low Side Drivers (LSDRV)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0150	LSDR	R	0	0	0	0	0	0	LSDR1	LSDR0
		W								
0x0151	LSCR	R	0	0	0	0	LSOLE1	LSOLE0	LSE1	LSE0
		W								
0x0152	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0153	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0154	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0155	LSSR	R	0	0	0	0	0	0	LSOL1	LSOL0
		W								
0x0156	LSIE	R	LSOCIE	0	0	0	0	0	0	0
		W								
0x0157	LSIF	R	0	0	0	0	0	0	LSOCIF1	LSOCIF0
		W								

P.26 0x0158-0x015F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x058-0x015F	Reserved	R	0	0	0	0	0	0	0	0
		W								

P.27 0x0160-0x0167 LIN Physical Layer (LINPHY)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0160	LPDR	R	0	0	0	0	0	0	LPDR1	LPDR0
		W								
0x0161	LPCR	R	0	0	0	0	LPE	RXONLY	LPWUE	LPPUE
		W								
0x0162	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0163	LPSLRM	R	LPDTDIS	0	0	0	0	0	LPSLR1	LPSLR0
		W								