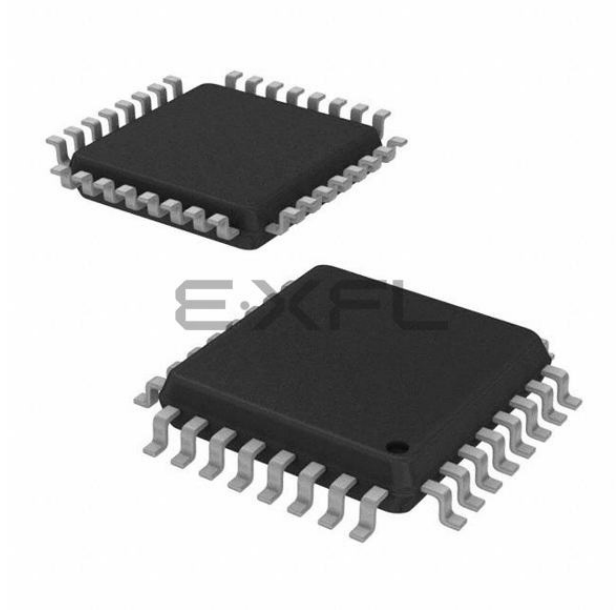

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Product Status	Active
Core Processor	12V1
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Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vr48af0clc

Chapter 1
Device Overview MC9S12VR-Family

Revision History

Version Number	Revision Date	Description of Changes
Rev 3.4	30-January-2014	• Corrected Figure 1-4 32LQFP pinout pin 5
Rev 4.0 Initial Draft	3-February-2014	• Added MC9S12VR16 & MC9S12VR32 to Table 1-1 • Added MC9S12VR16 & MC9S12VR32 maskset N11N to Table 1-3 • Added CPMU differences between masksets N11N & N59H
Draft A	2-April-2014	• Added 32QFN package
Draft B	24-February-2015	• Included feedback from shared review

1.1 Introduction

The MC9S12VR-Family is an optimized automotive 16-bit microcontroller product line focused on low-cost, high-performance, and low pin-count. This family integrates an S12 microcontroller with a LIN Physical interface, a 5V regulator system to supply the microcontroller, and analog blocks to control other elements of the system which operate at vehicle battery level (e.g. relay drivers, high-side driver outputs, wake up inputs). The MC9S12VR-Family is targeted at generic automotive applications requiring single node LIN communications. Typical examples of these applications include window lift modules, seat modules and sun-roof modules to name a few.

The MC9S12VR-Family uses many of the same features found on the MC9S12G family, including error correction code (ECC) on flash memory, EEPROM for diagnostic or data storage, a fast analog-to-digital converter (ADC) and a frequency modulated phase locked loop (IPLL) that improves the EMC performance. The MC9S12VR-Family delivers an optimized solution with the integration of several key system components into a single device, optimizing system architecture and achieving significant space savings. The MC9S12VR-Family delivers all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of NXP's existing 8-bit and 16-bit MCU families. Like the MC9S12XS family, the MC9S12VR-Family runs 16-bit wide accesses without wait states for all peripherals and memories. Misaligned single cycle 16-bit RAM access is not supported. The MC9S12VR-Family is available in 32-pin and 48-pin LQFP. In addition to the I/O ports available in each module, further I/O ports are available with interrupt capability allowing wake-up from stop or wait modes.

The MC9S12VR-Family is a general-purpose family of devices created with relay based motor control in mind and is suitable for a range of applications, including:

- Window lift modules
- Door modules
- Seat controllers

1.7.2 Detailed Signal Descriptions

This section describes the signal properties.

1.7.2.1 $\overline{\text{RESET}}$ — External Reset Signal

The $\overline{\text{RESET}}$ signal is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The $\overline{\text{RESET}}$ pin has an internal pull-up device.

1.7.2.2 TEST — Test Pin

This input only pin is reserved for factory test. This pin has an internal pull-down device.

NOTE

The TEST pin must be tied to ground in all applications.

1.7.2.3 BKGD / MODC — Background Debug Signal

The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has an internal pull-up device.

1.7.2.4 PAD[5:0] / KWAD[5:0] — Port AD Input Signals of ADC

PAD[5:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wake-up capability (KWAD[5:0]).These signals can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull devices are disabled.

1.7.2.5 PE[1:0] — Port E I/O Signals

PE[1:0] are general-purpose input or output signals. The signals can have pull-down device, enabled by a single control bit for this signal group. Out of reset the pull-down devices are enabled.

1.7.2.6 PP[5:0] / KWP[5:0] — Port P I/O Signals

PP[5:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wake-up capability (KWP[5:0]). PP[2] has a high current drive strength and an over-current interrupt feature. They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull devices are disabled.

1.7.2.7 PS[5:0] — Port S I/O Signals

PS[5:0] are general-purpose input or output signals. They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull-up devices are enabled.

1.11.5 Flash IFR Mapping

Table 1-13. Flash IFR Mapping

IFR Byte Address	Target															
	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0x405A - 0x405B							ADC Bandgap Reference[1]									
0x40B8 - 0x40B9			ACLKTR[5:0][2]										HTTR[3:0][3]			
0x40BA - 0x40BB		TCTRIM[4:0][4]					IRCTRIM[9:0][4]									

1 see Section 1.12.1 ADC Calibration

2 see Section 4.3.2.16 Autonomous Clock Trimming Register (CPMUACLKTR)

3 see Section 4.3.2.19 High Temperature Trimming Register (CPMUHTTR)

4 see Section 4.3.2.20 S12CPMU_UHV_V8 IRC1M Trim Registers (CPMUIRCTRIMH / CPMUIRCTRIML)

1.11.6 ADC External Trigger Input Connection

The ADC module includes external trigger inputs ETRIG0, ETRIG1, ETRIG2, and ETRIG3. The external trigger allows the user to synchronize ADC conversion to external trigger events. On MC9S12VR64/48 ETRIG0 is connected to PP0 / PWM0 and ETRIG1 is connected to PP1 / PWM1. ETRIG2 and ETRIG3 are not used. ETRIG0 can be routed to PS2 and ETRIG1 can be routed to PS3. On MC9S12VR32/16 ETRIG0 is connected to PS2 and ETRIG1 is connected to PS3.

1.11.7 ADC Special Conversion Channels

Whenever the ADC's Special Channel Conversion Bit (SC) in 8.3.2.6 ATD Control Register 5 (ATDCTL5) is set, it is capable of running conversion on a number of internal channels. Table 1-14 lists the internal sources which are connected to these special conversion channels.

Table 2-9. IRQCR Register Field Descriptions

Field	Description
7 IRQE	**IRQ select Edge sensitive only** — 1 $\overline{\text{IRQ}}$ pin configured to respond only to falling edges. Falling edges on the $\overline{\text{IRQ}}$ pin will be detected anytime IRQE=1 and will be cleared only upon a reset or the servicing of the $\overline{\text{IRQ}}$ interrupt. 0 $\overline{\text{IRQ}}$ pin configured for low level recognition
6 IRQEN	**IRQ ENable** — 1 $\overline{\text{IRQ}}$ pin is connected to interrupt logic 0 $\overline{\text{IRQ}}$ pin is disconnected from interrupt logic

2.3.9 Reserved Register

Address 0x001E (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-7. Reserved Register

[1] Read: Anytime
Write:Never

2.3.10 Reserved Register

Address 0x001F Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 2-8. Reserved Register

[1] Read: Anytime
Write: Only in special mode

NOTE

These reserved registers are designed for factory test purposes only and are not intended for general user access. Writing to these registers when in special modes can alter the module's functionality.

[1] Read: Anytime
Write: Once in normal, anytime in special mode

Table 2-15. Module Routing Register 0 Field Descriptions

Field	Description
7-6 MODRR0	**MODule Routing Register 0** — HS1 This register controls the routing of PWM and TIM channels to pin HS1 of HSDRV module. By default the pin is controlled by the related HSDRV port register bit. 11 PWM channel 1 routed to HS1 if enabled 10 PWM channel 4 routed to HS1 if enabled 01 TIM output compare channel 3 routed to HS1 if enabled 00 HS1 controlled by register bit HSDR[HSDR1]. Refer to HSDRV section.
5-4 MODRR0	**MODule Routing Register 0** — HS0 This register controls the routing of PWM and TIM channels to pin HS0 of HSDRV module. By default the pin is controlled by the related HSDRV port register bit. 11 PWM channel 3 routed to HS0 if enabled 10 PWM channel 3 routed to HS0 if enabled 01 TIM output compare channel 2 routed to HS0 if enabled 00 HS0 controlled by register bit HSDR[HSDR0]. Refer to HSDRV section.
3-2 MODRR0	**MODule Routing Register 0** — LS1 This register controls the routing of PWM and TIM channels to pin LS1 of LSDRV module. By default the pin is controlled by the related LSDRV port register bit. 11 PWM channel 7 routed to LS1 if enabled 10 PWM channel 7 routed to LS1 if enabled 01 TIM output compare channel 1 routed to LS1 if enabled 00 LS1 controlled by register bit LSDR[LSDR1]. Refer to LSDRV section.
1-0 MODRR0	**MODule Routing Register 0** — LS0 This register controls the routing of PWM and TIM channels to pin LS0 of LSDRV module. By default the pin is controlled by the related LSDRV port register bit. 11 PWM channel 5 routed to LS0 if enabled 10 PWM channel 6 routed to LS0 if enabled 01 TIM output compare channel 0 routed to LS0 if enabled 00 LS0 controlled by register bit LSDR[LSDR0]. Refer to LSDRV section.

2.3.21 Port S Data Direction Register (DDRS)

Address 0x024A (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-22. Port S Data Direction Register (DDRS - S12VR64/48)

1 Read: Anytime
Write: Anytime

Address 0x024A (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	DDRS3	DDRS2	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-23. Port S Data Direction Register (DDRS - S12VR32/16)

1 Read: Anytime
Write: Anytime

Table 2-19. DDRS Register Field Descriptions

Field	Description
5 DDRS	**Data Direction Register port S —** This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
4 DDRS	**Data Direction Register port S —** This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. In this case the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
3 DDRS	**Data Direction Register port S —** This bit determines whether the associated pin is an input or output. The ECLK output function, routed SCI1 and routed PWM function forces the I/O state to output if enabled. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. In these cases the data direction bit will not change. The routed ETRIG function has no effect on the I/O state. 1 Associated pin is configured as output 0 Associated pin is configured as input

4.4.6 System Clock Configurations

4.4.6.1 PLL Engaged Internal Mode (PEI)

This mode is the default mode after System Reset or Power-On Reset.

The Bus Clock is based on the PLLCLK, the reference clock for the PLL is internally generated (IRC1M). The PLL is configured to 50 MHz VCOCLK with POSTDIV set to 0x03. If locked (LOCK=1) this results in a PLLCLK of 12.5 MHz and a Bus Clock of 6.25 MHz. The PLL can be re-configured to other bus frequencies.

The clock sources for COP and RTI can be based on the internal reference clock generator (IRC1M) or the RC-Oscillator (ACLK).

4.4.6.2 PLL Engaged External Mode (PEE)

In this mode, the Bus Clock is based on the PLLCLK as well (like PEI). The reference clock for the PLL is based on the external oscillator.

The clock sources for COP and RTI can be based on the internal reference clock generator or on the external oscillator clock or the RC-Oscillator (ACLK).

This mode can be entered from default mode PEI by performing the following steps:

1. Configure the PLL for desired bus frequency.
2. Enable the external Oscillator (OSCE bit).
3. Wait for oscillator to start-up and the PLL being locked (LOCK = 1) and (UPOSC =1).
4. Clear all flags in the CPMUFLG register to be able to detect any future status bit change.
5. Optionally status interrupts can be enabled (CPMUINT register).

Loosing PLL lock status (LOCK=0) means loosing the oscillator status information as well (UPOSC=0).

The impact of loosing the oscillator status (UPOSC=0) in PEE mode is as follows:

- The PLLCLK is derived from the VCO clock (with its actual frequency) divided by four until the PLL locks again.

Application software needs to be prepared to deal with the impact of loosing the oscillator status at any time.

8.2 Signal Description

This section lists all inputs to the ADC12B6CV2 block.

8.2.1 Detailed Signal Descriptions

8.2.1.1 AN*x* (*x* = 5, 4, 3, 2, 1, 0)

This pin serves as the analog input Channel *x*. It can also be configured as digital port or external trigger for the ATD conversion.

8.2.1.2 ETRIG3, ETRIG2, ETRIG1, ETRIG0

These inputs can be configured to serve as an external trigger for the ATD conversion.

Refer to device specification for availability and connectivity of these inputs!

8.2.1.3 VRH, VRL

VRH is the high reference voltage, VRL is the low reference voltage for ATD conversion.

8.2.1.4 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ADC12B6CV2 block.

8.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC12B6CV2.

8.3.1 Module Memory Map

Figure 8-2 gives an overview on all ADC12B6CV2 registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ATDCTL0	R	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
		W								
0x0001	ATDCTL1	R	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
		W								
0x0002	ATDCTL2	R	0	AFFC	Reserved	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ACMPIE
		W								

= Unimplemented or Reserved

Figure 8-2. ADC12B6CV2 Register Summary (Sheet 1 of 2)

Table 9-10. PWMCTL Field Descriptions (continued)

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
5 CON23	**Concatenate Channels 2 and 3** 0 Channels 2 and 3 are separate 8-bit PWMs. 1 Channels 2 and 3 are concatenated to create one 16-bit PWM channel. Channel 2 becomes the high order byte and channel 3 becomes the low order byte. Channel 3 output pin is used as the output for this 16-bit PWM (bit 3 of port PWMP). Channel 3 clock select control-bit determines the clock source, channel 3 polarity bit determines the polarity, channel 3 enable bit enables the output and channel 3 center aligned enable bit determines the output mode.
4 CON01	**Concatenate Channels 0 and 1** 0 Channels 0 and 1 are separate 8-bit PWMs. 1 Channels 0 and 1 are concatenated to create one 16-bit PWM channel. Channel 0 becomes the high order byte and channel 1 becomes the low order byte. Channel 1 output pin is used as the output for this 16-bit PWM (bit 1 of port PWMP). Channel 1 clock select control-bit determines the clock source, channel 1 polarity bit determines the polarity, channel 1 enable bit enables the output and channel 1 center aligned enable bit determines the output mode.
3 PSWAI	**PWM Stops in Wait Mode —** Enabling this bit allows for lower power consumption in wait mode by disabling the input clock to the prescaler. 0 Allow the clock to the prescaler to continue while in wait mode. 1 Stop the input clock to the prescaler whenever the MCU is in wait mode.
2 PFRZ	**PWM Counters Stop in Freeze Mode** — In freeze mode, there is an option to disable the input clock to the prescaler by setting the PFRZ bit in the PWMCTL register. If this bit is set, whenever the MCU is in freeze mode, the input clock to the prescaler is disabled. This feature is useful during emulation as it allows the PWM function to be suspended. In this way, the counters of the PWM can be stopped while in freeze mode so that once normal program flow is continued, the counters are re-enabled to simulate real-time operations. Since the registers can still be accessed in this mode, to re-enable the prescaler clock, either disable the PFRZ bit or exit freeze mode. 0 Allow PWM to continue while in freeze mode. 1 Disable PWM input clock to the prescaler whenever the part is in freeze mode. This is useful for emulation.

9.3.2.7 PWM Clock A/B Select Register (PWMCLKAB)

Each PWM channel has a choice of four clocks to use as the clock source for that channel as described below.

	7	6	5	4	3	2	1	0
R W	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
Reset	0	0	0	0	0	0	0	0

Figure 9-9. PWM Clock Select Register (PWMCLK)

Read: Anytime

Write: Anytime

NOTE

Register bits PCLKAB0 to PCLKAB7 can be written anytime. If a clock select is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Figure 10-17 shows two cases of break detect. In trace RXD_1 the break symbol starts with the start bit, while in RXD_2 the break starts in the middle of a transmission. If BRKDFE = 1, in RXD_1 case there will be no byte transferred to the receive buffer and the RDRF flag will not be modified. Also no framing error or parity error will be flagged from this transfer. In RXD_2 case, however the break signal starts later during the transmission. At the expected stop bit position the byte received so far will be transferred to the receive buffer, the receive data register full flag will be set, a framing error and if enabled and appropriate a parity error will be set. Once the break is detected the BRKDIF flag will be set.

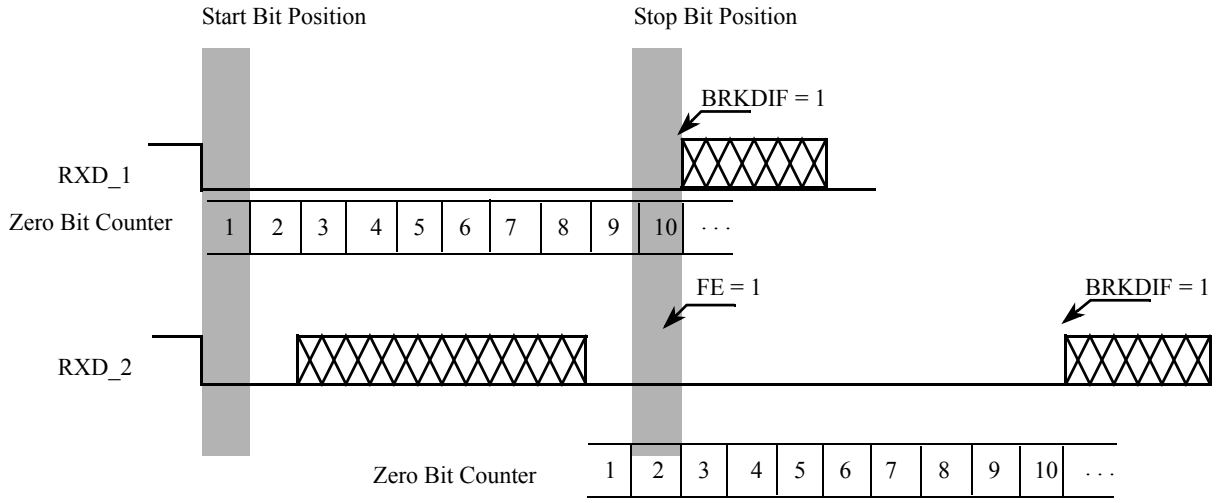

Figure 10-17. Break Detection if BRKDFE = 1 (M = 0)

10.4.5.4 Idle Characters

An idle character (or preamble) contains all logic 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in SCI control register 1 (SCICR1). The preamble is a synchronizing idle character that begins the first transmission initiated after writing the TE bit from 0 to 1.

If the TE bit is cleared during a transmission, the TXD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle character to be sent after the frame currently being transmitted.

NOTE

When queueing an idle character, return the TE bit to logic 1 before the stop bit of the current frame shifts out through the TXD pin. Setting TE after the stop bit appears on TXD causes data previously written to the SCI data register to be lost. Toggle the TE bit for a queued idle character while the TDRE flag is set and immediately before writing the next byte to the SCI data register.

If the TE bit is clear and the transmission is complete, the SCI is not the master of the TXD pin

10.4.6 Receiver

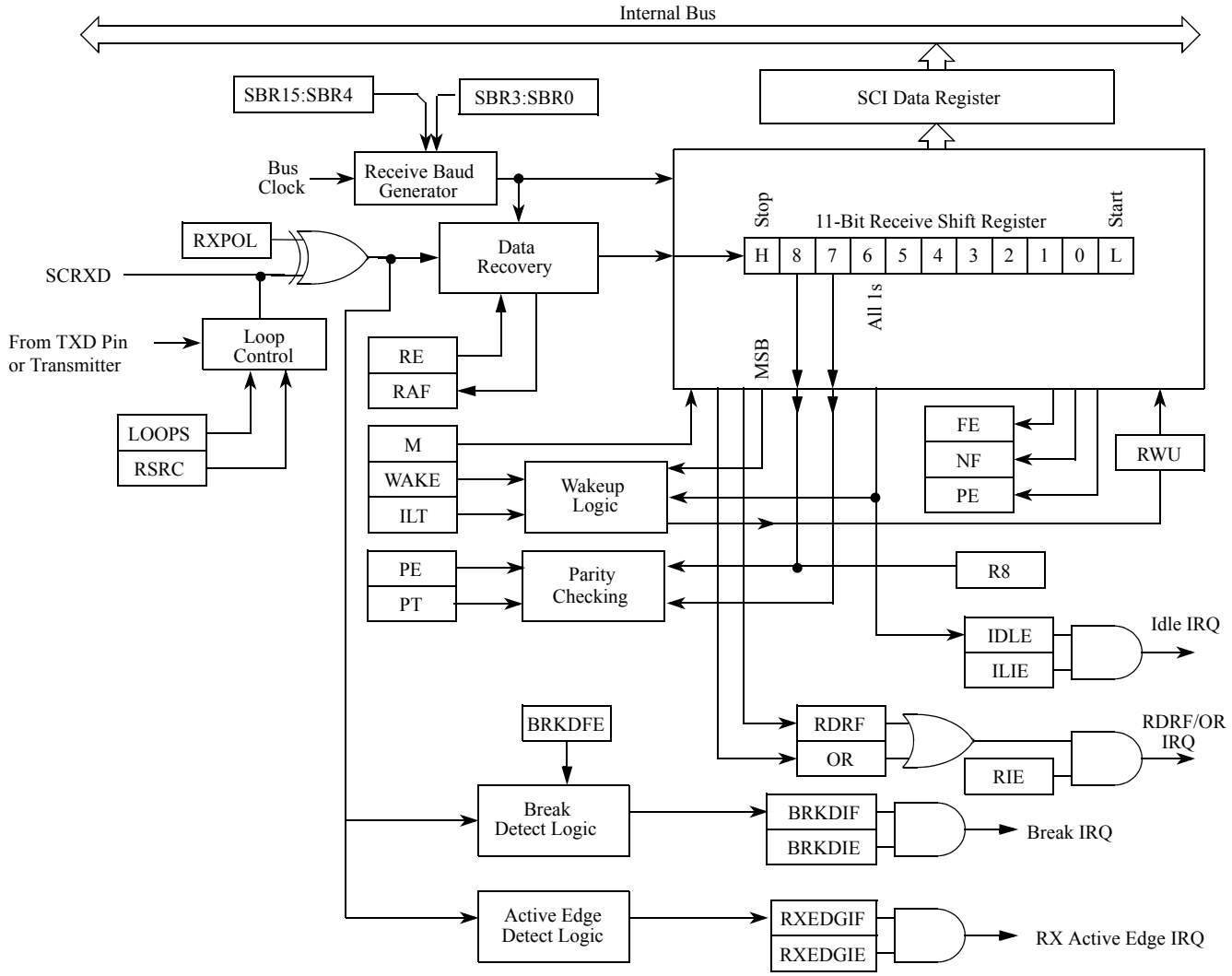

Figure 10-20. SCI Receiver Block Diagram

10.4.6.1 Receiver Character Length

The SCI receiver can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When receiving 9-bit data, bit R8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

10.4.6.2 Character Reception

During an SCI reception, the receive shift register shifts a frame in from the RXD pin. The SCI data register is the read-only buffer between the internal data bus and the receive shift register.

After a complete frame shifts into the receive shift register, the data portion of the frame transfers to the SCI data register. The receive data register full flag, RDRF, in SCI status register 1 (SCISR1) becomes set,

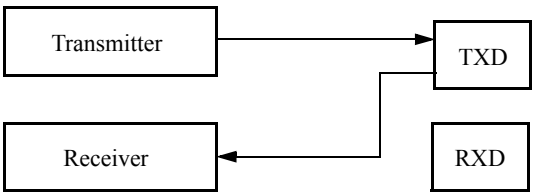

Figure 10-30. Single-Wire Operation (LOOPS = 1, RSRC = 1)

Enable single-wire operation by setting the LOOPS bit and the receiver source bit, RSRC, in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Setting the RSRC bit connects the TXD pin to the receiver. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).The TXDIR bit (SCISR2[1]) determines whether the TXD pin is going to be used as an input (TXDIR = 0) or an output (TXDIR = 1) in this mode of operation.

NOTE

In single-wire operation data from the TXD pin is inverted if RXPOL is set.

10.4.8 Loop Operation

In loop operation the transmitter output goes to the receiver input. The RXD pin is disconnected from the SCI.

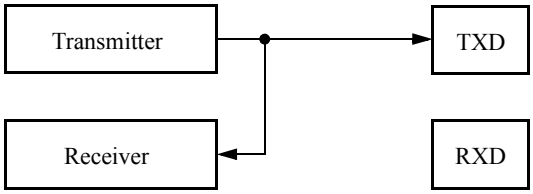

Figure 10-31. Loop Operation (LOOPS = 1, RSRC = 0)

Enable loop operation by setting the LOOPS bit and clearing the RSRC bit in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Clearing the RSRC bit connects the transmitter output to the receiver input. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).

NOTE

In loop operation data from the transmitter is not recognized by the receiver if RXPOL and TXPOL are not the same.

10.5 Initialization/Application Information

10.5.1 Reset Initialization

See Section 10.3.2, “Register Descriptions”.

Chapter 15
Low-Side Drivers - LSDRV (S12LSDRV1)

Table 15-1. Revision History Table

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V1.01	22 February 2011	All	- Added clarification to open-load mechanism in over-current conditions
V1.02	12 April 2011	All	- improved clarification to open-load mechanism in over-current conditions - corrected typos
V1.03	3 April 2011	Register Descriptions for LSDR and LSCR	- added Note on considering settling time $t_{LS\_settling}$ to LSDR and LSCR register description - added Note on how to disable the low-side driver to LSDR register description
V1.04	29 January 2013	All	- Cleaning

15.1 Introduction

The LSDRV module provides two low-side drivers typically used to drive inductive loads (relays).

15.1.1 Features

The LSDRV module includes two independent low side drivers with common current sink. Each driver has the following features:

- Selectable driver control of low-side switches: LSDRx register bits, PWM or timer channels. See PIM chapter for routing options.
- Open-load detection while enabled
  - While driver off: selectable high-load resistance open-load detection
- Over-current protection with shutdown and interrupt while enabled
- Active clamp to protect the device against over-voltage when the power transistor that is driving an inductive load (relay) is turned off.

15.1.2 Modes of Operation

The LSDRV module behaves as follows in the system operating modes:

1. MCU run mode

Table 15-3. Register Summary

Address Offset Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0003 Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	W								
0x0004 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0005 LSSR	R	0	0	0	0	0	0	LSOL1	LSOL0
	W								
0x0006 LSIE	R	LSOCIE	0	0	0	0	0	0	0
	W								
0x0007 LSIF	R	0	0	0	0	0	0	LSOCIF1	LSOCIF0
	W								

Table 15-9. LSDRV Interrupt Sources

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
LSDRV Interrupt (LSI)	LSDRV Over-Current Interrupt (LSOCI)	LSOCIE=1

15.4.4.1 LSDRV Over Current Interrupt (LSOCI)

If a low-side driver over-current event is detected the related interrupt flag LSOCIFx asserts. Depending on the setting of the LSDRV Error Interrupt Enable (LSOCIE) bit an interrupt is requested.

16.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the LIN Physical Layer.

16.3.1 Module Memory Map

A summary of the registers associated with the LIN Physical Layer module is shown in Table 16-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset / Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 LPDR	R	0	0	0	0	0	0	LPDR1	LPDR0
	W								
0x0001 LPCR	R	0	0	0	0	LPE	RXONLY	LPWUE	LPPUE
	W								
0x0002 Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	W								
0x0003 LPSLRM	R	LPDTDIS	0	0	0	0	0	LPSLR1	LPSLR0
	W								
0x0004 Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	W								
0x0005 LPSR	R	LPDT	0	0	0	0	0	0	0
	W								
0x0006 LPIE	R	LPDTIE	LPOCIE	0	0	0	0	0	0
	W								
0x0007 LPIF	R	LPDTIF	LPOCIF	0	0	0	0	0	0
	W								

Figure 16-2. Register Summary

Table 18-24. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)
100	HI	Data 2 [15:8]
	LO	Data 2 [7:0]
101	HI	Data 3 [15:8]
	LO	Data 3 [7:0]

18.3.2.12 Flash Reserved1 Register (FRSV1)

This Flash register is reserved for factory testing.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-17. Flash Reserved1 Register (FRSV1)

All bits in the FRSV1 register read 0 and are not writable.

18.3.2.13 Flash Reserved2 Register (FRSV2)

This Flash register is reserved for factory testing.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-18. Flash Reserved2 Register (FRSV2)

All bits in the FRSV2 register read 0 and are not writable.

18.3.2.14 Flash Reserved3 Register (FRSV3)

This Flash register is reserved for factory testing.

18.4.7.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the DFDIF and SFDIF flags in combination with the DFDIE and SFDIE interrupt enable bits to generate the Flash error interrupt request. For a detailed description of the register bits involved, refer to Section 18.3.2.5, “Flash Configuration Register (FCNFG)”, Section 18.3.2.6, “Flash Error Configuration Register (FERCNFG)”, Section 18.3.2.7, “Flash Status Register (FSTAT)”, and Section 18.3.2.8, “Flash Error Status Register (FERSTAT)”.

The logic used for generating the Flash module interrupts is shown in Figure 18-26.

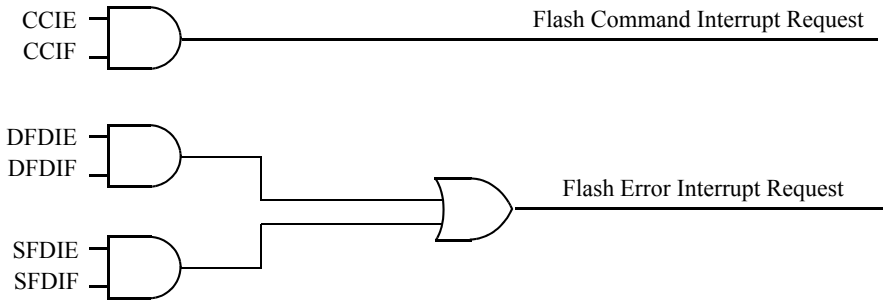

Figure 18-26. Flash Module Interrupts Implementation

18.4.8 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 18.4.7, “Interrupts”).

18.4.9 Stop Mode

If a Flash command is active (CCIF = 0) when the MCU requests stop mode, the current Flash operation will be completed before the MCU is allowed to enter stop mode.

18.5 Security

The Flash module provides security information to the MCU. The Flash security state is defined by the SEC bits of the FSEC register (see Table 18-11). During reset, the Flash module initializes the FSEC register using data read from the security byte of the Flash configuration field at global address 0x3_FF0F. The security state out of reset can be permanently changed by programming the security byte assuming that the MCU is starting from a mode where the necessary P-Flash erase and program commands are available and that the upper region of the P-Flash is unprotected. If the Flash security byte is successfully programmed, its new value will take affect after the next MCU reset.

Table 19-5. Program IFR Fields

Global Address	Size (Bytes)	Field Description
0x0_4000 – 0x0_4007	8	Reserved
0x0_4008 – 0x0_40B5	174	Reserved
0x0_40B6 – 0x0_40B7	2	Version ID[1]
0x0_40B8 – 0x0_40BF	8	Reserved
0x0_40C0 – 0x0_40FF	64	Program Once Field Refer to Section 19.4.6.6, “Program Once Command”

1 Used to track firmware patch versions, see Section 19.4.2 IFR Version ID Word

Table 19-6. Memory Controller Resource Fields (NVMRES[1]=1)

Global Address	Size (Bytes)	Description
0x0_4000 – 0x0_40FF	256	P-Flash IFR (see Table 19-5)
0x0_4100 – 0x0_41FF	256	Reserved.
0x0_4200 – 0x0_57FF		Reserved
0x0_5800 – 0x0_59FF	512	Reserved
0x0_5A00 – 0x0_5FFF	1,536	Reserved
0x0_6000 – 0x0_6BFF	3,072	Reserved
0x0_6C00 – 0x0_7FFF	5,120	Reserved

1 NVMRES - See Section 19.4.3 Internal NVM resource (NVMRES) for NVMRES (NVM Resource) detail.

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation P_D can be calculated from the equation below. Table A-6 below lists the power dissipation components . **Figure A-2.** gives an overview of the supply currents.

$$P_D = P_{INT} + P_{HS} + P_{LS} + P_{LIN} + P_{SENSE} + P_{HVI} - P_{EVDD} - P_{GPIO}$$

Table A-6. Power Dissipation Components

Power Component	Description
$P_{INT} = V_{SUP} I_{SUP}$	Internal Power for LQFP 48 Package with seperate VSUP and VSUPHS pins.
$P_{INT} = V_{SUP} (I_{SUP} - I_{PHS0/1})$	Internal Power for LQFP 32 Package with single VSUP pin which is double bonded to VSUP pad and VSUPHS pad.
$P_{HS} = I_{PHS0/1}^2 R_{DSONHS0/1}$	Power dissipation of High-side drivers
$P_{LS} = I_{PLS0/1}^2 R_{DSONLS0/1}$	Power dissipation of Low-side drivers
$P_{LIN} = V_{LIN} I_{LIN}$	Power dissipation of LINPHY
$P_{SENSE} = V_{SENSE} I_{SENSE}$	Power dissipation of Battery Sensor
$P_{HVI} = V_{HVI} I_{HVI}$	Power dissipation of High Voltage Inputs
$P_{EVDD} = V_{DDX} I_{EVDD}$	Power dissipation of external load driven by EVDD. (see **Figure A-2.**) This component is included in P_{INT} and is subtracted from overall MCU power dissipation P_D
$P_{GPIO} = V_{I/O} I_{I/O}$	Power dissipation of external load driven by GPIO Port.(see **Figure A-2.**) Assuming the load is connected between GPIO and ground. This power component is included in P_{INT} and is subtracted from overall MCU power dissipation P_D