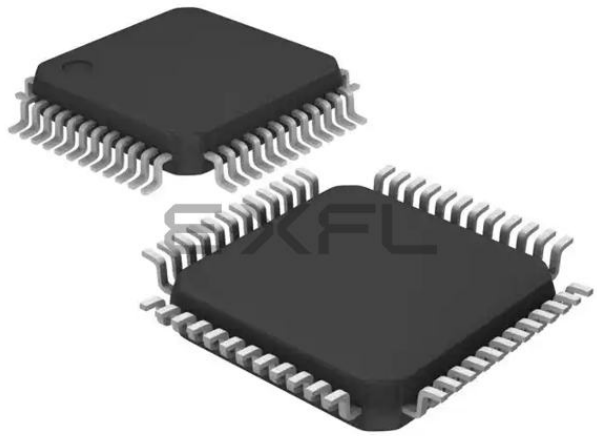

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Details	
Product Status	Active
Core Processor	12V1
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Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vr48af0clfr

— Power-on reset (POR) circuit
— Low-voltage reset (LVR)

1.4.17 Low-side drivers (LSDRV)

- 2x low-side drivers targeted for up to approximately 150mA current capability.
- Internal timer or PWM channels can be routed to control the low-side drivers
- Open-load detection
- Over-current protection with shutdown and interrupt
- Active clamp (for driving relays)
- Recirculation detection

1.4.18 High-side drivers (HSDRV)

- 2 High-side drivers targeted for up to approximately 50mA current capability
- Internal timer or PWM channels can be routed to control the high-side drivers
- Over-current protection with shutdown and interrupt
- Slew rate control on MC9S12VR32/16 (maskset N11N)

1.4.19 Background Debug (BDM)

- Background debug module (BDM) with single-wire interface
  — Non-intrusive memory access commands
  — Supports in-circuit programming of on-chip nonvolatile memory

1.4.20 Debugger (DBG)

- Trace buffer with depth of 64 entries
- Three comparators (A, B and C)
  — Access address comparisons with optional data comparisons
  — Program counter comparisons
  — Exact address or address range comparisons
- Two types of comparator matches
  — Tagged This matches just before a specific instruction begins execution
  — Force This is valid on the first instruction boundary after a match occurs
- Four trace modes
- Four stage state sequencer

1.7.3.6 VSUP — Voltage Supply Pin for Voltage Regulator

VSUP is the 12V/18V shared supply voltage pin for the on chip voltage regulator.

1.7.3.7 VSUPHS — Voltage Supply Pin for High-Side Drivers

VSUPHS is the 12V/18V shared supply voltage pin for the high-side drivers.

1.7.3.8 Power and Ground Connection Summary

Table 1-6. Power and Ground Connection Summary

Mnemonic	Nominal Voltage	Description
VSS	0V	Ground pin for 1.8V core supply voltage generated by on chip voltage regulator
VDDX1	5.0 V	5V power supply output for I/O drivers generated by on chip voltage regulator
VSSX1	0V	Ground pin for I/O drivers
VDDX2	5.0 V	5V power supply output for I/O drivers generated by on chip voltage regulator
VSSX2	0V	Ground pin for I/O drivers
VDDA	5.0 V	External power supply for the analog-to-digital converter and for the reference circuit of the internal voltage regulator
VSSA	0V	Ground pin for VDDA analog supply
LGND	0V	Ground pin for LIN physical
LSGND	0V	Ground pin for low-side driver
VSUP	12V/18V	External power supply for voltage regulator
VSUPHS	12V/18V	External power supply for high-side driver

1.7.4 Device Pinouts

MC9S12VR-Family is available in 48-pin package and 32-pin package. Signals in parentheses in **Figure 1-3.** and **Figure 1-4.** denote alternative module routing options.

Table 1-10. Interrupt Vector Locations (Sheet 3 of 3)

Vector Address	Interrupt Source	CCR Mask	Local Enable	Wake up from STOP	Wake up from WAIT
Vector base + $80	Spurious interrupt	—	None	-	-

1.10.3 Effects of Reset

When a reset occurs, MCU registers and control bits are initialized. Refer to the respective block sections for register reset states.

On each reset, the Flash module executes a reset sequence to load Flash configuration registers.

1.10.3.1 Flash Configuration Reset Sequence Phase

On each reset, the Flash module will hold CPU activity while loading Flash module registers from the Flash memory. If double faults are detected in the reset phase, Flash module protection and security may be active on leaving reset. This is explained in more detail in the Flash module Section 18.1, “Introduction”.

1.10.3.2 Reset While Flash Command Active

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed.

1.10.3.3 I/O Pins

Refer to the PIM section for reset configurations of all peripheral module ports.

1.10.3.4 RAM

The RAM arrays are not initialized out of reset.

1.11 Module Device level Dependencies

1.11.1 CPMU Differences between Maskset N59H (MC9S12VR64/48) and N11N (MC9S12VR32/16)

The following features described in the CPMU section (CPMU V8) are only available on Maskset N11N:

- Full swing pierce oscillator OSCMOD bit in CPMUOSC2 register. See Section 4.3.2.24 S12CPMU_UHV_V8 Oscillator Register 2 (CPMUOSC2)
- Oscillator clock monitor reset configuration OMRE bit in CPMUOSC2 register. See Section 4.3.2.24 S12CPMU_UHV_V8 Oscillator Register 2 (CPMUOSC2)
- PLL clock monitor reset PMRF flag in CPMUINT register. See Section 4.3.2.5 S12CPMU_UHV_V8 Interrupt Enable Register (CPMUINT)

2.3.41 Port AD Data Register (PT1AD)

Address 0x0271 (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PT1AD5	PT1AD4	PT1AD3	PT1AD2	PT1AD1	PT1AD0
W								
Altern. Function	—	—	AN5	AN4	AN3	AN2	AN1	AN0
Reset	0	0	0	0	0	0	0	0

Figure 2-56. Port AD Data Register (PT1AD - S12VR64/48)

[1] Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

Address 0x0271 (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PT1AD1	PT1AD0
W								
Altern. Function	—	—	—	—	—	—	AN1	AN0
Reset	0	0	0	0	0	0	0	0

Figure 2-57. Port AD Data Register (PT1AD - S12VR32/16)

[1] Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

Table 2-41. PT1AD Register Field Descriptions

Field	Description
5-0 PT1AD	**PorT data register 1 port AD** — General-purpose input/output data, ADC AN analog input When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit set to 1, a read returns the value of the port register bit. If the data direction bit is set to 0 and the ADC Digital Input Enable Register (ATDDIEN) is set to 1 the synchronized pin input state is read.

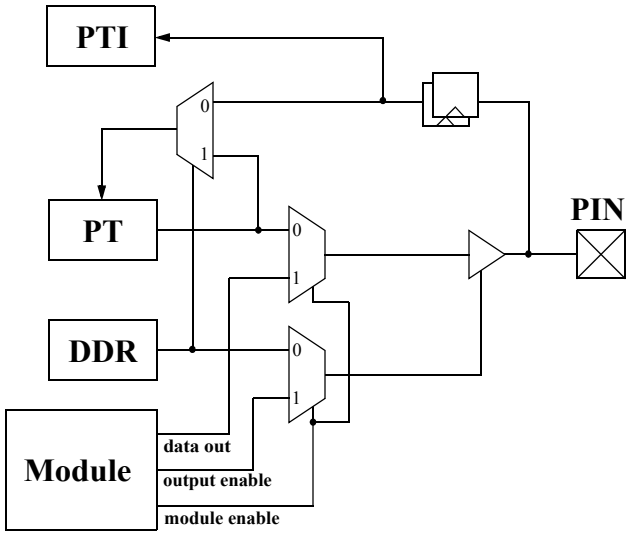

Figure 2-70. Illustration of I/O pin functionality

2.4.2.4 Reduced drive register (RDRx)

If the pin is used as an output this register allows the configuration of the drive strength independent of the use with a peripheral module.

2.4.2.5 Pull device enable register (PERx)

This register turns on a pullup or pulldown device on the related pins determined by the associated polarity select register (2.4.2.6/2-106).

The pull device becomes active only if the pin is used as an input or as a wired-or output. Some peripheral module only allow certain configurations of pull devices to become active. Refer to the respective bit descriptions.

2.4.2.6 Polarity select register (PPSx)

This register selects either a pullup or pulldown device if enabled.

It becomes only active if the pin is used as an input. A pullup device can be activated if the pin is used as a wired-or output.

2.4.2.7 Wired-or mode register (WOMx)

If the pin is used as an output this register turns off the active-high drive. This allows wired-or type connections of outputs.

3.4.4 Prioritization of Memory Accesses

On S12VR devices, the CPU and the BDM are not able to access the memory in parallel. An arbitration occurs whenever both modules attempt a memory access at the same time. CPU accesses are handled with higher priority than BDM accesses unless the BDM module has been stalled for more then 128 bus cycles. In this case the pending BDM access will be processed immediately.

3.4.5 Interrupts

The S12GMMC does not generate any interrupts.

4.2 Signal Description

This section lists and describes the signals that connect off chip as well as internal supply nodes and special signals.

4.2.1 $\overline{\text{RESET}}$

Pin $\overline{\text{RESET}}$ is an active-low bidirectional pin. As an input it initializes the MCU asynchronously to a known start-up state. As an open-drain output it indicates that an MCU-internal reset has been triggered.

4.2.2 EXTAL and XTAL

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. If XOSCLCP is enabled, the MCU internal OSCCLK_LCP is derived from the EXTAL input frequency. If OSCE=0, the EXTAL pin is pulled down by an internal resistor of approximately 200 kΩ and the XTAL pin is pulled down by an internal resistor of approximately 700 kΩ.

NOTE

NXP recommends an evaluation of the application board and chosen resonator or crystal by the resonator or crystal supplier.
The loop controlled circuit (XOSCLCP) is not suited for overtone resonators and crystals.

4.2.3 VSUP — Regulator Power Input Pin

Pin VSUP is the power input of VREGAUTO. All currents sourced into the regulator loads flow through this pin.

An appropriate reverse battery protection network consisting of a diode and capacitors is recommended.

4.2.4 VDDA, VSSA — Regulator Reference Supply Pins

Pins VDDA and VSSA are used to supply the analog parts of the regulator.
Internal precision reference circuits are supplied from these signals.

A local decoupling capacitor between VDDA and VSSA according to the electrical specification is required. Additionally a bigger tank capacitor is required on the 5 Volt supply network as well to ensure Voltage regulator stability.

VDDA has to be connected externally to VDDX.

4.2.5 VDDX, VSSX— Pad Supply Pins

This supply domain is monitored by the Low Voltage Reset circuit.

A local decoupling capacitor between VDDX and VSSX according to the electrical specification is required.

4.3 Memory Map and Registers

This section provides a detailed description of all registers accessible in the S12CPMU_UHV_V8.

4.3.1 Module Memory Map

The S12CPMU_UHV_V8 registers are shown in Figure 4-3.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0034	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0035	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0036	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0037	CPMUFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	OSCIF	UPOSC
		W								
0x0038	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	**PMRF**
		W								
0x0039	CPMUCLKS	R	PLLSEL	PSTP	CSAD	COP OSCSEL1	PRE	PCE	RTI OSCSEL	COP OSCSEL0
		W								
0x003A	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
0x003B	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x003C	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x003D	RESERVED CPMUTEST0	R	0	0	0	0	0	0	0	0
		W								
0x003E	RESERVED CPMUTEST1	R	0	0	0	0	0	0	0	0
		W								
0x003F	CPMU ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02F0	CPMU HTCTL	R	0	0	VSEL	0	HTE	HTDS	HTIE	HTIF
		W								
0x02F1	CPMU LVCTL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								
0x02F2	CPMU APICTL	R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
		W								
			= Unimplemented or Reserved							

Figure 4-3. CPMU Register Summary[1]

4.4.6.3 PLL Bypassed External Mode (PBE)

In this mode, the Bus Clock frequency is half the external oscillator clock. The reference clock for the PLL is based on the external oscillator.

The clock sources for COP and RTI can be based on the internal reference clock generator or on the external oscillator clock or the RC-Oscillator (ACLK).

This mode can be entered from default mode PEI by performing the following steps:

1. Make sure the PLL configuration is valid.
2. Enable the external Oscillator (OSCE bit)
3. Wait for the oscillator to start-up and the PLL being locked (LOCK = 1) and (UPOSC =1)
4. Clear all flags in the CPMUFLG register to be able to detect any status bit change.
5. Optionally status interrupts can be enabled (CPMUINT register).
6. Select the Oscillator clock as source of the Bus Clock (PLLSEL=0)

Loosing PLL lock status (LOCK=0) means loosing the oscillator status information as well (UPOSC=0).

The impact of loosing the oscillator status (UPOSC=0) in PBE mode is as follows:

- PLLSEL is set automatically and the Bus clock is switched back to the PLL clock.
- The PLLCLK is derived from the VCO clock (with its actual frequency) divided by four until the PLL locks again.

NOTEApplication software needs to be prepared to deal with the impact of loosing the oscillator status at any time.

When using the oscillator clock as system clock (write PLLSEL = 0) it is highly recommended to enable the oscillator clock monitor reset feature (write OMRE = 1 in CPMUOSC2 register). If the oscillator monitor reset feature is disabled (OMRE = 0) and the oscillator clock is used as system clock, the system might stall in case of loss of oscillation.

4.5 Resets

4.5.1 General

All reset sources are listed in Table 4-31. Refer to MCU specification for related vector addresses and priorities.

Table 4-31. Reset Summary

Reset Source	Local Enable
Power-On Reset (POR)	None
Low Voltage Reset (LVR)	None
External pin $\overline{\text{RESET}}$	None
Illegal Address Reset	None

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x3_FF09	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x3_FF0A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x3_FF0B	Reserved	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented, Reserved

= Implemented (do not alter)

X = Indeterminate

0 = Always read zero

Figure 5-2. BDM Register Summary (continued)

5.3.2.1 BDM Status Register (BDMSTS)

Register Global Address 0x3_FF01

	7	6	5	4	3	2	1	0
R	ENBDM	BDMACT	0	SDV	TRACE	0	UNSEC	0
W								
Reset								
Special Single-Chip Mode	0[1]	1	0	0	0	0	0[2]	0
All Other Modes	0	0	0	0	0	0	0	0

= Unimplemented, Reserved

= Implemented (do not alter)

0 = Always read zero

1 ENBDM is read as 1 by a debugging environment in special single chip mode when the device is not secured or secured but fully erased (Flash). This is because the ENBDM bit is set by the standard BDM firmware before a BDM command can be fully transmitted and executed.

2 UNSEC is read as 1 by a debugging environment in special single chip mode when the device is secured and fully erased, else it is 0 and can only be read if not secure (see also bit description).

Figure 5-3. BDM Status Register (BDMSTS)

Read: All modes through BDM operation when not secured

Write: All modes through BDM operation when not secured, but subject to the following:

— ENBDM should only be set via a BDM hardware command if the BDM firmware commands are needed. (This does not apply in special single chip mode).

— BDMACT can only be set by BDM hardware upon entry into BDM. It can only be cleared by the standard BDM firmware lookup table upon exit from BDM active mode.

— All other bits, while writable via BDM hardware or standard BDM firmware write commands, should only be altered by the BDM hardware or standard firmware lookup table as part of BDM command execution.

Hardware commands are used to read and write target system memory locations and to enter active background debug mode, see Section 5.4.3, “BDM Hardware Commands”. Target system memory includes all memory that is accessible by the CPU.

Firmware commands are used to read and write CPU resources and to exit from active background debug mode, see Section 5.4.4, “Standard BDM Firmware Commands”. The CPU resources referred to are the accumulator (D), X index register (X), Y index register (Y), stack pointer (SP), and program counter (PC).

Hardware commands can be executed at any time and in any mode excluding a few exceptions as highlighted (see Section 5.4.3, “BDM Hardware Commands”) and in secure mode (see Section 5.4.1, “Security”). BDM firmware commands can only be executed when the system is not secure and is in active background debug mode (BDM).

5.4.1 Security

If the user resets into special single chip mode with the system secured, a secured mode BDM firmware lookup table is brought into the map overlapping a portion of the standard BDM firmware lookup table. The secure BDM firmware verifies that the on-chip Flash EEPROM are erased. This being the case, the UNSEC and ENBDM bit will get set. The BDM program jumps to the start of the standard BDM firmware and the secured mode BDM firmware is turned off and all BDM commands are allowed. If the Flash does not verify as erased, the BDM firmware sets the ENBDM bit, without asserting UNSEC, and the firmware enters a loop. This causes the BDM hardware commands to become enabled, but does not enable the firmware commands. This allows the BDM hardware to be used to erase the Flash.

BDM operation is not possible in any other mode than special single chip mode when the device is secured. The device can only be unsecured via BDM serial interface in special single chip mode. More information regarding security is provided in the security section of the device documentation.

5.4.2 Enabling and Activating BDM

The system must be in active BDM to execute standard BDM firmware commands. BDM can be activated only after being enabled. BDM is enabled by setting the ENBDM bit in the BDM status (BDMSTS) register. The ENBDM bit is set by writing to the BDM status (BDMSTS) register, via the single-wire interface, using a hardware command such as WRITE_BD_BYTE.

After being enabled, BDM is activated by one of the following[1]:

- Hardware BACKGROUND command
- CPU BGND instruction
- Breakpoint force or tag mechanism[2]

When BDM is activated, the CPU finishes executing the current instruction and then begins executing the firmware in the standard BDM firmware lookup table. When BDM is activated by a breakpoint, the type of breakpoint used determines if BDM becomes active before or after execution of the next instruction.

1. BDM is enabled and active immediately out of special single-chip reset.
2. This method is provided by the S12S_DBG module.

or level sensitive with polarity control. Table 8-23 gives a brief description of the different combinations of control bits and their effect on the external trigger function.

In order to avoid maybe false trigger events please enable the external digital input via ATDDIEN register first and in the following enable the external trigger mode by bit ETRIGE.

Table 8-23. External Trigger Control Bits

ETRIGLE	ETRIGP	ETRIGE	SCAN	Description
X	X	0	0	Ignores external trigger. Performs one conversion sequence and stops.
X	X	0	1	Ignores external trigger. Performs continuous conversion sequences.
0	0	1	X	Trigger falling edge sensitive. Performs one conversion sequence per trigger.
0	1	1	X	Trigger rising edge sensitive. Performs one conversion sequence per trigger.
1	0	1	X	Trigger low level sensitive. Performs continuous conversions while trigger level is active.
1	1	1	X	Trigger high level sensitive. Performs continuous conversions while trigger level is active.

In either level or edge sensitive mode, the first conversion begins when the trigger is received.

Once ETRIGE is enabled a conversion must be triggered externally after writing to ATDCTL5 register.

During a conversion in edge sensitive mode, if additional trigger events are detected the overrun error flag ETORF is set.

If level sensitive mode is active and the external trigger de-asserts and later asserts again during a conversion sequence, this does not constitute an overrun. Therefore, the flag is not set. If the trigger is left active in level sensitive mode when a sequence is about to be complete, another sequence will be triggered immediately.

8.4.2.2 General-Purpose Digital Port Operation

Each ATD input pin can be switched between analog or digital input functionality. An analog multiplexer makes each ATD input pin selected as analog input available to the A/D converter.

The pad of the ATD input pin is always connected to the analog input channel of the analog mulitplexer.

Each pad input signal is buffered to the digital port register.

This buffer can be turned on or off with the ATDDIEN register for each ATD input pin.
This is important so that the buffer does not draw excess current when an ATD input pin is selected as analog input to the ADC12B6CV2.

PWMx Period = Channel Clock Period * PWMPERx

- Center Aligned Output (CAEx = 1)

  PWMx Period = Channel Clock Period * (2 * PWMPERx)

For boundary case programming values, please refer to Section 9.4.2.8, “PWM Boundary Cases”.

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	1	1	1	1	1	1	1	1

Figure 9-13. PWM Channel Period Registers (PWMPERx)

[1] This register is available only when the corresponding channel exists and is reserved if that channel does not exist. Writes to a reserved register have no functional effect. Reads from a reserved register return zeroes.

Read: Anytime

Write: Anytime

9.3.2.12 PWM Channel Duty Registers (PWMDTYx)

There is a dedicated duty register for each channel. The value in this register determines the duty of the associated PWM channel. The duty value is compared to the counter and if it is equal to the counter value a match occurs and the output changes state.

The duty registers for each channel are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to $00)
- The channel is disabled

In this way, the output of the PWM will always be either the old duty waveform or the new duty waveform, not some variation in between. If the channel is not enabled, then writes to the duty register will go directly to the latches as well as the buffer.

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active duty due to the double buffering scheme.

See Section 9.4.2.3, “PWM Period and Duty” for more information.

NOTE

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time. If the polarity bit is one, the output starts high and then goes low when the duty count is reached, so the duty registers contain a count of the high time. If the polarity bit is zero, the output starts low and then goes high when the duty count is reached, so the duty registers contain a count of the low time.

10.1.4 Block Diagram

Figure 10-1 is a high level block diagram of the SCI module, showing the interaction of various function blocks.

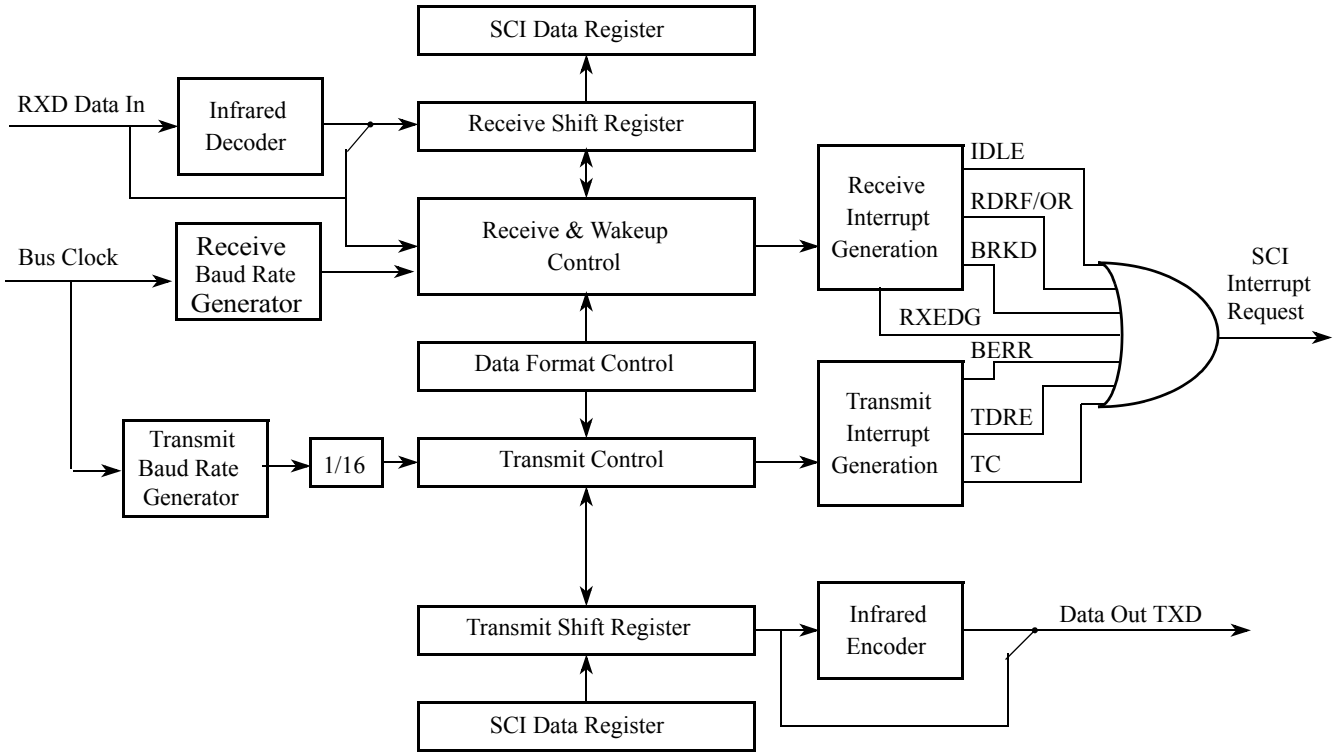

Figure 10-1. SCI Block Diagram

13.3.5 Reserved Register

Module Base + 0x0003 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

= Unimplemented

Figure 13-4. Reserved Register

[1] Read: Anytime
Write: Only in special mode

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special mode can alter the module's functionality.

Table 13-6. Reserved Register Field Descriptions

Field	Description
7-0 Reserved	These reserved bits are used for test purposes. Writing to these bits can alter the module functionality.

Address & Name		7	6	5	4	3	2	1	0
FRSV5	R	0	0	0	0	0	0	0	0
	W								
FRSV6	R	0	0	0	0	0	0	0	0
	W								
FRSV7	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Figure 18-3. FTMRG64K512 Register Summary (continued)

18.3.2.1 Flash Clock Divider Register (FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

	7	6	5	4	3	2	1	0
R	FDIVLD	FDIVLCK	FDIV[5:0]					
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-4. Flash Clock Divider Register (FCLKDIV)

All bits in the FCLKDIV register are readable, bit 7 is not writable, bit 6 is write-once-hi and controls the writability of the FDIV field in normal mode. In special mode, bits 6-0 are writable any number of times but bit 7 remains unwritable.

CAUTION

The FCLKDIV register should never be written while a Flash command is executing (CCIF=0).

Table 18-7. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	**Clock Divider Loaded** 0 FCLKDIV register has not been written since the last reset 1 FCLKDIV register has been written since the last reset

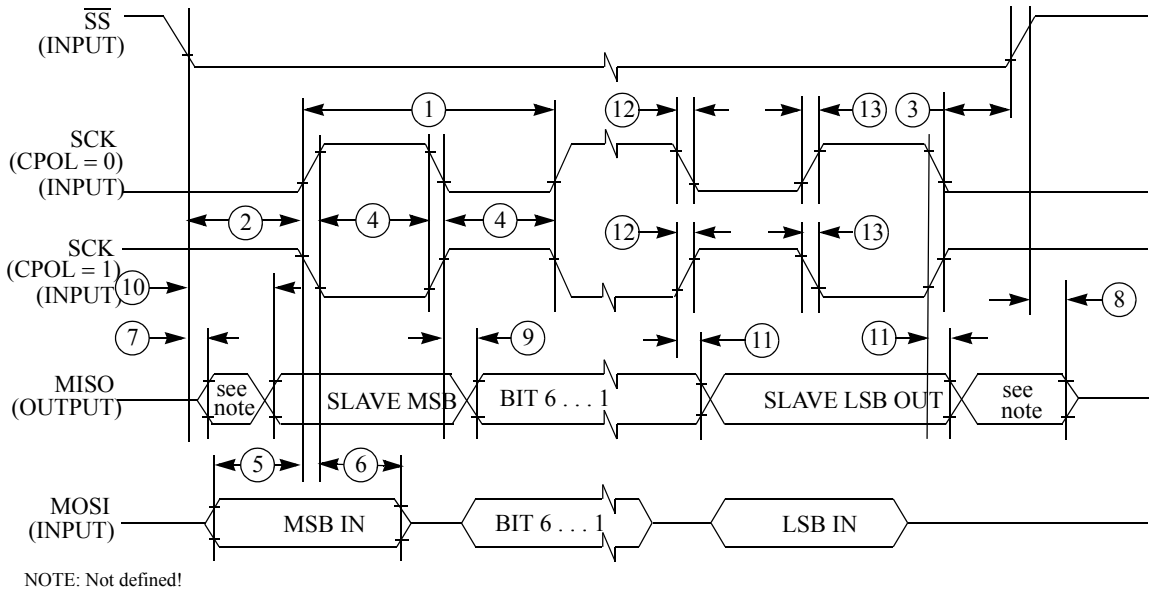

Figure K-4. SPI Slave Timing (CPHA=0)

In **Figure K-5.** the timing diagram for slave mode with transmission format CPHA=1 is depicted.

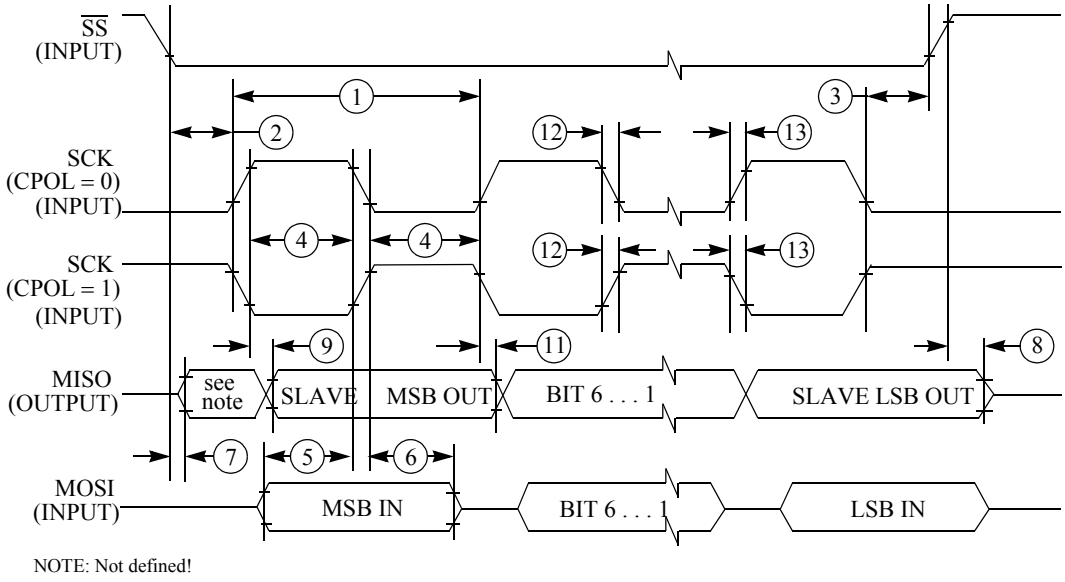

Figure K-5. SPI Slave Timing (CPHA=1)

In **Table K-3.** the timing characteristics for slave mode are listed.

Table K-3. SPI Slave Mode Timing Characteristics

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	SCK Frequency	f_{sck}	DC	—	1/4	f_{bus}
1	SCK Period	t_{sck}	4	—	∞	t_{bus}
2	Enable Lead Time	t_{lead}	4	—	—	t_{bus}
3	Enable Lag Time	t_{lag}	4	—	—	t_{bus}
4	Clock (SCK) High or Low Time	t_{wsck}	4	—	—	t_{bus}
5	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
7	Slave Access Time (time to data active)	t_a	—	—	20	ns
8	Slave MISO Disable Time	t_{dis}	—	—	22	ns
9	Data Valid after SCK Edge	t_{vsck}	—	—	$28 + 0.5 \cdot t_{bus}$ [1]	ns
10	Data Valid after $\overline{SS}$ fall	t_{vss}	—	—	$28 + 0.5 \cdot t_{bus}$ [1]	ns
11	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

[1] $0.5t_{bus}$ added due to internal synchronization delay

Table M-2. NVM Timing Characteristics for S12FTMRG64K512

#	Command	f_{NVMOP} cycle	f_{NVMBUS} cycle	Symbol	Min[1]	Typ[2]	Max[3]	Lfmax[4]	Unit
11	Erase P-Flash Sector	20015	858	t_{ERSPG}	19.10	20.05	20.08	26.73	ms
12	Unsecure Flash	100066	17570	t_{UNSECU}	96.00	100.77	101.47	160.22	ms
13	Verify Backdoor Access Key	0	481	t_{VFYKEY}	19.24	19.24	19.24	481.00	us
14	Set User Margin Level	0	399	t_{MLOADU}	15.96	15.96	15.96	399.00	us
15	Set Factory Margin Level	0	408	t_{MLOADF}	16.32	16.32	16.32	408.00	us
16	Erase Verify EEPROM Section	0	546	$t_{DRD1SEC}$	0.02	0.02	0.04	1.09	ms
17	Program EEPROM (1 Word)	68	1552	t_{DPGM_1}	0.13	0.13	0.32	6.29	ms
18	Program EEPROM (2 Word)	136	2486	t_{DPGM_2}	0.23	0.24	0.53	10.11	ms
19	Program EEPROM (3 Word)	204	3420	t_{DPGM_3}	0.33	0.34	0.75	13.94	ms
20	Program EEPROM (4 Word)	272	4354	t_{DPGM_4}	0.43	0.45	0.97	17.76	ms
21	Erase EEPROM Sector	5015	746	t_{DERSPG}	4.81	5.04	20.57	37.76	ms

1 Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2 Typical times are based on typical f_{NVMOP} and typical f_{NVMBUS}

3 Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging

4 Worst times are based on minimum f_{NVMOP} and minimum f_{NVMBUS}

Table M-3. NVM Timing Characteristics for S12FTMR32K128

Num	Command	f_{NVMOP} cycle	f_{NVMBUS} cycle	Symbol	Min[1]	Typ[2]	Max[3]	Lfmax[4]	Unit
1	Erase Verify All Blocks[5,6]	0	8947	t_{RD1ALL}	0.36	0.36	0.72	17.89	ms
2	Erase Verify Block (Pflash)[5]	0	8723	t_{RD1BLK_P}	0.35	0.35	0.70	17.45	ms
3	Erase Verify Block (EEPROM)[6]	0	597	t_{RD1BLK_D}	0.02	0.02	0.05	1.19	ms
4	Erase Verify P-Flash Section	0	492	t_{RD1SEC}	19.68	19.68	39.36	984.00	us
5	Read Once	0	445	t_{RDONCE}	17.80	17.80	17.80	445.00	us
6	Program P-Flash (4 Word)	164	2941	t_{PGM_4}	0.27	0.28	0.63	11.97	ms
7	Program Once	164	2888	$t_{PGMONCE}$	0.27	0.28	0.28	3.09	ms
8	Erase All Blocks[5,6]	100066	9348	t_{ERSALL}	95.67	100.44	100.81	143.78	ms
9	Erase Flash Block (Pflash)[5]	100060	9067	t_{ERSBLK_P}	95.66	100.42	100.79	143.21	ms
10	Erase Flash Block (EEPROM)[6]	100060	906	t_{ERSBLK_D}	95.33	100.10	100.13	126.89	ms
11	Erase P-Flash Sector	20015	881	t_{ERSPG}	19.10	20.05	20.09	26.78	ms
12	Unsecure Flash	100066	9426	t_{UNSECU}	95.68	100.44	100.82	143.93	ms