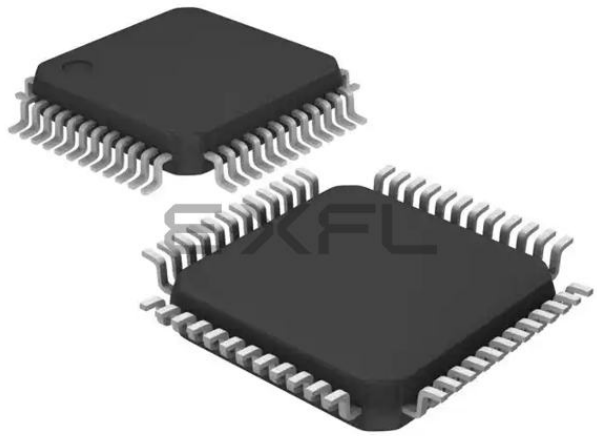

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Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
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Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vr48f2vlfr

LQFP			Function					Power Supply	Internal Pull Resistor	
48	32 [1]	Pin	1th Func.	2nd Func.	3rd Func.	4th Func.	5th Func.		CTRL	Reset State
28	19	VSSX2	—	—	—	—	—	—	—	—
29	—	HS1	OC3[5]	PWM1	PWM4	—	—	V_{SUPHS}	—	—
30	20	VSENSE	—	—	—	—	—	—	—	—
31	21	PL0	HVI0	KWL0	—	—	—	V_{DDX}	—	—
32	22	PL1	HVI1	KWL1	—	—	—	V_{DDX}	—	—
33	23	PL2	HVI2	KWL2	—	—	—	V_{DDX}	—	—
34	24	PL3	HVI3	KWL3	—	—	—	V_{DDX}	—	—
35	—	PAD5	KWAD5	AN5	—	—	—	V_{DDA}	PER1AD/ PPS1AD	Disabled
36	—	PAD4	KWAD4	AN4	—	—	—	V_{DDA}	PER1AD/ PPS1AD	Disabled
37	25	VSSA	—	—	—	—	—	—	—	—
38	26	VDDA	—	—	—	—	—	—	—	—
39	—	PAD3	KWAD3	AN3	—	—	—	V_{DDA}	PER1AD/ PPS1AD	Disabled
40	—	PAD2	KWAD2	AN2	—	—	—	V_{DDA}	PER1AD/ PPS1AD	Disabled
41	27	PAD1	KWAD1	AN1	—	—	—	V_{DDA}	PER1AD/ PPS1AD	Disabled
42	28	PAD0	KWAD0	AN0	—	—	—	V_{DDA}	PER1AD/ PPS1AD	Disabled
43	29	PT0	IOC0	PWM6	RXD0	—	—	V_{DDX}	PERT/PPST	Disabled
44	30	PT1	IOC1	PWM7	TXD0	LPDR1	—	V_{DDX}	PERT/PPST	Disabled
45	31	PT2	IOC2	LPRXD	SCK	—	—	V_{DDX}	PERT/PPST	Disabled
46	32	PT3	IOC3	LPTXD	$\overline{SS}$	—	—	V_{DDX}	PERT/PPST	Disabled
47	—	PS0	RXD0	RXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
48	—	PS1	TXD0	LPDR1	TXD1	—	—	V_{DDX}	PERS/PPSS	Up

1 SPI and SCI1 functionality on PS2, PS3, PT2 and PT3 not available on MC9S12VR16/32

2 Timer Output Compare Channel 0

3 Timer Output Compare Channel 1

4 Timer Output Compare Channel 2

5 Timer Output Compare Channel 3

Table 1-14. Usage of ADC Special Conversion Channels

ATDCTL5 Register Bits						Usage
SC	CD	CC	CB	CA	ADC Channel	
1	0	0	0	1	Internal_7	Bandgap Voltage V_{BG} or Chip temperature sensor V_{HT} see Section 4.3.2.13 High Temperature Control Register (CPMUHTCTL)
1	0	0	1	0	Internal_0	Flash Supply Voltage VDDF
1	1	0	1	0	Internal_4	V_{SENSE} or V_{SUP} selectable in BATS module see Section 17.1.1 Features
1	1	0	1	1	Internal_5	High voltage inputs Port L see Section 2.3.36 Port L Analog Access Register (PTAL)

1.12 Application Information

1.12.1 ADC Calibration

MCUs of the MC9S12VR-Family are able to measure the internal bandgap reference voltage V_{BG} with the analog digital converter. (see Table 1-14) V_{BG} is a constant voltage with a narrow distribution over temperature and external voltage supply. The ADC conversion result of V_{BG} is provided at address 0x0_405A/0x0_405B in the NVM IFR for reference. The measurement conditions of the reference conversion are listed in Table 1-15. By measuring the voltage V_{BG} and comparing the result to the reference value in the IFR it is possible to determine the reference voltage of the ADC V_{RH} in the application environment:

$$V_{RH} = \frac{StoredReference}{ConvertedReference} \bullet 5V$$

The exact absolute value of an analog conversion can be determined as follows:

$$Result = ConvertedADInput \bullet \frac{StoredReference \bullet 5V}{ConvertedReference \bullet 2^{n}}$$

With:

ConvertedADInput:	Result of the analog to digital conversion of the desired pin
ConvertedReference:	Result of channel “Internal_7” conversion
StoredReference:	Value in IFR location 0x0_405A/0x0_405B
n:	ADC resolution (10 bit)

[1] Read: Anytime
Write: Anytime

Table 2-12. DDRT Register Field Descriptions

Field	Description
3 DDRT	**Data Direction Register port T —** This bit determines whether the pin is an input or output Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. The enabled routed LINPHY forces the I/O state to be an input (LPTXD). Else the TIM forces the I/O state to be an output for a TIM port associated with an enabled TIM output compare. In these cases the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
2 DDRT	**Data Direction Register port T —** This bit determines whether the pin is an input or output. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. The enabled routed LINPHY forces the I/O state to be an output (LPRXD). Else the TIM forces the I/O state to be an output for a TIM port associated with an enabled TIM output compare. In these cases the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
1-0 DDRT	**Data Direction Register port T —** This bit determines whether the pin is an input or output. Depending on the configuration of the enabled routed SCI0 the I/O state will be forced to be input or output. The enabled routed LINPHY forces the I/O state to be an output (LPDR[LPDR1]). Else the TIM forces the I/O state to be an output for a TIM port associated with an enabled TIM output compare. In these cases the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input

2.3.14 Port T Pull Device Enable Register (PERT)

Address 0x0244 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PERT3	PERT2	PERT1	PERT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-12. Port T Pull Device Enable Register (PERT)

[1] Read: Anytime
Write: Anytime

Table 2-13. PERT Register Field Descriptions

Field	Description
3-0 PERT	**Pull device Enable Register port T** — Enable pull device on input pin This bit controls whether a pull device on the associated port input pin is active. If a pin is used as output this bit has no effect. The polarity is selected by the related polarity select register bit. 1 Pull device enabled 0 Pull device disabled

Table 2-17. PTS Register Field Descriptions

Field	Description
5 PTS	**PorT data register port S** — General-purpose input/output data, SPI $\overline{SS}$ When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read. • The SPI function takes precedence over the general-purpose I/O function if enabled.
4 PTS	**PorT data register port S** — General-purpose input/output data, SPI SCK When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read. • The SPI function takes precedence over the general-purpose I/O function if enabled.
3 PTS	**PorT data register port S** — General-purpose input/output data, ECLK, SPI MOSI, routed SCI1, routed PWM, routed ETRIG When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read. • The ECLK output function takes precedence over the SPI, routed SCI1 and PWM and the general purpose I/O function if enabled. • The SPI function takes precedence over the routed SCI1, routed PWM and the general purpose I/O function if enabled. • The routed SCI1 function takes precedence over the PWM and general-purpose I/O function if enabled. • The routed PWM function takes precedence over the general-purpose I/O function if enabled.
2 PTS	**PorT data register port S** — General-purpose input/output data, SPI MISO, routed SCI1, routed PWM, routed ETRIG When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read. • The SPI function takes precedence over the routed SCI1, routed PWM and the general purpose I/O function if enabled. • The routed SCI1 function takes precedence over the routed PWM and the general-purpose I/O function if enabled. • The routed PWM function takes precedence over the general-purpose I/O function if enabled.
1 PTS	**PorT data register port S** — General-purpose input/output data, SCI1, routed SCI0 or LPDR[LPDR1] When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read. • The SCI1 function takes precedence over the routed SCI0 or LPDR[LPDR1] function and the general-purpose I/O function if enabled. • The routed SCI0 or LPDR[LPDR1] function takes precedence over the general-purpose I/O function if enabled.
0 PTS	**PorT data register port S** — General-purpose input/output data, SCI1, routed SCI0 When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read. • The SCI1 function takes precedence over the routed SCI0 function and the general-purpose I/O function if enabled. • The routed SCI0 function takes precedence over the general-purpose I/O function if enabled.

For example selecting a pullup device: This device does not become active while the port is used as a push-pull output.

Table 2-48. Register availability per port[1]

Port	Data	Input	Data Direction	Reduced Drive	Pull Enable	Polarity Select	Wired-Or Mode	Interrupt Enable	Interrupt Flag	Routing
E	yes	-	yes	-	yes	-	-	-	-	-
T	yes	yes	yes	-	yes	yes	-	-	-	yes
S	yes	yes	yes	-	yes	yes	yes	-	-	yes
P	yes	yes	yes	yes	yes	yes	-	yes	yes	-
L	-	yes	yes[2]	-	-	yes	-	yes	yes	-
AD	yes	yes	yes	-	yes	yes	-	yes	yes	-

1 Each cell represents one register with individual configuration bits

2 Input buffer control only

2.4.2.1 Data register (PTx)

This register holds the value driven out to the pin if the pin is used as a general-purpose I/O.

Writing to this register has only an effect on the pin if the pin is used as general-purpose output. When reading this address, the synchronized state of the pin is returned if the associated data direction register bit is set to “0”.

If the data direction register bits are set to logic level “1”, the contents of the data register is returned. This is independent of any other configuration (Figure 2-70).

2.4.2.2 Input register (PTIx)

This register is read-only and always returns the synchronized state of the pin (Figure 2-70).

2.4.2.3 Data direction register (DDRx)

This register defines whether the pin is used as an general-purpose input or an output.

If a peripheral module controls the pin the contents of the data direction register is ignored (Figure 2-70).

Independent of the pin usage with a peripheral module this register determines the source of data when reading the associated data register address (2.4.2.1/2-105).

NOTE

Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on port data or port input registers, when changing the data direction register.

Table 4-13. CPMUCOP Field Descriptions

Field	Description
7 WCOP	**Window COP Mode Bit** — When set, a write to the CPMUARMCOP register must occur in the last 25% of the selected period.A write during the first 75% of the selected period generates a COP reset.As long as all writes occur during this window, $55 can be written as often as desired.Once $AA is written after the $55, the time-out logic restarts and the user must wait until the next window before writing to CPMUARMCOP. Table 4-14 shows the duration of this window for the seven available COP rates. 0 Normal COP operation 1 Window COP operation
6 RSBCK	**COP and RTI Stop in Active BDM Mode Bit** 0 Allows the COP and RTI to keep running in Active BDM mode. 1 Stops the COP and RTI counters whenever the part is in Active BDM mode.
5 WRTMASK	**Write Mask for WCOP and CR[2:0] Bit** — This write-only bit serves as a mask for the WCOP and CR[2:0] bits while writing the CPMUCOP register. It is intended for BDM writing the RSBCK without changing the content of WCOP and CR[2:0]. 0 Write of WCOP and CR[2:0] has an effect with this write of CPMUCOP 1 Write of WCOP and CR[2:0] has no effect with this write of CPMUCOP. (Does not count for “write once”.)
2–0 CR[2:0]	**COP Watchdog Timer Rate Select** — These bits select the COP time-out rate (see Table 4-14 and Table 4-15). Writing a nonzero value to CR[2:0] enables the COP counter and starts the time-out period.A COP counter time-out causes a System Reset.This can be avoided by periodically (before time-out) initializing the COP counter via the CPMUARMCOP register. While all of the following four conditions are true the CR[2:0], WCOP bits are ignored and the COP operates at highest time-out period (2^{24} cycles) in normal COP mode (Window COP mode disabled): 1) COP is enabled (CR[2:0] is not 000) 2) BDM mode active 3) RSBCK = 0 4) Operation in Special Mode

Table 4-14. COP Watchdog Rates if COPOSCSEL1=0. (default out of reset)

CR2	CR1	CR0	COPCLK Cycles to time-out (COPCLK is either IRCCLK or OSCCLK depending on the COPOSCSEL0 bit)
0	0	0	COP disabled
0	0	1	2^{14}
0	1	0	2^{16}
0	1	1	2^{18}
1	0	0	2^{20}
1	0	1	2^{22}
1	1	0	2^{23}
1	1	1	2^{24}

4.3.2.12 S12CPMU_UHV_V8 COP Timer Arm/Reset Register (CPMUARMCOP)

This register is used to restart the COP time-out period.

0x003F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	ARMCOP-Bit 7	ARMCOP-Bit 6	ARMCOP-Bit 5	ARMCOP-Bit 4	ARMCOP-Bit 3	ARMCOP-Bit 2	ARMCOP-Bit 1	ARMCOP-Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 4-15. S12CPMU_UHV_V8 CPMUARMCOP Register

Read: Always reads $00

Write: Anytime

When the COP is disabled (CR[2:0] = “000”) writing to this register has no effect.

When the COP is enabled by setting CR[2:0] nonzero, the following applies:

Writing any value other than $55 or $AA causes a COP reset. To restart the COP time-out period write $55 followed by a write of $AA. These writes do not need to occur back-to-back, but the sequence ($55, $AA) must be completed prior to COP end of time-out period to avoid a COP reset. Sequences of $55 writes are allowed. When the WCOP bit is set, $55 and $AA writes must be done in the last 25% of the selected time-out period; writing any value in the first 75% of the selected period will cause a COP reset.

4.3.2.13 High Temperature Control Register (CPMUHTCTL)

The CPMUHTCTL register configures the temperature sense features.

0x02F0

	7	6	5	4	3	2	1	0
R	0	0	VSEL	0	HTE	HTDS	HTIE	HTIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 4-16. High Temperature Control Register (CPMUHTCTL)

Read: Anytime

Write: VSEL, HTE, HTIE and HTIF are write anytime, HTDS is read only

8.2 Signal Description

This section lists all inputs to the ADC12B6CV2 block.

8.2.1 Detailed Signal Descriptions

8.2.1.1 AN*x* (*x* = 5, 4, 3, 2, 1, 0)

This pin serves as the analog input Channel *x*. It can also be configured as digital port or external trigger for the ATD conversion.

8.2.1.2 ETRIG3, ETRIG2, ETRIG1, ETRIG0

These inputs can be configured to serve as an external trigger for the ATD conversion.

Refer to device specification for availability and connectivity of these inputs!

8.2.1.3 VRH, VRL

VRH is the high reference voltage, VRL is the low reference voltage for ATD conversion.

8.2.1.4 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ADC12B6CV2 block.

8.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC12B6CV2.

8.3.1 Module Memory Map

Figure 8-2 gives an overview on all ADC12B6CV2 registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ATDCTL0	R	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
		W								
0x0001	ATDCTL1	R	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
		W								
0x0002	ATDCTL2	R	0	AFFC	Reserved	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ACMPIE
		W								

= Unimplemented or Reserved

Figure 8-2. ADC12B6CV2 Register Summary (Sheet 1 of 2)

Table 10-11. SCISR1 Field Descriptions (continued)

Field	Description
3 OR	**Overrun Flag** — OR is set when software fails to read the SCI data register before the receive shift register receives the next frame. The OR bit is set immediately after the stop bit has been completely received for the second frame. The data in the shift register is lost, but the data already in the SCI data registers is not affected. Clear OR by reading SCI status register 1 (SCISR1) with OR set and then reading SCI data register low (SCIDRL). 0 No overrun 1 Overrun **Note:** OR flag may read back as set when RDRF flag is clear. This may happen if the following sequence of events occurs: 1. After the first frame is received, read status register SCISR1 (returns RDRF set and OR flag clear); 2. Receive second frame without reading the first frame in the data register (the second frame is not received and OR flag is set); 3. Read data register SCIDRL (returns first frame and clears RDRF flag in the status register); 4. Read status register SCISR1 (returns RDRF clear and OR set). Event 3 may be at exactly the same time as event 2 or any time after. When this happens, a dummy SCIDRL read following event 4 will be required to clear the OR flag if further frames are to be received.
2 NF	**Noise Flag** — NF is set when the SCI detects noise on the receiver input. NF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear NF by reading SCI status register 1(SCISR1), and then reading SCI data register low (SCIDRL). 0 No noise 1 Noise
1 FE	**Framing Error Flag** — FE is set when a logic 0 is accepted as the stop bit. FE bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. FE inhibits further data reception until it is cleared. Clear FE by reading SCI status register 1 (SCISR1) with FE set and then reading the SCI data register low (SCIDRL). 0 No framing error 1 Framing error
0 PF	**Parity Error Flag** — PF is set when the parity enable bit (PE) is set and the parity of the received data does not match the parity type bit (PT). PF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear PF by reading SCI status register 1 (SCISR1), and then reading SCI data register low (SCIDRL). 0 No parity error 1 Parity error

The main element of the SPI system is the SPI data register. The n-bit[1] data register in the master and the n-bit[1] data register in the slave are linked by the MOSI and MISO pins to form a distributed 2n-bit[1] register. When a data transfer operation is performed, this 2n-bit[1] register is serially shifted n[1] bit positions by the S-clock from the master, so data is exchanged between the master and the slave. Data written to the master SPI data register becomes the output data for the slave, and data read from the master SPI data register after a transfer operation is the input data from the slave.

A read of SPISR with SPTEF = 1 followed by a write to SPIDR puts data into the transmit data register. When a transfer is complete and SPIF is cleared, received data is moved into the receive data register. This data register acts as the SPI receive data register for reads and as the SPI transmit data register for writes. A common SPI data register address is shared for reading data from the read data buffer and for writing data to the transmit data register.

The clock phase control bit (CPHA) and a clock polarity control bit (CPOL) in the SPI control register 1 (SPICR1) select one of four possible clock formats to be used by the SPI system. The CPOL bit simply selects a non-inverted or inverted clock. The CPHA bit is used to accommodate two fundamentally different protocols by sampling data on odd numbered SCK edges or on even numbered SCK edges (see Section 11.4.3, “Transmission Formats”).

The SPI can be configured to operate as a master or as a slave. When the MSTR bit in SPI control register1 is set, master mode is selected, when the MSTR bit is clear, slave mode is selected.

NOTE

A change of CPOL or MSTR bit while there is a received byte pending in the receive shift register will destroy the received byte and must be avoided.

11.4.1 Master Mode

The SPI operates in master mode when the MSTR bit is set. Only a master SPI module can initiate transmissions. A transmission begins by writing to the master SPI data register. If the shift register is empty, data immediately transfers to the shift register. Data begins shifting out on the MOSI pin under the control of the serial clock.

- Serial clock

  The SPR2, SPR1, and SPR0 baud rate selection bits, in conjunction with the SPPR2, SPPR1, and SPPR0 baud rate preselection bits in the SPI baud rate register, control the baud rate generator and determine the speed of the transmission. The SCK pin is the SPI clock output. Through the SCK pin, the baud rate generator of the master controls the shift register of the slave peripheral.
- MOSI, MISO pin

  In master mode, the function of the serial data output pin (MOSI) and the serial data input pin (MISO) is determined by the SPC0 and BIDIROE control bits.
- $\overline{SS}$ pin

  If MODFEN and SSOE are set, the $\overline{SS}$ pin is configured as slave select output. The $\overline{SS}$ output becomes low during each transmission and is high when the SPI is in idle state.

1. n depends on the selected transfer width, please refer to Section 11.3.2.2, “SPI Control Register 2 (SPICR2)

NOTE

Care must be taken when expecting data from a master while the slave is in wait or stop mode. Even though the shift register will continue to operate, the rest of the SPI is shut down (i.e., a SPIF interrupt will **not** be generated until exiting stop or wait mode). Also, the byte from the shift register will not be copied into the SPIDR register until after the slave SPI has exited wait or stop mode. In slave mode, a received byte pending in the receive shift register will be lost when entering wait or stop mode. An SPIF flag and SPIDR copy is generated only if wait mode is entered or exited during a tranmission. If the slave enters wait mode in idle mode and exits wait mode in idle mode, neither a SPIF nor a SPIDR copy will occur.

11.4.7.3 SPI in Stop Mode

Stop mode is dependent on the system. The SPI enters stop mode when the module clock is disabled (held high or low). If the SPI is in master mode and exchanging data when the CPU enters stop mode, the transmission is frozen until the CPU exits stop mode. After stop, data to and from the external SPI is exchanged correctly. In slave mode, the SPI will stay synchronized with the master.

The stop mode is not dependent on the SPISWAI bit.

11.4.7.4 Reset

The reset values of registers and signals are described in Section 11.3, “Memory Map and Register Definition”, which details the registers and their bit fields.

- If a data transmission occurs in slave mode after reset without a write to SPIDR, it will transmit garbage, or the data last received from the master before the reset.
- Reading from the SPIDR after reset will always read zeros.

11.4.7.5 Interrupts

The SPI only originates interrupt requests when SPI is enabled (SPE bit in SPICR1 set). The following is a description of how the SPI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt priority are chip dependent.

The interrupt flags MODF, SPIF, and SPTEF are logically ORed to generate an interrupt request.

11.4.7.5.1 MODF

MODF occurs when the master detects an error on the $\overline{SS}$ pin. The master SPI must be configured for the MODF feature (see Table 11-3). After MODF is set, the current transfer is aborted and the following bit is changed:

- MSTR = 0, The master bit in SPICR1 resets.

The MODF interrupt is reflected in the status register MODF flag. Clearing the flag will also clear the interrupt. This interrupt will stay active while the MODF flag is set. MODF has an automatic clearing process which is described in Section 11.3.2.4, “SPI Status Register (SPISR)”.

Chapter 12
Timer Module (TIM16B4CV3)

Table 12-1.

V03.00	Jan. 28, 2009		Initial version
V03.01	Aug. 26, 2009	12.1.2/12-390 Figure 1-4./1-8 1.3.2.15/1-18 12.3.2.2/12-393, 1.3.2.3/1-8, 1.3.2.4/1-9, 12.4.3/12-404	- Correct typo: TSCR ->TSCR1; - Correct typo: ECTxxx->TIMxxx - Correct reference: Figure 1-25 -> Figure 12-22 - Add description, “a counter overflow when TTOV[7] is set”, to be the condition of channel 7 override event. - Phrase the description of OC7M to make it more explicit
V03.02	Apri,12,2010	12.3.2.6/12-396 12.3.2.9/12-398 12.4.3/12-404	-Add Table 1-10 -update TCRE bit description -add Figure 1-31
V03.03	Jan,14,2013		-single source generate different channel guide

12.1 Introduction

The basic scalable timer consists of a 16-bit, software-programmable counter driven by a flexible programmable prescaler.

This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform.

This timer could contain up to 4 input capture/output compare channels . The input capture function is used to detect a selected transition edge and record the time. The output compare function is used for generating output signals or for timer software delays.

A full access for the counter registers or the input capture/output compare registers should take place in one clock cycle. Accessing high byte and low byte separately for all of these registers may not yield the same result as accessing them in one word.

12.1.1 Features

The TIM16B4CV3 includes these distinctive features:

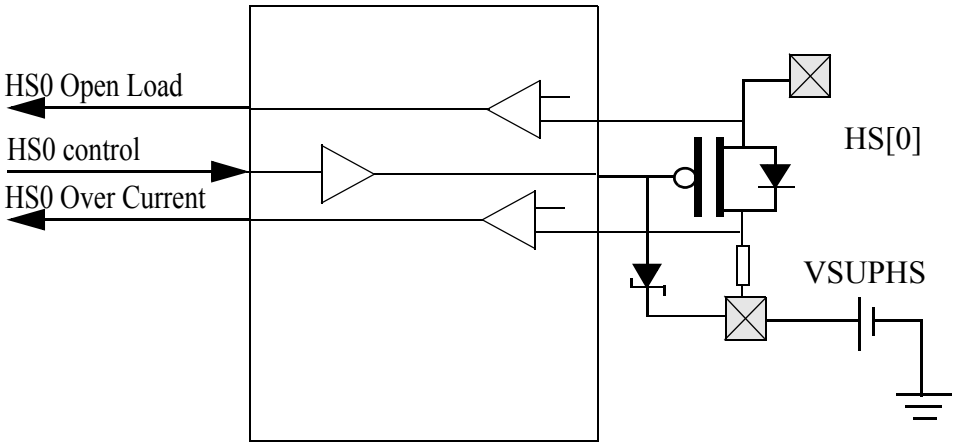
- Up to 4 channels available. (refer to device specification for exact number)
- All channels have same input capture/output compare functionality.
- Clock prescaling.
- 16-bit counter.

cleared automatically. After returning from stop mode the driver is re-enabled and the state of the HSCR[HSE0] bit is set automatically. If the data register bit (HSDR[HSDR0]) is chosen as source in the PIM module, then the high-side driver stays turned off until the software sets the associated bit in the data register (HSDR[HSDR0]). When the timer or PWM is chosen as source, the high-side driver is controlled by the timer or PWM without further handling. When it is required that the driver stays turned off after the stop mode for this case (PWM or timer), the software must take the appropriate action to turn off the driver before entering stop mode.

14.1.3 Block Diagram

Figure 14-1 shows a block diagram of the HSDRV1C module. The module consists of a control and an output stage. The high-side driver gate control can be routed. See PIM chapter for routing options.

Figure 14-1. HSDRV1C Block Diagram



14.2 External Signal Description

Table 14-2 shows the external pins associated with the HSDRV1C module.

Table 14-2. HSDRV1C Signal Properties

Name	Function	Reset State
HS[0]	High-side driver output 0	disabled (off)
VSUPHS	High Voltage Power Supply for high side driver	disabled (off)

14.2.1 HS[0] — High Side Driver Pin

Output of the high-side driver intended to drive LEDs or resistive loads.

14.2.2 VSUPHS — High Side Driver Power Pin

Power supply for the high-side driver.

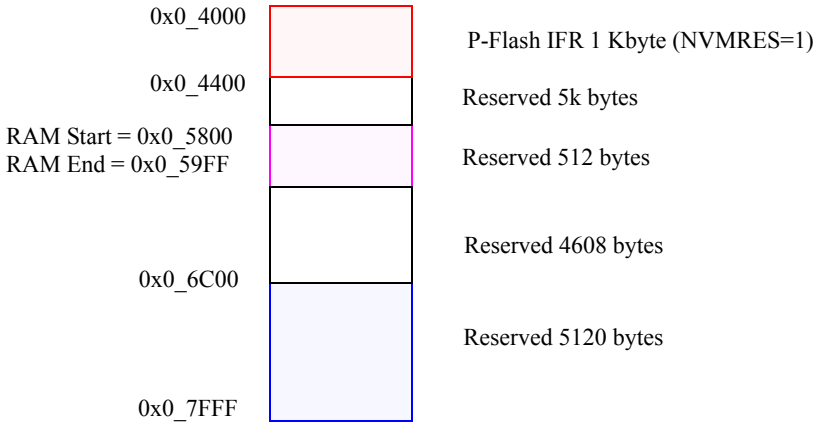


Figure 19-3. Memory Controller Resource Memory Map (NVMRES=1)

19.3.2 Register Descriptions

The Flash module contains a set of 20 control and status registers located between Flash module base + 0x0000 and 0x0013.

In the case of the writable registers, the write accesses are forbidden during Fash command execution (for more detail, see Caution note in Section 19.3 Memory Map and Registers).

A summary of the Flash module registers is given in Figure 19-4 with detailed descriptions in the following subsections.

Address & Name		7	6	5	4	3	2	1	0
FCLKDIV	R	FDIVLD	FDIVLCK	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
	W								
FSEC	R	KEYEN1	KEYEN0	RNV5	RNV4	RNV3	RNV2	SEC1	SEC0
	W								
FCCOBIX	R	0	0	0	0	0	CCOBIX2	CCOBIX1	CCOBIX0
	W								

Figure 19-4. FTMRG32K128 Register Summary

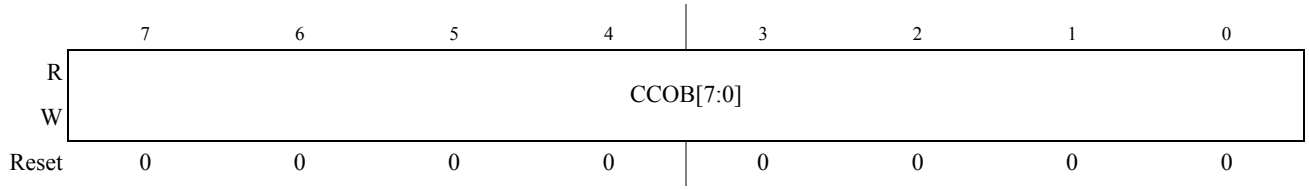


Figure 19-17. Flash Common Command Object Low Register (FCCOBLO)

19.3.2.11.1 FCCOB - NVM Command Mode

NVM command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates the command's execution by writing a 1 to the CCIF bit in the FSTAT register (a 1 written by the user clears the CCIF command completion flag to 0). When the user clears the CCIF bit in the FSTAT register all FCCOB parameter fields are locked and cannot be changed by the user until the command completes (as evidenced by the Memory Controller returning CCIF to 1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in NVM command mode is shown in Table 19-24. The return values are available for reading after the CCIF flag in the FSTAT register has been returned to 1 by the Memory Controller. Writes to the unimplemented parameter fields (CCOBIX = 110 and CCOBIX = 111) are ignored with reads from these fields returning 0x0000.

Table 19-24 shows the generic Flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific Flash command. For details on the FCCOB settings required by each command, see the Flash command descriptions in Section 19.4.6 Flash Command Description.

Table 19-24. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)
000	HI	FCMD[7:0] defining Flash command
	LO	6'h0, Global address [17:16]
001	HI	Global address [15:8]
	LO	Global address [7:0]
010	HI	Data 0 [15:8]
	LO	Data 0 [7:0]
011	HI	Data 1 [15:8]
	LO	Data 1 [7:0]
100	HI	Data 2 [15:8]
	LO	Data 2 [7:0]
101	HI	Data 3 [15:8]
	LO	Data 3 [7:0]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-21. Flash Reserved4 Register (FRSV4)

All bits in the FRSV4 register read 0 and are not writable.

19.3.2.16 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

	7	6	5	4	3	2	1	0
R	NV[7:0]							
W								
Reset	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]

= Unimplemented or Reserved

Figure 19-22. Flash Option Register (FOPT)

1 Loaded from IFR Flash configuration field, during reset sequence.

All bits in the FOPT register are readable but are not writable.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x3_FF0E located in P-Flash memory (see Table 19-4) as indicated by reset condition F in Figure 19-22. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 19-25. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	**Nonvolatile Bits** — The NV[7:0] bits are available as nonvolatile bits. Refer to the device user guide for proper use of the NV bits.

19.3.2.17 Flash Reserved5 Register (FRSV5)

This Flash register is reserved for factory testing.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-23. Flash Reserved5 Register (FRSV5)

19.4.4.3 Valid Flash Module Commands

Table 19-27 present the valid Flash commands, as enabled by the combination of the functional MCU mode (Normal SingleChip NS, Special Singlechip SS) with the MCU security state (Unsecured, Secured).

Special Singlechip mode is selected by input mmc_ss_mode_ts2 asserted. MCU Secured state is selected by input mmc_secure input asserted.

Table 19-27. Flash Commands by Mode and Security State

FCMD	Command	Unsecured		Secured	
		NS[1]	SS[2]	NS[3]	SS[4]
0x01	Erase Verify All Blocks	*	*	*	*
0x02	Erase Verify Block	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	
0x04	Read Once	*	*	*	
0x06	Program P-Flash	*	*	*	
0x07	Program Once	*	*	*	
0x08	Erase All Blocks		*		*
0x09	Erase Flash Block	*	*	*	
0x0A	Erase P-Flash Sector	*	*	*	
0x0B	Unsecure Flash		*		*
0x0C	Verify Backdoor Access Key	*		*	
0x0D	Set User Margin Level	*	*	*	
0x0E	Set Field Margin Level		*		
0x10	Erase Verify EEPROM Section	*	*	*	
0x11	Program EEPROM	*	*	*	
0x12	Erase EEPROM Sector	*	*	*	

1 Unsecured Normal Single Chip mode

2 Unsecured Special Single Chip mode.

3 Secured Normal Single Chip mode.

4 Secured Special Single Chip mode.

The following subsections describe these security-related subjects:

- Unsecuring the MCU using Backdoor Key Access
- Unsecuring the MCU in Special Single Chip Mode using BDM
- Mode and Security Effects on Flash Command Availability

19.5.1 Unsecuring the MCU using Backdoor Key Access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys (four 16-bit words programmed at addresses 0x3_FF00-0x3_FF07). If the KEYEN[1:0] bits are in the enabled state (see Section 19.3.2.2 Flash Security Register (FSEC)), the Verify Backdoor Access Key command (see Section 19.4.6.11 Verify Backdoor Access Key Command) allows the user to present four prospective keys for comparison to the keys stored in the Flash memory via the Memory Controller. If the keys presented in the Verify Backdoor Access Key command match the backdoor keys stored in the Flash memory, the SEC bits in the FSEC register (see Table 19-11) will be changed to unsecure the MCU. Key values of 0x0000 and 0xFFFF are not permitted as backdoor keys. While the Verify Backdoor Access Key command is active, P-Flash memory and EEPROM memory will not be available for read access and will return invalid data.

The user code stored in the P-Flash memory must have a method of receiving the backdoor keys from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports.

If the KEYEN[1:0] bits are in the enabled state (see Section 19.3.2.2 Flash Security Register (FSEC)), the MCU can be unsecured by the backdoor key access sequence described below:

1. Follow the command sequence for the Verify Backdoor Access Key command as explained in Section 19.4.6.11 Verify Backdoor Access Key Command
2. If the Verify Backdoor Access Key command is successful, the MCU is unsecured and the SEC[1:0] bits in the FSEC register are forced to the unsecure state of 10

The Verify Backdoor Access Key command is monitored by the Memory Controller and an illegal key will prohibit future use of the Verify Backdoor Access Key command. A reset of the MCU is the only method to re-enable the Verify Backdoor Access Key command. The security as defined in the Flash security byte (0x3_FF0F) is not changed by using the Verify Backdoor Access Key command sequence. The backdoor keys stored in addresses 0x3_FF00-0x3_FF07 are unaffected by the Verify Backdoor Access Key command sequence. The Verify Backdoor Access Key command sequence has no effect on the program and erase protections defined in the Flash protection register, FPROT.

After the backdoor keys have been correctly matched, the MCU will be unsecured. After the MCU is unsecured, the sector containing the Flash security byte can be erased and the Flash security byte can be reprogrammed to the unsecure state, if desired. In the unsecure state, the user has full control of the contents of the backdoor keys by programming addresses 0x3_FF00-0x3_FF07 in the Flash configuration field.

Appendix L
XOSCLCP Electrical Specifications

Table L-1. XOSCLCP Characteristics

Conditions are shown in Table A-5 unless otherwise noted						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Nominal crystal or resonator frequency	f_{OSC}	4.0		20	MHz
2	Startup Current	i_{OSC}	100			µA
3a	Oscillator start-up time (4MHz)[1]	t_{UPOSC}	—	2	10	ms
3b	Oscillator start-up time (8MHz)[1]	t_{UPOSC}	—	1.6	8	ms
3c	Oscillator start-up time (16MHz)[1]	t_{UPOSC}	—	1	5	ms
4	Clock Monitor Failure Assert Frequency	f_{CMFA}	200	450	1200	kHz
5	Input Capacitance (EXTAL, XTAL pins)	C_{IN}		7		pF
6	EXTAL Pin Input Hysteresis	$V_{HYS,EXTAL}$	—	120	—	mV
7	EXTAL Pin oscillation amplitude (loop controlled Pierce)	$V_{PP,EXTAL}$	—	0.9	—	V
8	EXTAL Pin oscillation required amplitude[2]	$V_{PP,EXTAL}$	0.8	—	1.5	V

[1] These values apply for carefully designed PCB layouts with capacitors that match the crystal/resonator requirements.

[2]Needs to be measured at room temperature on the application board using a probe with very low (<=5pF) input capacitance.