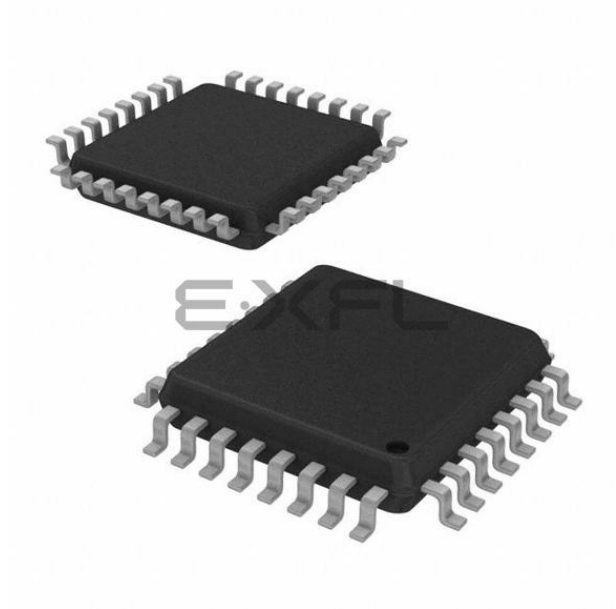

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Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vr64af0clc

Table 1-10. Interrupt Vector Locations (Sheet 2 of 3)

Vector Address	Interrupt Source	CCR Mask	Local Enable	Wake up from STOP	Wake up from WAIT
Vector base + $D4	SCI1	I bit	SCI1CR2 (TIE, TCIE, RIE, ILIE) SCI1ACR1 (RXEDGIE, BERRIE, BKDIE)	RXEDGIF only	Yes
Vector base + $D2	ADC	I bit	ATDCTL2 (ASCIE)	No	Yes
Vector base + $D0	Reserved				
Vector base + $CE	Port L	I bit	PIEL (PIEL3-PIEL0)	Yes	Yes
Vector base + $CC to Vector base + $CA	Reserved				
Vector base + $C8	Oscillator status interrupt	I bit	CPMUINT (OSCIE)	No	Yes
Vector base + $C6	PLL lock interrupt	I bit	CPMUINT (LOCKIE)	No	Yes
Vector base + $C4 to Vector base + $BC	Reserved				
Vector base + $BA	FLASH error	I bit	FERCNFG (SFDIE, DFDIE)	No	No
Vector base + $B8	FLASH command	I bit	FCNFG (CCIE)	No	Yes
Vector base + $B6 to Vector base + $B0	Reserved				
Vector base + $AE	HSDRV over-current interrupt	I bit	HSIE (HSERR)	No	Yes
Vector base + $AC	LSDRV over-current interrupt	I bit	LSIE (LSERR)	No	Yes
Vector base + $AA	LINPHY over-current interrupt or Txd-dominant timeout interrupt	I bit	LPIE (LPDTIE & LPOCIE)	No	Yes
Vector base + $A8	BATS low & high battery voltage interrupt	I bit	BATIE (BVHIE,BVLIE)	No	Yes
Vector base + $A6 to Vector base + $90	Reserved				
Vector base + $8E	Port P interrupt	I bit	PIEP (PIEP5-PIEP3, PIEP1-PIEP0)	Yes	Yes
Vector base+ $8C	Port P2 (EVDD Hall Sensor Supply) over-current interrupt	I bit	PIEP (OCIE)	No	Yes
Vector base + $8A	Low-voltage interrupt (LVI)	I bit	CPMUCTRL (LVIE)	No	Yes
Vector base + $88	Autonomous periodical interrupt (API)	I bit	CPMUAPICTRL (APIE)	Yes	Yes
Vector base + $86	High temperature interrupt	I bit	CPMUHTCTL(HTIE)	No	Yes
Vector base + $84	ADC compare interrupt	I bit	ATDCTL2 (ACMPIE)	No	Yes
Vector base + $82	Port AD interrupt	I bit	PIE1AD(PIE1AD5-PIE1AD0)	Yes	Yes

2.4.2.8 Interrupt enable register (PIEx)

If the pin is used as an interrupt input this register serves as a mask to the interrupt flag to enable/disable the interrupt.

2.4.2.9 Interrupt flag register (PIFx)

If the pin is used as an interrupt input this register holds the interrupt flag after a valid pin event.

2.4.2.10 Module routing register (MODRRx)

Routing registers allow software re-configuration of specific peripheral inputs and outputs:

- MODRR0 selects the driving source of the HSDRV and LSDRV pins
- MODRR1 selects optional pins for PWM channels and ETRIG inputs (S12VR64/48 only)
- MODRR2 supports options to test the internal SCI-LINPHY interface signals

2.4.3 Pins and Ports

NOTE

Please refer to the device pinout section to determine the pin availability in the different package options.

2.4.3.1 BKGD pin

The BKGD pin is associated with the BDM module.

During reset, the BKGD pin is used as MODC input.

2.4.3.2 Port E

This port is associated with the CPMU OSC.

Port E pins PE1-0 can be used for general-purpose or with the CPMU OSC module.

2.4.3.3 Port T

This port is associated with TIM, routed SCI-LINPHY interface and routed SPI.

Port T pins can be used for either general-purpose I/O or with the channels of the standard TIM, SPI, or SCI and LINPHY subsystems.

2.4.3.4 Port S

This port is associated with the API_EXTCLK, ECLK, SPI, SCI1, routed SCI0, routed PWM channels and ETRIG inputs.

Port S pins can be used either for general-purpose I/O, or with the ECLK, SPI, SCI, and PWM subsystems.

Table 6-26. DBGXAM Field Descriptions

Field	Description
7–0 Bit[15:8]	**Comparator Address Mid Compare Bits** — The Comparator address mid compare bits control whether the selected comparator compares the address bus bits [15:8] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

6.3.2.8.4 Debug Comparator Address Low Register (DBGXAL)

Address: 0x002B

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 6-18. Debug Comparator Address Low Register (DBGXAL)

Read: Anytime. See Table 6-24 for visible register encoding.

Write: If DBG not armed. See Table 6-24 for visible register encoding.

Table 6-27. DBGXAL Field Descriptions

Field	Description
7–0 Bits[7:0]	**Comparator Address Low Compare Bits** — The Comparator address low compare bits control whether the selected comparator compares the address bus bits [7:0] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

6.3.2.8.5 Debug Comparator Data High Register (DBGADH)

Address: 0x002C

	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 6-19. Debug Comparator Data High Register (DBGADH)

Read: If COMRV[1:0] = 00

Write: If COMRV[1:0] = 00 and DBG not armed.

NOTE

When program control returns from a tagged breakpoint using an RTI or BDM GO command without program counter modification it returns to the instruction whose tag generated the breakpoint. To avoid a repeated breakpoint at the same location reconfigure the DBG module in the SWI routine, if configured for an SWI breakpoint, or over the BDM interface by executing a TRACE command before the GO to increment the program flow past the tagged instruction.

6.5 Application Information

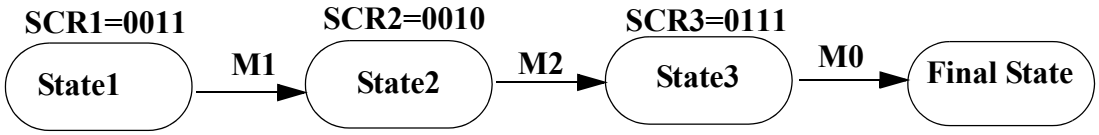
6.5.1 State Machine scenarios

Defining the state control registers as SCR1,SCR2, SCR3 and M0,M1,M2 as matches on channels 0,1,2 respectively. SCR encoding supported by S12SDBGV1 are shown in black. SCR encoding supported only in S12SDBGV2 are shown in red. For backwards compatibility the new scenarios use a 4th bit in each SCR register. Thus the existing encoding for SCRx[2:0] is not changed.

6.5.2 Scenario 1

A trigger is generated if a given sequence of 3 code events is executed.

Figure 6-27. Scenario 1

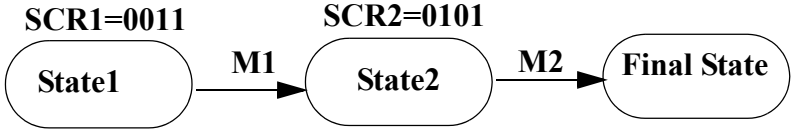


Scenario 1 is possible with S12SDBGV1 SCR encoding

6.5.3 Scenario 2

A trigger is generated if a given sequence of 2 code events is executed.

Figure 6-28. Scenario 2a



NOTE

Changing the PWM output mode from left aligned to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

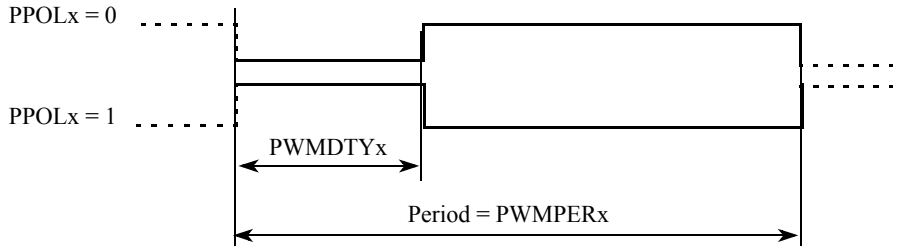


Figure 9-17. PWM Left Aligned Output Waveform

To calculate the output frequency in left aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB) and divide it by the value in the period register for that channel.

- PWMx Frequency = Clock (A, B, SA, or SB) / PWMPERx
- PWMx Duty Cycle (high time as a% of period):
  - Polarity = 0 (PPOLx = 0)

    Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  - Polarity = 1 (PPOLx = 1)

    Duty Cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a left aligned output, consider the following case:

Clock Source = bus clock, where bus clock = 10 MHz (100 ns period)

PPOLx = 0

PWMPERx = 4

PWMDTYx = 1

PWMx Frequency = 10 MHz/4 = 2.5 MHz

PWMx Period = 400 ns

PWMx Duty Cycle = 3/4 *100% = 75%

The output waveform generated is shown in Figure 9-18.

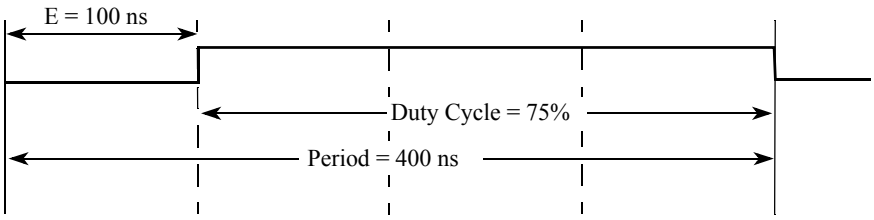


Figure 9-18. PWM Left Aligned Output Example Waveform

10.3.2.9 SCI Data Registers (SCIDRH, SCIDRL)

	7	6	5	4	3	2	1	0
R	R8	T8	0	0	0	Reserved	Reserved	Reserved
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-12. SCI Data Registers (SCIDRH)

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 10-13. SCI Data Registers (SCIDRL)

Read: Anytime; reading accesses SCI receive data register

Write: Anytime; writing accesses SCI transmit data register; writing to R8 has no effect

Table 10-13. SCIDRH and SCIDRL Field Descriptions

Field	Description
SCIDRH 7 R8	**Received Bit 8** — R8 is the ninth data bit received when the SCI is configured for 9-bit data format (M = 1).
SCIDRH 6 T8	**Transmit Bit 8** — T8 is the ninth data bit transmitted when the SCI is configured for 9-bit data format (M = 1).
SCIDRL 7:0 R[7:0] T[7:0]	**R7:R0** — Received bits seven through zero for 9-bit or 8-bit data formats **T7:T0** — Transmit bits seven through zero for 9-bit or 8-bit formats

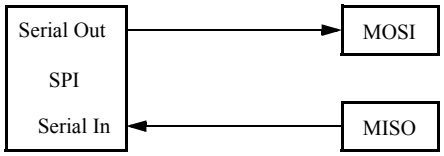
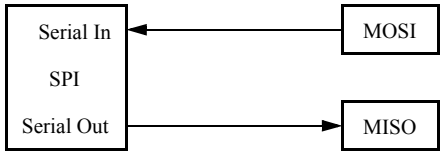
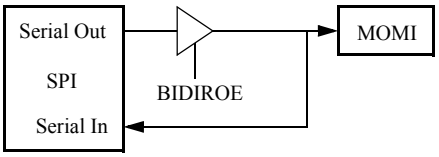
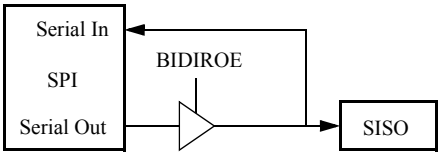
NOTE

If the value of T8 is the same as in the previous transmission, T8 does not have to be rewritten.The same value is transmitted until T8 is rewritten

In 8-bit data format, only SCI data register low (SCIDRL) needs to be accessed.

When transmitting in 9-bit data format and using 8-bit write instructions, write first to SCI data register high (SCIDRH), then SCIDRL.

Table 11-11. Normal Mode and Bidirectional Mode

When SPE = 1	Master Mode MSTR = 1	Slave Mode MSTR = 0
Normal Mode SPC0 = 0		
Bidirectional Mode SPC0 = 1		

The direction of each serial I/O pin depends on the BIDIROE bit. If the pin is configured as an output, serial data from the shift register is driven out on the pin. The same pin is also the serial input to the shift register.

- The SCK is output for the master mode and input for the slave mode.
- The $\overline{SS}$ is the input or output for the master mode, and it is always the input for the slave mode.
- The bidirectional mode does not affect SCK and $\overline{SS}$ functions.

NOTE

In bidirectional master mode, with mode fault enabled, both data pins MISO and MOSI can be occupied by the SPI, though MOSI is normally used for transmissions in bidirectional mode and MISO is not used by the SPI. If a mode fault occurs, the SPI is automatically switched to slave mode. In this case MISO becomes occupied by the SPI and MOSI is not used. This must be considered, if the MISO pin is used for another purpose.

11.4.6 Error Conditions

The SPI has one error condition:

- Mode fault error

11.4.6.1 Mode Fault Error

If the $\overline{SS}$ input becomes low while the SPI is configured as a master, it indicates a system error where more than one master may be trying to drive the MOSI and SCK lines simultaneously. This condition is not permitted in normal operation, the MODF bit in the SPI status register is set automatically, provided the MODFEN bit is set.

In the special case where the SPI is in master mode and MODFEN bit is cleared, the $\overline{SS}$ pin is not used by the SPI. In this special case, the mode fault error function is inhibited and MODF remains cleared. In case

[1] The register is available only if corresponding channel exists.

12.3.2.1 Timer Input Capture/Output Compare Select (TIOS)

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	IOS3	IOS2	IOS1	IOS0
Reset	0	0	0	0	0	0	0	0

Figure 12-4. Timer Input Capture/Output Compare Select (TIOS)

Read: Anytime

Write: Anytime

Table 12-2. TIOS Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 IOS[3:0]	**Input Capture or Output Compare Channel Configuration** 0 The corresponding implemented channel acts as an input capture. 1 The corresponding implemented channel acts as an output compare.

12.3.2.2 Timer Compare Force Register (CFORC)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	RESERVED	RESERVED	RESERVED	RESERVED	FOC3	FOC2	FOC1	FOC0
Reset	0	0	0	0	0	0	0	0

Figure 12-5. Timer Compare Force Register (CFORC)

Read: Anytime but will always return 0x0000 (1 state is transient)

Write: Anytime

Table 12-3. CFORC Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 FOC[3:0]	**Note: Force Output Compare Action for Channel 3:0** — A write to this register with the corresponding data bit(s) set causes the action which is programmed for output compare “x” to occur immediately. The action taken is the same as if a successful comparison had just taken place with the TCx register except the interrupt flag does not get set. If forced output compare on any channel occurs at the same time as the successful output compare then forced output compare action will take precedence and interrupt flag won’t get set.

13.2 External Signal Description

Table 13-2 shows the external pins associated with the HSDRV module.

Table 13-2. HSDRV Signal Properties

Name	Function	Reset State
HS0	High-side driver output 0	disabled (off)
HS1	High-side driver output 1	disabled (off)
VSUPHS	High Voltage Power Supply for both high side drivers	disabled (off)

13.2.1 HS0, HS1— High Side Driver Pins

Outputs of the two high-side drivers are intended to drive LEDs or resistive loads.

13.2.2 VSUPHS — High Side Driver Power Pin

Power supply for both high-side drivers.

This pin must be connected to the main power supply with the appropriate reverse battery protection network.

13.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the HSDRV module.

13.3.1 Module Memory Map

A summary of registers associated with the HSDRV module is shown in Table 13-3. Detailed descriptions of the registers and bits are given in the following sections.

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Table 13-3. Register Summary

Address Offset Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 HSDR	R	0	0	0	0	0	0	HSDR1	HSDR0
	W								
0x0001 HSCR	R	0	0	HSOCME1	HSOCME0	0	0	HSE1	HSE0
	W								
0x0002 Reserved	R	0	0	0	0	0	0	0	0
	W								

13.4 Functional Description

13.4.1 General

The HSDRV module provides two high-side drivers able to drive LED or resistive loads. The driver can be controlled directly through register bits or alternatively by dedicated timer or PWM channels. See PIM chapter for routing details.

13.4.2 Over-Current Shutdown

Each high-side driver has an over-current shutdown feature with a current threshold of I_{OCTHSX}.

If an over-current is detected the related interrupt flag (HSOCIF1 or HSOCIF0) is set in the HSDRV Interrupt Flag Register (HSIF). As long as the over-current interrupt flag remains set, the related high-side driver is turned off to protect the circuit. Clearing the related over-current interrupt flag returns back the control to the selected source in the PIM module.

The over-current detection and driver shutdown can be masked for an initial T_{HSOCM} after switching the driver on. This can be achieved by writing the related HSOCME register bit in the HSCR register to 1. The HSOCME bits are only writable while the related driver is disabled (HSE=0).

13.4.3 Interrupts

This section describes the interrupt generated by HSDRV module. The interrupt is only available in MCU run mode. Entering and exiting MCU stop mode has no effect on the interrupt flags.

The HSDRV interrupt vector is named in Table 13-9. Vector addresses and interrupt priorities are defined at MCU level.

13.4.3.1 HSDRV Over Current Interrupt (HSOCI)

Table 13-9. HSDRV Interrupt Sources

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
HSDRV Interrupt (HSI)	HSDRV Over-Current Interrupt (HSOCI)	HSOCIE = 1

If an over-current is detected the related interrupt flag HSOCIFx asserts. Depending on the setting of the HSDRV Error Interrupt Enable (HSOCIE) bit an interrupt is requested.

Chapter 17
Supply Voltage Sensor - (BATSV2)

Table 17-1. Revision History Table

Rev. No. (Item No.)	Data	Sections Affected	Substantial Change(s)
V01.00	15 Dec 2010	all	Initial Version
V02.00	16 Mar 2011	17.3.2.1 17.4.2.1	- added BVLS[1] to support four voltage level - moved BVHS to register bit 6

17.1 Introduction

The BATS module provides the functionality to measure the voltage of the battery supply pin VSENSE or of the chip supply pin VSUP.

17.1.1 Features

Either One of the voltage present on the VSENSE or VSUP pin can be routed via an internal divider to the internal Analog to Digital Converter. Independent of the routing to the Analog to Digital Converter, it is possible to route one of these voltages to a comparator to generate a low or a high voltage interrupt to alert the MCU.

17.1.2 Modes of Operation

The BATS module behaves as follows in the system power modes:

1. Run mode

   The activation of the VSENSE Level Sense Enable (BSESE=1) or ADC connection Enable (BSEAE=1) closes the path from the VSENSE pin through the resistor chain to ground and enables the associated features if selected.

   The activation of the VSUP Level Sense Enable (BSUSE=1) or ADC connection Enable (BSUAE=1) closes the path from VSUP pin through the resistor chain to ground and enables the associated features if selected.

   BSESE takes precedence over BSUSE. BSEAE takes precedence over BSUAE.

2. Stop mode

   During stop mode operation the path from the VSENSE pin through the resistor chain to ground is opened and the low voltage sense features are disabled.

When opening the resistors path to ground by changing BSESE, BSEAE or BSUSE, BSUAE then for a time T_{EN_UNC} + two bus cycles the measured value is invalid. This is to let internal nodes be charged to correct value. BVHIE, BVLIE might be cleared for this time period to avoid false interrupts.

Chapter 18
64 KByte Flash Module (S12FTMRG64K512V1) for S12VR64

Table 18-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.00	17 Jun 2010	18.4.6.1/18-505 18.4.6.2/18-506 18.4.6.3/18-506 18.4.6.14/18-516	Clarify Erase Verify Commands Descriptions related to the bits MGSTAT[1:0] of the register FSTAT.
V01.01	31 aug 2010	18.4.6.2/18-506 18.4.6.12/18-513 18.4.6.13/18-514	Updated description of the commands RD1BLK, MLOADU and MLOADF
V01.02	31 Jan 2011	18.3.2.9/18-490	Updated description of protection on Section 18.3.2.9 P-Flash Protection Register (FPROT)
V01.03	04 Oct 2013	18.3.2.9/18-490 18.3.2.10/18-493	Updated notes regarding restrictions to change Protection in Special Single Chip Mode (SS)

Table 18-49. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 18-27)
		Set if an invalid global address [17:16] is supplied see)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

18.4.6.10 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and EEPROM memory space and, if the erase is successful, will release security.

Table 18-50. Unsecure Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and EEPROM memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security state. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag is set after the Unsecure Flash operation has completed.

Table 18-51. Unsecure Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 18-27)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

18.4.6.11 Verify Backdoor Access Key Command

The Verify Backdoor Access Key command will only execute if it is enabled by the KEYEN bits in the FSEC register (see Table 18-10). The Verify Backdoor Access Key command releases security if user-supplied keys match those stored in the Flash security bytes of the Flash configuration field (see Table 18-4). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

All bits in the FRSV5 register read 0 and are not writable.

19.3.2.18 Flash Reserved6 Register (FRSV6)

This Flash register is reserved for factory testing.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-24. Flash Reserved6 Register (FRSV6)

All bits in the FRSV6 register read 0 and are not writable.

19.3.2.19 Flash Reserved7 Register (FRSV7)

This Flash register is reserved for factory testing.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-25. Flash Reserved7 Register (FRSV7)

All bits in the FRSV7 register read 0 and are not writable.

19.4 Functional Description

19.4.1 Modes of Operation

The FTMRG32K128 module provides the modes of operation normal and special . The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, FPROT and EEPROT registers (see Table 19-27).

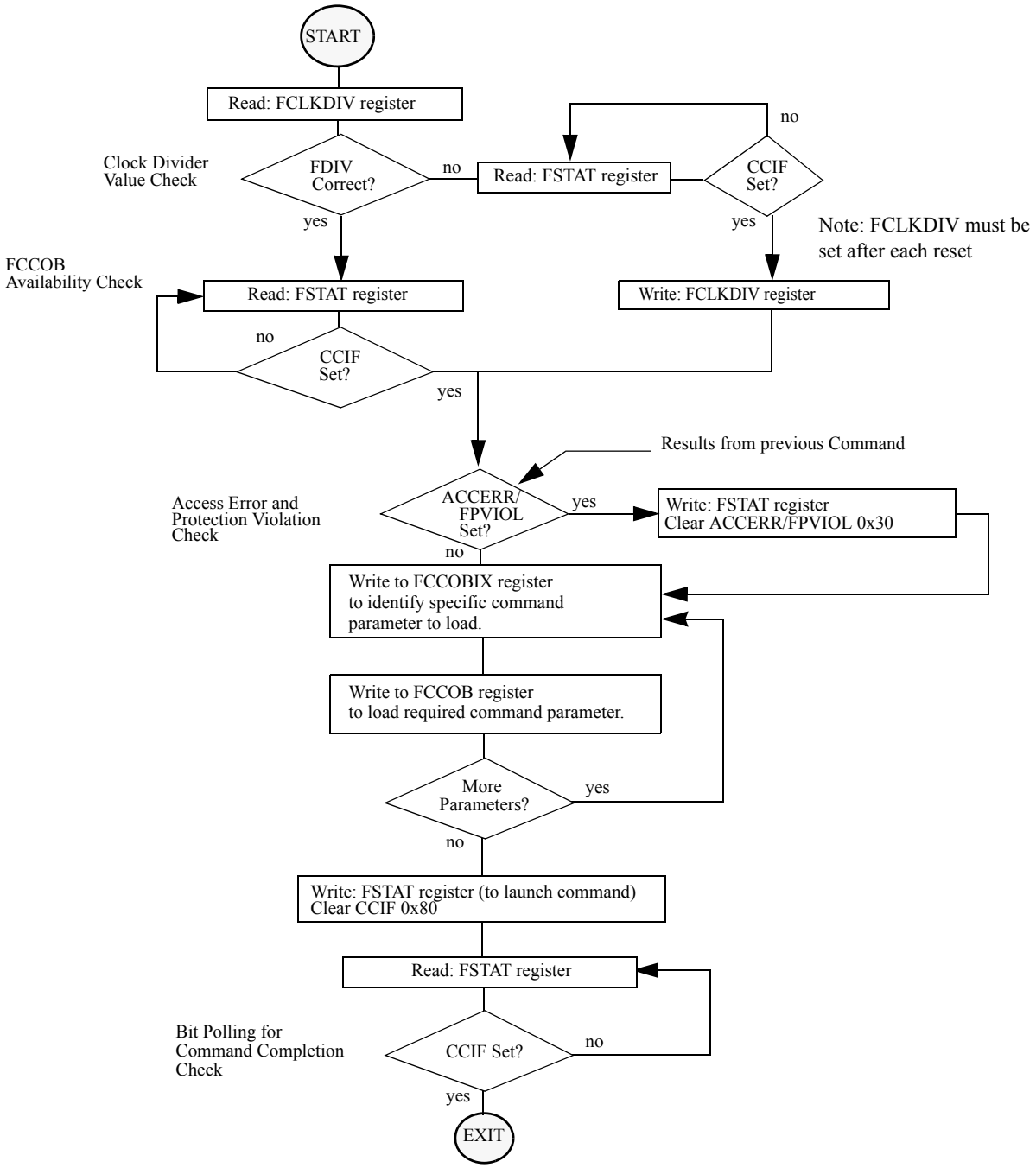


Figure 19-26. Generic Flash Command Write Sequence Flowchart

19.4.6.2 Erase Verify Block Command

The Erase Verify Block command allows the user to verify that an entire P-Flash or EEPROM block has been erased. The FCCOB FlashBlockSelectionCode[1:0]bits determine which block must be verified.

Table 19-33. Erase Verify Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x02	Flash block selection code [1:0]. See Table 19-34

Table 19-34. Flash block selection code description

Selection code[1:0]	Flash block to be verified
00	EEPROM
01	Invalid (ACCERR)
10	Invalid (ACCERR)
11	P-Flash

Upon clearing CCIF to launch the Erase Verify Block command, the Memory Controller will verify that the selected P-Flash or EEPROM block is erased. The CCIF flag will set after the Erase Verify Block operation has completed.If the block is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 19-35. Erase Verify Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

19.4.6.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases.

P.23 0x0140-0x0147 High Side Drivers

P.23.1 S12HSDRVV2 on MC9S12VR64/48

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0140	HSDR	R	0	0	0	0	0	0	HSDR1	HSDR0
		W								
0x0141	HSCR	R	0	0	HSOCME1	HSOCME0	0	0	HSE1	HSE0
		W								
0x0142	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0143	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0144	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0145	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0146	HSIE	R	HSOCIE	0	0	0	0	0	0	0
		W								
0x0147	HSIF	R	0	0	0	0	0	0	HSOCIF1	HSOCIF0
		W								

P.23.2 S12HSDRV1CV3 on MC9S12VR32/16

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0140	HSDR	R	0	0	0	0	0	0	0	HSDR0
		W								
0x0141	HSCR	R	0	0	0	HSOCME0	0	HSOLE0	0	HSE0
		W								
0x0142	HSSLR	R	0	0	0	0	0	HSSLCU0	0	HSSLEN0
		W								
0x0143	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0144	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0145	Reserved	R	0	0	0	0	0	0	0	HSOL0
		W								
0x0146	HSIE	R	HSOCIE	0	0	0	0	0	0	0
		W								
0x0147	HSIF	R	0	0	0	0	0	0	0	HSOCIF0
		W								

P.34 0x0300-0x03FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0300-0x03FF	Reserved	R	0	0	0	0	0	0	0	0
		W								