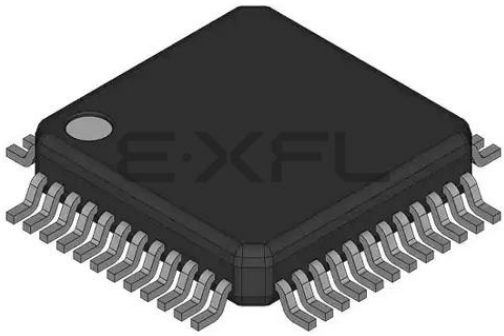

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vr64af0clf

- Clock monitor supervising the correct function of the oscillator

1.4.9 Timer (TIM)

- Up to 4 x 16-bit channels for input capture or output compare
- 16-bit free-running counter with 8-bit precision prescaler

1.4.10 Pulse Width Modulation Module (PWM)

- Up to eight 8-bit channels or reconfigurable four 16-bit channel PWM resolution
  - — Programmable period and duty cycle per channel
  - — Center-aligned or left-aligned outputs
  - — Programmable clock select logic with a wide range of frequencies

1.4.11 LIN physical layer transceiver (LINPHY)

- Compliant with LIN Physical Layer 2.2 specification.
- Compliant with the SAE J2602-2 LIN standard.
- Standby mode with glitch-filtered wake-up.
- Slew rate selection optimized for the baud rates: 10.4kBit/s, 20kBit/s and Fast Mode (up to 250kBit/s).
- Switchable 34kΩ/330kΩ pull-ups (in shutdown mode, 330kΩ only)
- Current limitation for LIN Bus pin falling edge.
- Over-current protection.
- LIN TxD-dominant timeout feature monitoring the LPTxD signal.
- Automatic transmitter shutdown in case of an over-current or TxD-dominant timeout.
- Fulfills the OEM “Hardware Requirements for LIN (CAN and FlexRay) Interfaces in Automotive Applications” v1.3.
- Internal connection to one SCI routable to external pins

1.4.12 Serial Peripheral Interface Module (SPI)

- Configurable 8- or 16-bit data size
- Full-duplex or single-wire bidirectional
- Double-buffered transmit and receive
- Master or slave
- MSB-first or LSB-first shifting
- Serial clock phase and polarity options

— Optional HVI to ADC link

A standard port pin has the following minimum features:

- Input/output selection
- 5 V output drive
- 5 V digital and analog input
- Input with selectable pullup or pulldown device

Optional features supported on dedicated pins:

- Two selectable output drive strengths
- Open drain for wired-or connections
- Interrupt input with glitch filtering
- High-voltage input
- 10 mA high-current output
- 20 mA high-current output with over-current protection for use as Hall sensor supply

2.2 External Signal Description

This section lists and describes the signals that do connect off-chip.

Table 2-2 shows all the pins and their functions that are controlled by the PIM. Routing options are denoted in parenthesis.

NOTE

If there is more than one function associated with a pin, the **output** priority is indicated by the position in the table from top (highest priority) to bottom (lowest priority).

Table 2-2. Pin Functions and Priorities[1]

Port	Pin Name	Pin Function & Priority[1]	I/O	Description	Pin Function after Reset
-	BKGD	MODC[2]	I	MODC input during $\overline{\text{RESET}}$	BKGD
		BKGD	I/O	BDM communication pin	
E	PE1	XTAL	-	CPMU OSC signal	GPIO
		PTE[1]	I/O	General-purpose	
	PE0	EXTAL	-	CPMU OSC signal	
		PTE[0]	I/O	General-purpose	

Global Address	Register Name[1]		Bit 7	6	5	4	3	2	1	Bit 0
0x025A	DDRP	R	0	0	**DDRP5**	**DDRP4**	**DDRP3**	DDRP2	DDRP1	**DDRP0**
		W								
0x025B	RDRP	R	0	0	0	0	0	RDRP2	RDRP1	**RDRP0**
		W								
0x025C	PERP	R	0	0	**PERP5**	**PERP4**	**PERP3**	PERP2	PERP1	**PERP0**
		W								
0x025D	PPSP	R	0	0	**PPSP5**	**PPSP4**	**PPSP3**	PPSP2	PPSP1	**PPSP0**
		W								
0x025E	PIEP	R	OCIE	0	**PIEP5**	**PIEP4**	**PIEP3**	PIEP2	PIEP1	**PIEP0**
		W								
0x025F	PIFP	R	OCIF	0	**PIFP5**	**PIFP4**	**PIFP3**	PIFP2	PIFP1	**PIFP0**
		W								
0x0260–0x0268	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0269	PTIL	R	0	0	0	0	PTIL3	PTIL2	PTIL1	PTIL0
		W								
0x026A	DIENL	R	0	0	0	0	DIENL3	DIENL2	DIENL1	DIENL0
		W								
0x026B	PTAL	R	PTTEL	PTPSL	PTABYPL	PTADIRL	PTAENL	0	PTAL1	PTAL0
		W								
0x026C	PIRL	R	0	0	0	0	PIRL3	PIRL2	PIRL1	PIRL0
		W								
0x026D	PPSL	R	0	0	0	0	PPSL3	PPSL2	PPSL1	PPSL0
		W								
0x026E	PIEL	R	0	0	0	0	PIEL3	PIEL2	PIEL1	PIEL0
		W								
0x026F	PIFL	R	0	0	0	0	PIFL3	PIFL2	PIFL1	PIFL0
		W								
0x0270	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0271	PT1AD	R	0	0	**PT1AD5**	**PT1AD4**	**PT1AD3**	**PT1AD2**	PT1AD1	PT1AD0
		W								

Table 2-9. IRQCR Register Field Descriptions

Field	Description
7 IRQE	**IRQ select Edge sensitive only** — 1 $\overline{\text{IRQ}}$ pin configured to respond only to falling edges. Falling edges on the $\overline{\text{IRQ}}$ pin will be detected anytime IRQE=1 and will be cleared only upon a reset or the servicing of the $\overline{\text{IRQ}}$ interrupt. 0 $\overline{\text{IRQ}}$ pin configured for low level recognition
6 IRQEN	**IRQ ENable** — 1 $\overline{\text{IRQ}}$ pin is connected to interrupt logic 0 $\overline{\text{IRQ}}$ pin is disconnected from interrupt logic

2.3.9 Reserved Register

Address 0x001E (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-7. Reserved Register

[1] Read: Anytime
Write:Never

2.3.10 Reserved Register

Address 0x001F Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 2-8. Reserved Register

[1] Read: Anytime
Write: Only in special mode

NOTE

These reserved registers are designed for factory test purposes only and are not intended for general user access. Writing to these registers when in special modes can alter the module's functionality.

[1] Read: Anytime
Write: Anytime

Table 2-12. DDRT Register Field Descriptions

Field	Description
3 DDRT	**Data Direction Register port T —** This bit determines whether the pin is an input or output Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. The enabled routed LINPHY forces the I/O state to be an input (LPTXD). Else the TIM forces the I/O state to be an output for a TIM port associated with an enabled TIM output compare. In these cases the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
2 DDRT	**Data Direction Register port T —** This bit determines whether the pin is an input or output. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. The enabled routed LINPHY forces the I/O state to be an output (LPRXD). Else the TIM forces the I/O state to be an output for a TIM port associated with an enabled TIM output compare. In these cases the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
1-0 DDRT	**Data Direction Register port T —** This bit determines whether the pin is an input or output. Depending on the configuration of the enabled routed SCI0 the I/O state will be forced to be input or output. The enabled routed LINPHY forces the I/O state to be an output (LPDR[LPDR1]). Else the TIM forces the I/O state to be an output for a TIM port associated with an enabled TIM output compare. In these cases the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input

2.3.14 Port T Pull Device Enable Register (PERT)

Address 0x0244 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PERT3	PERT2	PERT1	PERT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-12. Port T Pull Device Enable Register (PERT)

[1] Read: Anytime
Write: Anytime

Table 2-13. PERT Register Field Descriptions

Field	Description
3-0 PERT	**Pull device Enable Register port T** — Enable pull device on input pin This bit controls whether a pull device on the associated port input pin is active. If a pin is used as output this bit has no effect. The polarity is selected by the related polarity select register bit. 1 Pull device enabled 0 Pull device disabled

2.3.25 Module Routing Register 2 (MODRR2)

Address 0x024F (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	MODRR27	0	MODRR25	MODRR24	MODRR23	MODRR22	MODRR21	MODRR20
W								
Routing Option	LPRXD to TIM	—	SPI $\overline{SS}$ and SCK	SCI1	SCI0-to-LINPHY interface			
Reset	0	0	0	0	0	0	0	0

Figure 2-30. Module Routing Register 2 (MODRR2 - S12VR64/48)

[1] Read: Anytime
Write: Once in normal, anytime in special mode

Address 0x024F (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	MODRR27	0	0	0	0	MODRR22	MODRR21	MODRR20
W								
Routing Option	LPRXD to TIM	—	—	—	—	SCI0-to-LINPHY interface		
Reset	0	0	0	0	0	0	0	0

Figure 2-31. Module Routing Register 2 (MODRR2 - S12VR32/16)

[1] Read: Anytime
Write: Once in normal, anytime in special mode

Table 2-23. Module Routing Register 2 Field Descriptions

Field	Description
7 MODRR2	**MODule Routing Register 2** — TIM routing 1 TIM input capture channel 3 is connected to LPRXD 0 TIM input capture channel 3 is connected to PT3
5 MODRR2	**MODule Routing Register 2** — SPI $\overline{SS}$ and SCK routing 1 $\overline{SS}$ on PT3; SCK on PT2 0 $\overline{SS}$ on PS5; SCK on PS4
4 MODRR2	**MODule Routing Register 2** — SCI1 routing 1 TXD1 on PS3; RXD1 on PS2 0 TXD1 on PS1; RXD1 on PS0
3-0 MODRR2	**MODule Routing Register 2** — SCI0-to-LINPHY routing Selection of SCI0-to-LINPHY interface routing options to support probing and conformance testing. Refer to Figure 2-32 for an illustration and Table 2-24 for preferred settings. SCI0 must be enabled for TXD0 routing to take effect on pins. LINPHY must be enabled for LPRXD and LPDR[LPDR1] routings to take effect on pins.

Chapter 3
S12G Memory Map Controller (S12GMMCV1)

Table 3-1. Revision History Table

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
01.02	20-May 2010		Updates for S12VR48 and S12VR64
01.03	14-Feb 2014		Added S12VR32

3.1 Introduction

The S12GMMC module controls the access to all internal memories and peripherals for the CPU12 and S12SBDM module. It regulates access priorities and determines the address mapping of the on-chip resources. Figure 3-1 shows a block diagram of the S12GMMC module.

3.1.1 Glossary

Table 3-2. Glossary Of Terms

Term	Definition
Local Addresses	Address within the CPU12's Local Address Map (Figure 3-11)
Global Address	Address within the Global Address Map (Figure 3-11)
Aligned Bus Access	Bus access to an even address.
Misaligned Bus Access	Bus access to an odd address.
NS	Normal Single-Chip Mode
SS	Special Single-Chip Mode
Unimplemented Address Ranges	Address ranges which are not mapped to any on-chip resource.
NVM	Non-volatile Memory; Flash or EEPROM
IFR	NVM Information Row. Refer to FTMRG Block Guide

3.1.2 Overview

The S12GMMC connects the CPU12's and the S12SBDM's bus interfaces to the MCU's on-chip resources (memories and peripherals). It arbitrates the bus accesses and determines all of the MCU's memory maps. Furthermore, the S12GMMC is responsible for constraining memory accesses on secured devices and for selecting the MCU's functional mode.

4.2 Signal Description

This section lists and describes the signals that connect off chip as well as internal supply nodes and special signals.

4.2.1 $\overline{\text{RESET}}$

Pin $\overline{\text{RESET}}$ is an active-low bidirectional pin. As an input it initializes the MCU asynchronously to a known start-up state. As an open-drain output it indicates that an MCU-internal reset has been triggered.

4.2.2 EXTAL and XTAL

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. If XOSCLCP is enabled, the MCU internal OSCCLK_LCP is derived from the EXTAL input frequency. If OSCE=0, the EXTAL pin is pulled down by an internal resistor of approximately 200 kΩ and the XTAL pin is pulled down by an internal resistor of approximately 700 kΩ.

NOTE

NXP recommends an evaluation of the application board and chosen resonator or crystal by the resonator or crystal supplier.
The loop controlled circuit (XOSCLCP) is not suited for overtone resonators and crystals.

4.2.3 VSUP — Regulator Power Input Pin

Pin VSUP is the power input of VREGAUTO. All currents sourced into the regulator loads flow through this pin.

An appropriate reverse battery protection network consisting of a diode and capacitors is recommended.

4.2.4 VDDA, VSSA — Regulator Reference Supply Pins

Pins VDDA and VSSA are used to supply the analog parts of the regulator.
Internal precision reference circuits are supplied from these signals.

A local decoupling capacitor between VDDA and VSSA according to the electrical specification is required. Additionally a bigger tank capacitor is required on the 5 Volt supply network as well to ensure Voltage regulator stability.

VDDA has to be connected externally to VDDX.

4.2.5 VDDX, VSSX— Pad Supply Pins

This supply domain is monitored by the Low Voltage Reset circuit.

A local decoupling capacitor between VDDX and VSSX according to the electrical specification is required.

4.7.2 Application information for COP and API usage

In many applications the COP is used to check that the program is running and sequencing properly. Often the COP is kept running during Stop Mode and periodic wake-up events are needed to service the COP on time and maybe to check the system status.

For such an application it is recommended to use the ACLK as clock source for both COP and API. This guarantees lowest possible IDD current during Stop Mode. Additionally it eases software implementation using the same clock source for both, COP and API.

The Interrupt Service Routine (ISR) of the Autonomous Periodic Interrupt API should contain the write instruction to the CPMUARMCOP register. The value (byte) written is derived from the “main routine” (alternating sequence of $55 and $AA) of the application software.

Using this method, then in the case of a runtime or program sequencing issue the application “main routine” is not executed properly anymore and the alternating values are not provided properly. Hence the COP is written at the correct time (due to independent API interrupt request) but the wrong value is written (alternating sequence of $55 and $AA is no longer maintained) which causes a COP reset.

If the COP is stopped during any Stop Mode it is recommended to service the COP shortly before Stop Mode is entered.

8.3.2 Register Descriptions

This section describes in address order all the ADC12B6CV2 registers and their individual bits.

8.3.2.1 ATD Control Register 0 (ATDCTL0)

Writes to this register will abort current conversion sequence.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 8-3. ATD Control Register 0 (ATDCTL0)

Read: Anytime

Write: Anytime, in special modes always write 0 to Reserved Bit 7.

Table 8-1. ATDCTL0 Field Descriptions

Field	Description
3-0 WRAP[3-0]	**Wrap Around Channel Select Bits** — These bits determine the channel for wrap around when doing multi-channel conversions. The coding is summarized in Table 8-2.

Table 8-2. Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple Channel Conversions (MULT = 1) Wraparound to AN0 after Converting
0	0	0	0	Reserved[1]
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN5
0	1	1	1	AN5
1	0	0	0	AN5
1	0	0	1	AN5
1	0	1	0	AN5
1	0	1	1	AN5
1	1	0	0	AN5
1	1	0	1	AN5
1	1	1	0	AN5
1	1	1	1	AN5

9.2.1 PWM7 - PWM0 — PWM Channel 7 - 0

Those pins serve as waveform output of PWM channel 7 - 0.

9.3 Memory Map and Register Definition

9.3.1 Module Memory Map

This section describes the content of the registers in the scalable PWM module. The base address of the scalable PWM module is determined at the MCU level when the MCU is defined. The register decode map is fixed and begins at the first address of the module address offset. The figure below shows the registers associated with the scalable PWM and their relative offset from the base address. The register detail description follows the order they appear in the register map.

Reserved bits within a register will always read as 0 and the write will be unimplemented. Unimplemented functions are indicated by shading the bit.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

9.3.2 Register Descriptions

This section describes in detail all the registers and register bits in the scalable PWM module.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
PWME[1]	R W	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
PWMPOL[1]	R W	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
PWMCLK[1]	R W	PCLK7	PCLKL6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
PWMPRCLK	R W	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
PWMCAE[1]	R W	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
PWMCTL[1]	R W	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		= Unimplemented or Reserved							

Figure 9-2. The scalable PWM Register Summary (Sheet 1 of 4)

	7	6	5	4	3	2	1	0
R W	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
Reset	0	0	0	0	0	0	0	0

Figure 9-4. PWM Polarity Register (PWMPOL)

Read: Anytime

Write: Anytime

NOTE

PPOLx register bits can be written anytime. If the polarity is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition

Table 9-3. PWMPOL Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7–0 PPOL[7:0]	**Pulse Width Channel 7–0 Polarity Bits** 0 PWM channel 7–0 outputs are low at the beginning of the period, then go high when the duty count is reached. 1 PWM channel 7–0 outputs are high at the beginning of the period, then go low when the duty count is reached.

9.3.2.3 PWM Clock Select Register (PWMCLK)

Each PWM channel has a choice of four clocks to use as the clock source for that channel as described below.

	7	6	5	4	3	2	1	0
R W	PCLK7	PCLKL6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
Reset	0	0	0	0	0	0	0	0

Figure 9-5. PWM Clock Select Register (PWMCLK)

Read: Anytime

Write: Anytime

NOTE

Register bits PCLK0 to PCLK7 can be written anytime. If a clock select is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Table 9-11. PWMCLK Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7 PCLKAB7	**Pulse Width Channel 7 Clock A/B Select** 0 Clock B or SB is the clock source for PWM channel 7, as shown in Table 9-6. 1 Clock A or SA is the clock source for PWM channel 7, as shown in Table 9-6.
6 PCLKAB6	**Pulse Width Channel 6 Clock A/B Select** 0 Clock B or SB is the clock source for PWM channel 6, as shown in Table 9-6. 1 Clock A or SA is the clock source for PWM channel 6, as shown in Table 9-6.
5 PCLKAB5	**Pulse Width Channel 5 Clock A/B Select** 0 Clock A or SA is the clock source for PWM channel 5, as shown in Table 9-5. 1 Clock B or SB is the clock source for PWM channel 5, as shown in Table 9-5.
4 PCLKAB4	**Pulse Width Channel 4 Clock A/B Select** 0 Clock A or SA is the clock source for PWM channel 4, as shown in Table 9-5. 1 Clock B or SB is the clock source for PWM channel 4, as shown in Table 9-5.
3 PCLKAB3	**Pulse Width Channel 3 Clock A/B Select** 0 Clock B or SB is the clock source for PWM channel 3, as shown in Table 9-6. 1 Clock A or SA is the clock source for PWM channel 3, as shown in Table 9-6.
2 PCLKAB2	**Pulse Width Channel 2 Clock A/B Select** 0 Clock B or SB is the clock source for PWM channel 2, as shown in Table 9-6. 1 Clock A or SA is the clock source for PWM channel 2, as shown in Table 9-6.
1 PCLKAB1	**Pulse Width Channel 1 Clock A/B Select** 0 Clock A or SA is the clock source for PWM channel 1, as shown in Table 9-5. 1 Clock B or SB is the clock source for PWM channel 1, as shown in Table 9-5.
0 PCLKAB0	**Pulse Width Channel 0 Clock A/B Select** 0 Clock A or SA is the clock source for PWM channel 0, as shown in Table 9-5. 1 Clock B or SB is the clock source for PWM channel 0, as shown in Table 9-5.

The clock source of each PWM channel is determined by PCLKx bits in PWMCLK (see Section 9.3.2.3, “PWM Clock Select Register (PWMCLK)) and PCLKABx bits in PWMCLKAB as shown in Table 9-5 and Table 9-6.

9.3.2.8 PWM Scale A Register (PWMSCLA)

PWMSCLA is the programmable scale value used in scaling clock A to generate clock SA. Clock SA is generated by taking clock A, dividing it by the value in the PWMSCLA register and dividing that by two.

Clock SA = Clock A / (2 * PWMSCLA)

NOTE

When PWMSCLA = $00, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

Any value written to this register will cause the scale counter to load the new scale value (PWMSCLA).

9.4.2 PWM Channel Timers

The main part of the PWM module are the actual timers. Each of the timer channels has a counter, a period register and a duty register (each are 8-bit). The waveform output period is controlled by a match between the period register and the value in the counter. The duty is controlled by a match between the duty register and the counter value and causes the state of the output to change during the period. The starting polarity of the output is also selectable on a per channel basis. Shown below in Figure 9-16 is the block diagram for the PWM timer.

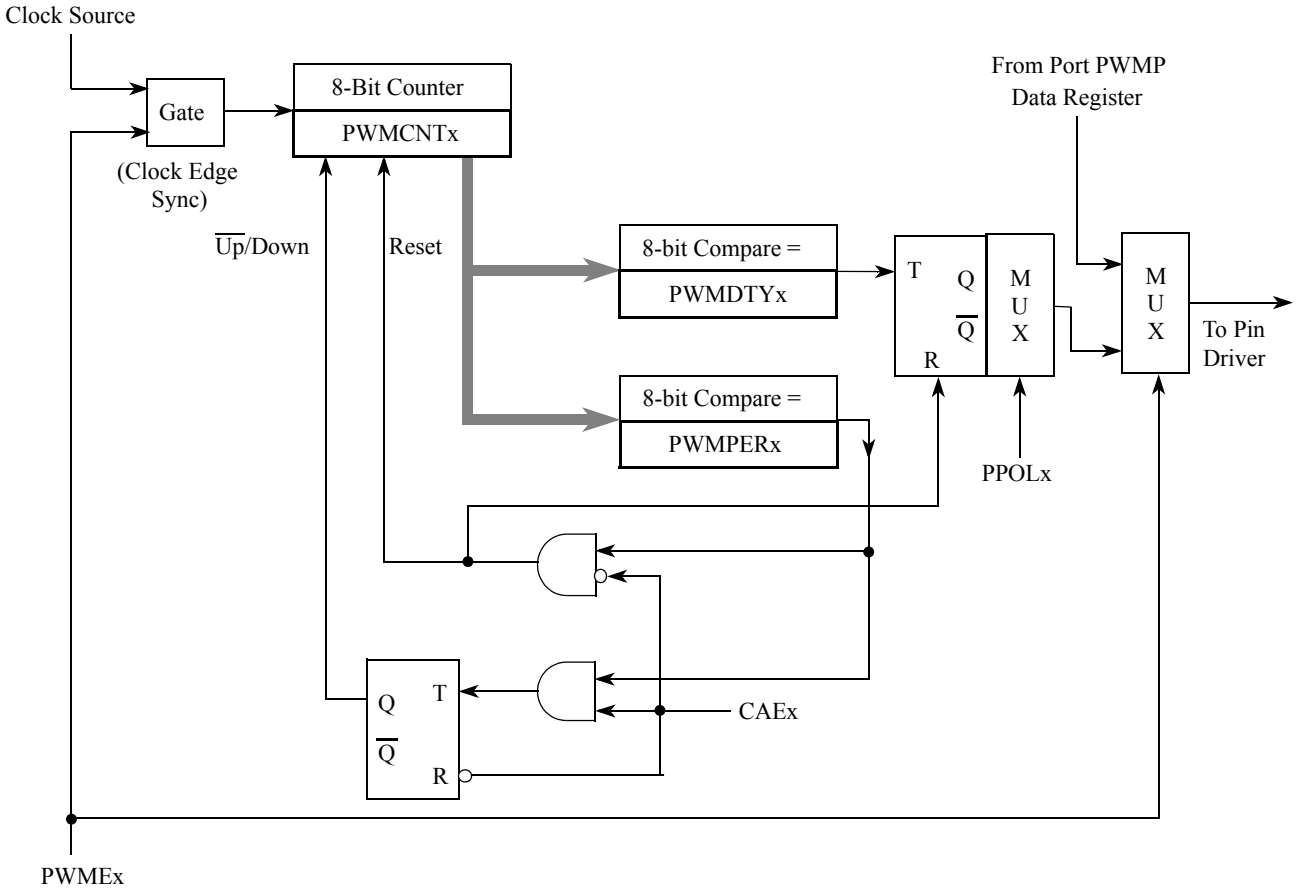


Figure 9-16. PWM Timer Channel Block Diagram

9.4.2.1 PWM Enable

Each PWM channel has an enable bit (PWMEx) to start its waveform output. When any of the PWMEx bits are set (PWMEx = 1), the associated PWM output signal is enabled immediately. However, the actual PWM waveform is not available on the associated PWM output until its clock source begins its next cycle due to the synchronization of PWMEx and the clock source. An exception to this is when channels are concatenated. Refer to Section 9.4.2.7, “PWM 16-Bit Functions” for more detail.

NOTE

The first PWM cycle after enabling the channel can be irregular.

10.5.3.1.6 RXEDGIF Description

The RXEDGIF interrupt is set when an active edge (falling if RXPOL = 0, rising if RXPOL = 1) on the RXD pin is detected. Clear RXEDGIF by writing a “1” to the SCIASR1 SCI alternative status register 1.

10.5.3.1.7 BERRIF Description

The BERRIF interrupt is set when a mismatch between the transmitted and the received data in a single wire application like LIN was detected. Clear BERRIF by writing a “1” to the SCIASR1 SCI alternative status register 1. This flag is also cleared if the bit error detect feature is disabled.

10.5.3.1.8 BKDIF Description

The BKDIF interrupt is set when a break signal was received. Clear BKDIF by writing a “1” to the SCIASR1 SCI alternative status register 1. This flag is also cleared if break detect feature is disabled.

10.5.4 Recovery from Wait Mode

The SCI interrupt request can be used to bring the CPU out of wait mode.

10.5.5 Recovery from Stop Mode

An active edge on the receive input can be used to bring the CPU out of stop mode.

13.4 Functional Description

13.4.1 General

The HSDRV module provides two high-side drivers able to drive LED or resistive loads. The driver can be controlled directly through register bits or alternatively by dedicated timer or PWM channels. See PIM chapter for routing details.

13.4.2 Over-Current Shutdown

Each high-side driver has an over-current shutdown feature with a current threshold of I_{OCTHSX}.

If an over-current is detected the related interrupt flag (HSOCIF1 or HSOCIF0) is set in the HSDRV Interrupt Flag Register (HSIF). As long as the over-current interrupt flag remains set, the related high-side driver is turned off to protect the circuit. Clearing the related over-current interrupt flag returns back the control to the selected source in the PIM module.

The over-current detection and driver shutdown can be masked for an initial T_{HSOCM} after switching the driver on. This can be achieved by writing the related HSOCME register bit in the HSCR register to 1. The HSOCME bits are only writable while the related driver is disabled (HSE=0).

13.4.3 Interrupts

This section describes the interrupt generated by HSDRV module. The interrupt is only available in MCU run mode. Entering and exiting MCU stop mode has no effect on the interrupt flags.

The HSDRV interrupt vector is named in Table 13-9. Vector addresses and interrupt priorities are defined at MCU level.

13.4.3.1 HSDRV Over Current Interrupt (HSOCI)

Table 13-9. HSDRV Interrupt Sources

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
HSDRV Interrupt (HSI)	HSDRV Over-Current Interrupt (HSOCI)	HSOCIE = 1

If an over-current is detected the related interrupt flag HSOCIFx asserts. Depending on the setting of the HSDRV Error Interrupt Enable (HSOCIE) bit an interrupt is requested.

17.3.2.1 BATS Module Enable Register (BATE)

Module Base + 0x0000 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	BVHS	BVLS[1:0]		BSUAE	BSUSE	BSEAE	BSESE
W								
Reset	0	0	0	0	0	0	0	1

= Unimplemented

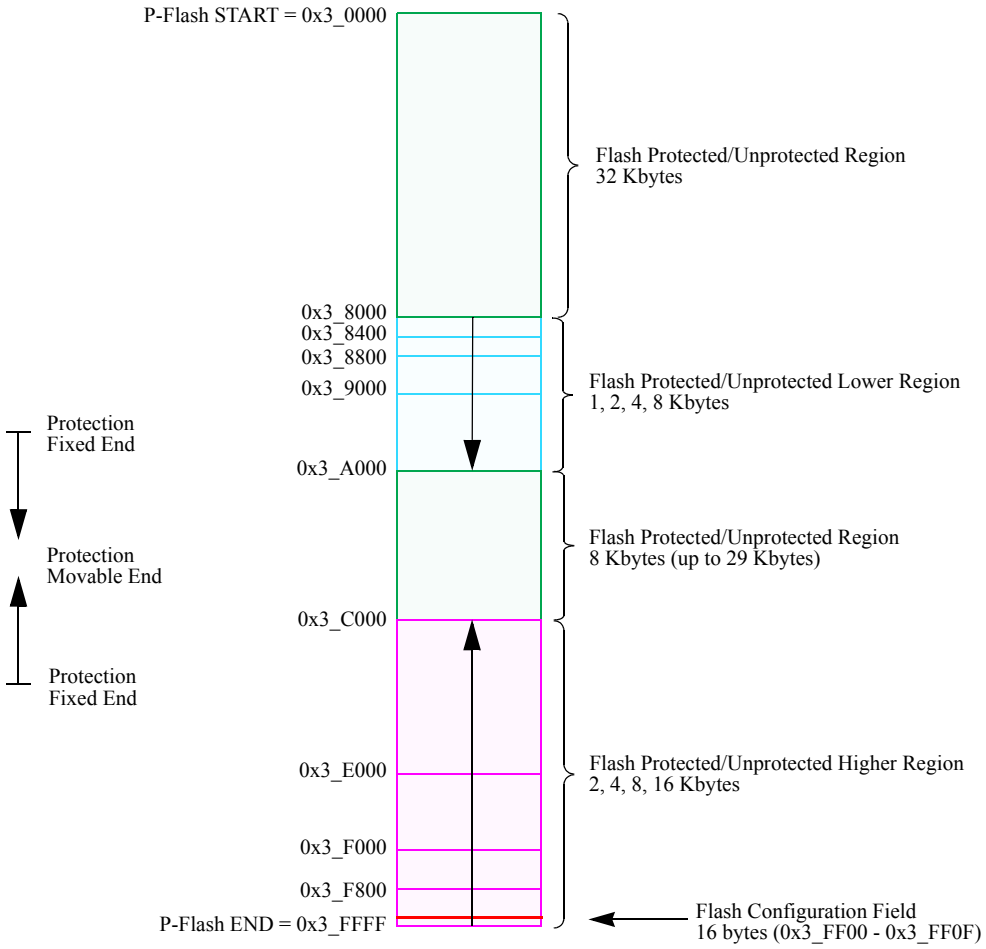
Figure 17-3. BATS Module Enable Register (BATE)

[1] Read: Anytime
Write: Anytime

Table 17-2. BATE Field Description

Field	Description
6 BVHS	**BATS Voltage High Select** — This bit selects the trigger level for the Voltage Level High Condition (BVHC). 0 Voltage level V_{HBI1} is selected 1 Voltage level V_{HBI2} is selected
5:4 BVLS[1:0]	**BATS Voltage Low Select** — This bit selects the trigger level for the Voltage Level Low Condition (BVLC). 00 Voltage level V_{LBI1} is selected 01 Voltage level V_{LBI2} is selected 10 Voltage level V_{LBI3} is selected 11 Voltage level V_{LBI4} is selected
3 BSUAE	**BATS VSUP ADC Connection Enable** — This bit connects the VSUP pin through the resistor chain to ground and connects the ADC channel to the divided down voltage. This bit can be set only if the BSEAE bit is cleared. 0 ADC Channel is disconnected 1 ADC Channel is connected
2 BSUSE	**BATS VSUP Level Sense Enable** — This bit connects the VSUP pin through the resistor chain to ground and enables the Voltage Level Sense features measuring BVLC and BVHC. This bit can be set only if the BSESE bit is cleared. 0 Level Sense features disabled 1 Level Sense features enabled
1 BSEAE	**BATS VSENSE ADC Connection Enable** — This bit connects the VSENSE pin through the resistor chain to ground and connects the ADC channel to divided down voltage. Setting this bit will clear bit BSUAE . 0 ADC Channel is disconnected 1 ADC Channel is connected
0 BSESE	**BATS VSENSE Level Sense Enable** — This bit connects the VSENSE pin through the resistor chain to ground and enables the Voltage Level Sense features measuring BVLC and BVHC.Setting this bit will clear bit BSUSE 0 Level Sense features disabled 1 Level Sense features enabled

NOTE


P-Flash START = 0x3_0000
Flash Protected/Unprotected Region
32 Kbytes
0x3_8000
0x3_8400
0x3_8800
0x3_9000
Flash Protected/Unprotected Lower Region
1, 2, 4, 8 Kbytes
Protection
Fixed End
0x3_A000
Flash Protected/Unprotected Region
8 Kbytes (up to 29 Kbytes)
Protection
Movable End
0x3_C000
Protection
Fixed End
0x3_E000
Flash Protected/Unprotected Higher Region
2, 4, 8, 16 Kbytes
0x3_F000
0x3_F800
P-Flash END = 0x3_FFFF
Flash Configuration Field
16 bytes (0x3_FF00 - 0x3_FF0F)

P.5 0x0010-0x0017 Module Mapping Control (MMC) Map 2 of 2

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0010	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0011	DIRECT	R	DP15	DP14	DP13	DP12	DP11	DP10	DP9	DP8
		W								
0x0012	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0013	Reserved	R	0	0	0	0	0	0	0	NVMRES
		W								
0x0014	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0015	PPAGE	R	0	0	0	0	PIX3	PIX2	PIX1	PIX0
		W								
0x0016	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0017	Reserved	R	0	0	0	0	0	0	0	0
		W								

P.6 0x0018-0x0019 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0018	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0019	Reserved	R	0	0	0	0	0	0	0	0
		W								

P.7 0x001A-0x001B Part ID Registers

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x001A	PARTIDH	R	PARTIDH							
		W								
0x001B	PARTIDL	R	PARTIDL							
		W								