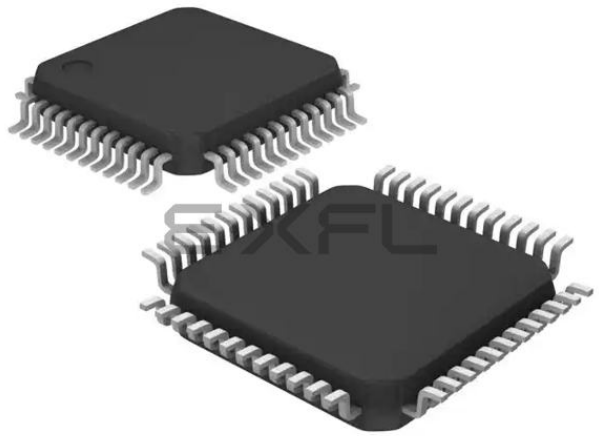


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vr64af0mlf

1.11.5 Flash IFR Mapping

Table 1-13. Flash IFR Mapping

IFR Byte Address	Target															
	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0x405A - 0x405B							ADC Bandgap Reference[1]									
0x40B8 - 0x40B9			ACLKTR[5:0][2]										HTTR[3:0][3]			
0x40BA - 0x40BB		TCTRIM[4:0][4]					IRCTRIM[9:0][4]									

1 see Section 1.12.1 ADC Calibration

2 see Section 4.3.2.16 Autonomous Clock Trimming Register (CPMUACLKTR)

3 see Section 4.3.2.19 High Temperature Trimming Register (CPMUHTTR)

4 see Section 4.3.2.20 S12CPMU_UHV_V8 IRC1M Trim Registers (CPMUIRCTRIMH / CPMUIRCTRIML)

1.11.6 ADC External Trigger Input Connection

The ADC module includes external trigger inputs ETRIG0, ETRIG1, ETRIG2, and ETRIG3. The external trigger allows the user to synchronize ADC conversion to external trigger events. On MC9S12VR64/48 ETRIG0 is connected to PP0 / PWM0 and ETRIG1 is connected to PP1 / PWM1. ETRIG2 and ETRIG3 are not used. ETRIG0 can be routed to PS2 and ETRIG1 can be routed to PS3. On MC9S12VR32/16 ETRIG0 is connected to PS2 and ETRIG1 is connected to PS3.

1.11.7 ADC Special Conversion Channels

Whenever the ADC's Special Channel Conversion Bit (SC) in 8.3.2.6 ATD Control Register 5 (ATDCTL5) is set, it is capable of running conversion on a number of internal channels. Table 1-14 lists the internal sources which are connected to these special conversion channels.

2.3.15 Port T Polarity Select Register (PPST)

Address 0x0245 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PPST3	PPST2	PPST1	PPST0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-13. Port T Polarity Select Register (PPST)

[1] Read: Anytime
Write: Anytime

Table 2-14. PPST Register Field Descriptions

Field	Description
3-0 PPST	**Pull device Polarity Select register port T** — Configure pull device polarity on input pin This bit selects a pullup or a pulldown device if enabled on the associated port input pin. 1 A pulldown device is selected 0 A pullup device is selected

2.3.16 Module Routing Register 0 (MODRR0)

Address 0x0246 (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	MODRR07	MODRR06	MODRR05	MODRR04	MODRR03	MODRR02	MODRR01	MODRR00
W								
Routing Option	HS1		HS0		LS1		LS0	
Reset	0	0	0	0	0	0	0	0

Figure 2-14. Module Routing Register 0 (MODRR0 - S12VR64/48)

[1] Read: Anytime
Write: Once in normal, anytime in special mode

Address 0x0246 (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	MODRR05	MODRR04	MODRR03	MODRR02	MODRR01	MODRR00
W								
Routing Option	—		HS0		LS1		LS0	
Reset	0	0	0	0	0	0	0	0

Figure 2-15. Module Routing Register 0 (MODRR0 - S12VR32/16)

[1] Read: Anytime
Write: Once in normal, anytime in special mode

Table 2-15. Module Routing Register 0 Field Descriptions

Field	Description
7-6 MODRR0	**MODule Routing Register 0** — HS1 This register controls the routing of PWM and TIM channels to pin HS1 of HSDRV module. By default the pin is controlled by the related HSDRV port register bit. 11 PWM channel 1 routed to HS1 if enabled 10 PWM channel 4 routed to HS1 if enabled 01 TIM output compare channel 3 routed to HS1 if enabled 00 HS1 controlled by register bit HSDR[HSDR1]. Refer to HSDRV section.
5-4 MODRR0	**MODule Routing Register 0** — HS0 This register controls the routing of PWM and TIM channels to pin HS0 of HSDRV module. By default the pin is controlled by the related HSDRV port register bit. 11 PWM channel 3 routed to HS0 if enabled 10 PWM channel 3 routed to HS0 if enabled 01 TIM output compare channel 2 routed to HS0 if enabled 00 HS0 controlled by register bit HSDR[HSDR0]. Refer to HSDRV section.
3-2 MODRR0	**MODule Routing Register 0** — LS1 This register controls the routing of PWM and TIM channels to pin LS1 of LSDRV module. By default the pin is controlled by the related LSDRV port register bit. 11 PWM channel 7 routed to LS1 if enabled 10 PWM channel 7 routed to LS1 if enabled 01 TIM output compare channel 1 routed to LS1 if enabled 00 LS1 controlled by register bit LSDR[LSDR1]. Refer to LSDRV section.
1-0 MODRR0	**MODule Routing Register 0** — LS0 This register controls the routing of PWM and TIM channels to pin LS0 of LSDRV module. By default the pin is controlled by the related LSDRV port register bit. 11 PWM channel 5 routed to LS0 if enabled 10 PWM channel 6 routed to LS0 if enabled 01 TIM output compare channel 0 routed to LS0 if enabled 00 LS0 controlled by register bit LSDR[LSDR0]. Refer to LSDRV section.

Table 2-28. RDRP Register Field Descriptions

Field	Description
2 RDRP	**Reduced Drive Register port P** — Select reduced drive for output pin This bit configures the drive strength of the associated output pin as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/10 of the full drive strength) 0 Full drive strength enabled
1-0 RDRP	**Reduced Drive Register port P** — Select reduced drive for output pin This bit configures the drive strength of the associated output pin as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/5 of the full drive strength) 0 Full drive strength enabled

2.3.30 Port P Pull Device Enable Register (PERP)

Address 0x025C (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-41. Port P Pull Device Enable Register (PERP - S12VR64/48)

[1] Read: Anytime
Write: Anytime

Address 0x025C (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PERP2	PERP1	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-42. Port P Pull Device Enable Register (PERP - S12VR32/16)

[1] Read: Anytime
Write: Anytime

Table 2-29. PERP Register Field Descriptions

Field	Description
5-0 PERP	**Pull device Enable Register port P** — Enable pull device on input pin This bit controls whether a pull device on the associated port input pin is active. If a pin is used as output this bit has no effect. The polarity is selected by the related polarity select register bit. 1 Pull device enabled 0 Pull device disabled

2.3.33 Port P Interrupt Flag Register (PIFP)

Address 0x025F (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	OCIF	0	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-47. Port P Interrupt Flag Register (PIFP - S12VR64/48)

[1] Read: Anytime
Write: Anytime, write 1 to clear

Address 0x025F (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	OCIF	0	0	0	0	PIFP2	PIFP1	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-48. Port P Interrupt Flag Register (PIFP - S12VR32/16)

[1] Read: Anytime
Write: Anytime, write 1 to clear

Table 2-32. PIFP Register Field Descriptions

Field	Description
7 OCIF	**Over-Current Interrupt Flag** register port P — This flag asserts if an over-current condition is detected on PP2 (Section 2.4.4.3, “Over-Current Interrupt and Protection”). 1 PP2 Over-current event occurred 0 No PP2 over-current event occurred
5-0 PIFP	**Pin Interrupt Flag** register port P — This flag asserts after a valid active edge was detected on the related pin (Section 2.4.4, “Interrupts”). This can be a rising or a falling edge based on the state of the polarity select register. An interrupt will occur if the associated interrupt enable bit is set. 1 Active edge on the associated bit has occurred 0 No active edge occurred

4.3.2.16 Autonomous Clock Trimming Register (CPMUACLKTR)

The CPMUACLKTR register configures the trimming of the Autonomous Clock (ACLK - trimmable internal RC-Oscillator) which can be selected as clock source for some CPMU features.

0x02F3

	7	6	5	4	3	2	1	0
R	ACLKTR5	ACLKTR4	ACLKTR3	ACLKTR2	ACLKTR1	ACLKTR0	0	0
W								
Reset	F	F	F	F	F	F	0	0

After de-assert of System Reset a value is automatically loaded from the Flash memory.

Figure 4-21. Autonomous Clock Trimming Register (CPMUACLKTR)

Read: Anytime

Write: Anytime

Table 4-19. CPMUACLKTR Field Descriptions

Field	Description
7–2 ACLKTR[5:0]	**Autonomous Clock Period Trimming Bits** — See Table 4-20 for trimming effects. The ACLKTR[5:0] value represents a signed number influencing the ACLK period time.

Table 4-20. Trimming Effect of ACLKTR[5:0]

ACLKTR[5:0]	Decimal	ACLK frequency
100000	-32	lowest
100001	-31	increasing
....		
111111	-1	
000000	0	mid
000001	+1	increasing
....		
011110	+30	
011111	+31	highest

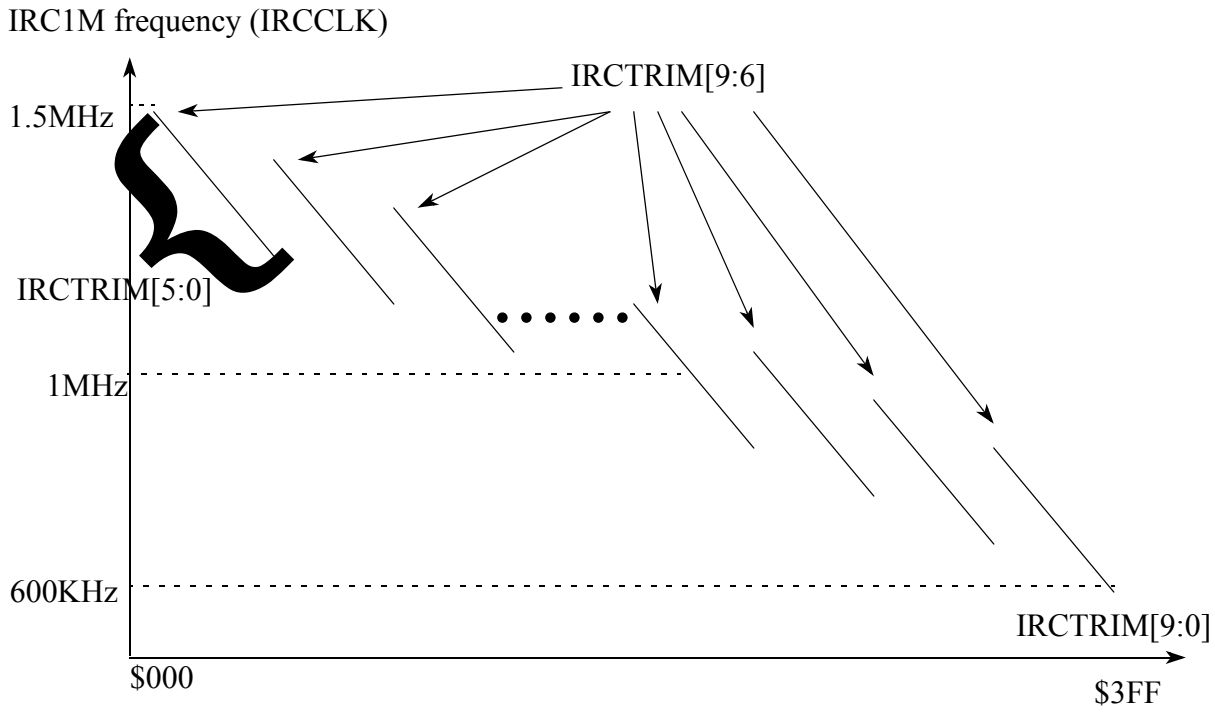
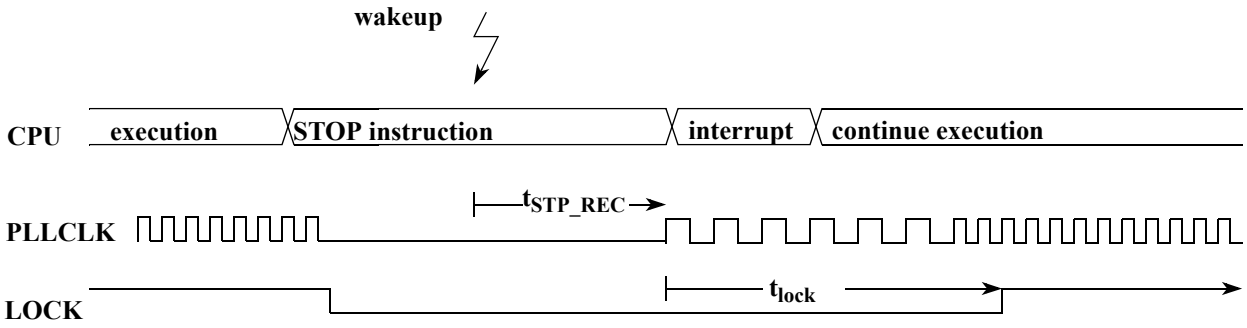


Figure 4-28. IRC1M Frequency Trimming Diagram

4.4.3 Stop Mode using PLLCLK as source of the Bus Clock

An example of what happens going into Stop Mode and exiting Stop Mode after an interrupt is shown in Figure 4-36. Disable PLL Lock interrupt (LOCKIE=0) before going into Stop Mode.

Figure 4-36. Stop Mode using PLLCLK as source of the Bus Clock



Depending on the COP configuration there might be an additional significant latency time until COP is active again after exit from Stop Mode due to clock domain crossing synchronization. This latency time occurs if COP clock source is ACLK and the CSAD bit is set (please refer to CSAD bit description for details).

4.4.4 Full Stop Mode using Oscillator Clock as source of the Bus Clock

An example of what happens going into Full Stop Mode and exiting Full Stop Mode after an interrupt is shown in Figure 4-37.

Disable PLL Lock interrupt (LOCKIE=0) and oscillator status change interrupt (OSCIE=0) before going into Full Stop Mode.

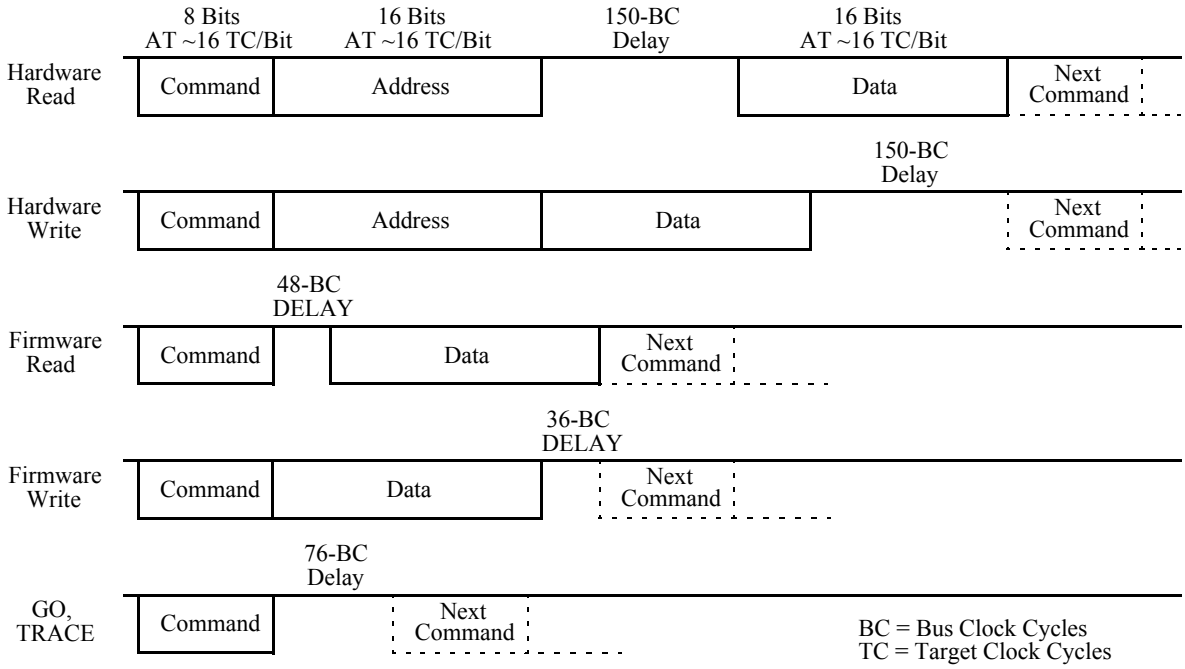


Figure 5-6. BDM Command Structure

5.4.6 BDM Serial Interface

The BDM communicates with external devices serially via the BKGD pin. During reset, this pin is a mode select input which selects between normal and special modes of operation. After reset, this pin becomes the dedicated serial interface pin for the BDM.

The BDM serial interface is timed based on the VCO clock (please refer to the CPMU Block Guide for more details), which gets divided by 8. This clock will be referred to as the target clock in the following explanation.

The BDM serial interface uses a clocking scheme in which the external host generates a falling edge on the BKGD pin to indicate the start of each bit time. This falling edge is sent for every bit whether data is transmitted or received. Data is transferred most significant bit (MSB) first at 16 target clock cycles per bit. The interface times out if 512 clock cycles occur between falling edges from the host.

The BKGD pin is a pseudo open-drain pin and has an weak on-chip active pull-up that is enabled at all times. It is assumed that there is an external pull-up and that drivers connected to BKGD do not typically drive the high level. Since R-C rise time could be unacceptably long, the target system and host provide brief driven-high (speedup) pulses to drive BKGD to a logic 1. The source of this speedup pulse is the host for transmit cases and the target for receive cases.

The timing for host-to-target is shown in Figure 5-7 and that of target-to-host in Figure 5-8 and Figure 5-9. All four cases begin when the host drives the BKGD pin low to generate a falling edge. Since the host and target are operating from separate clocks, it can take the target system up to one full clock cycle to recognize this edge. The target measures delays from this perceived start of the bit time while the host measures delays from the point it actually drove BKGD low to start the bit up to one target clock cycle

10.4.6 Receiver

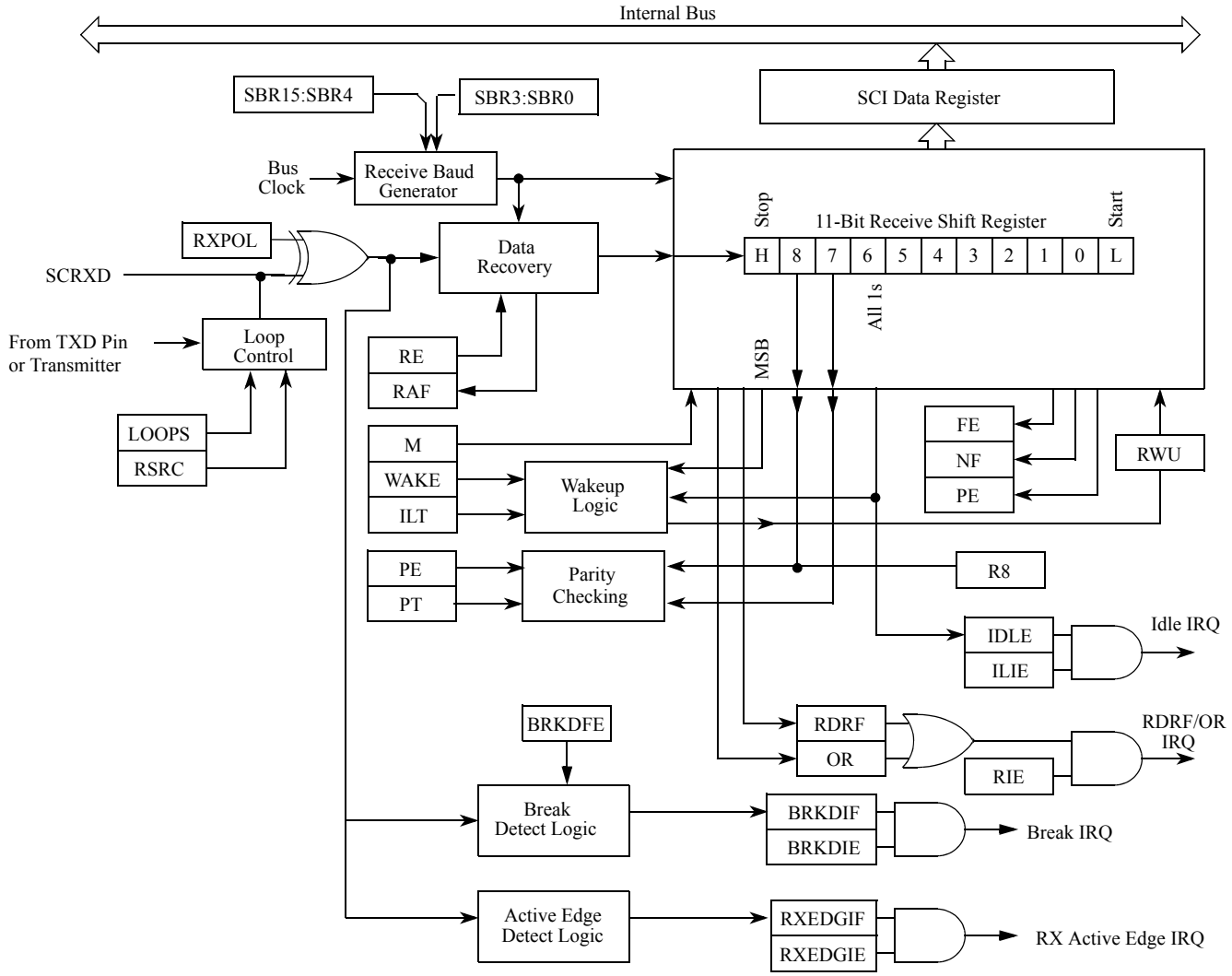


Figure 10-20. SCI Receiver Block Diagram

10.4.6.1 Receiver Character Length

The SCI receiver can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When receiving 9-bit data, bit R8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

10.4.6.2 Character Reception

During an SCI reception, the receive shift register shifts a frame in from the RXD pin. The SCI data register is the read-only buffer between the internal data bus and the receive shift register.

After a complete frame shifts into the receive shift register, the data portion of the frame transfers to the SCI data register. The receive data register full flag, RDRF, in SCI status register 1 (SCISR1) becomes set,

In Figure 10-24, a large burst of noise is perceived as the beginning of a start bit, although the test sample at RT5 is high. The RT5 sample sets the noise flag. Although this is a worst-case misalignment of perceived bit time, the data samples RT8, RT9, and RT10 are within the bit time and data recovery is successful.

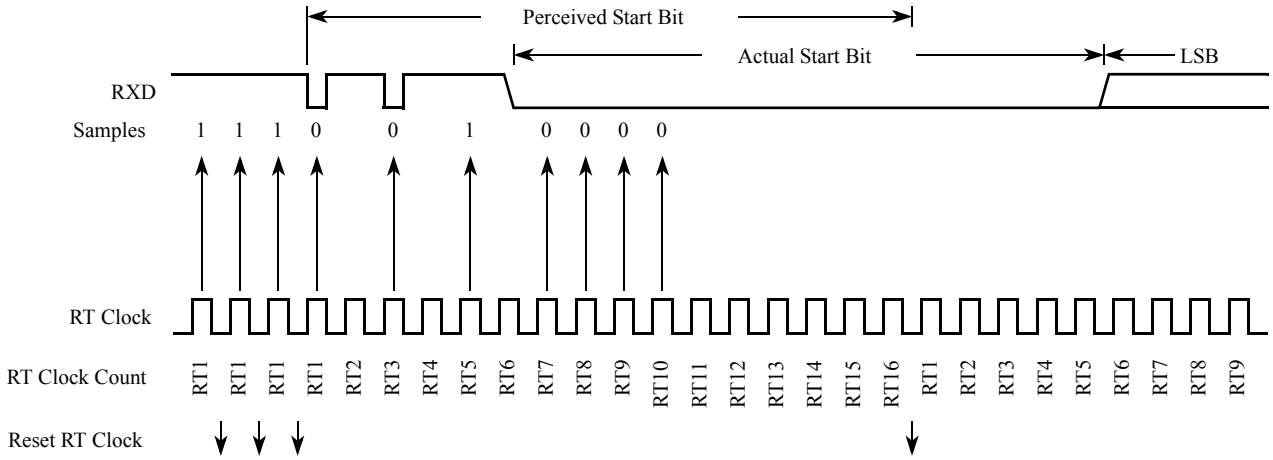


Figure 10-24. Start Bit Search Example 3

Figure 10-25 shows the effect of noise early in the start bit time. Although this noise does not affect proper synchronization with the start bit time, it does set the noise flag.

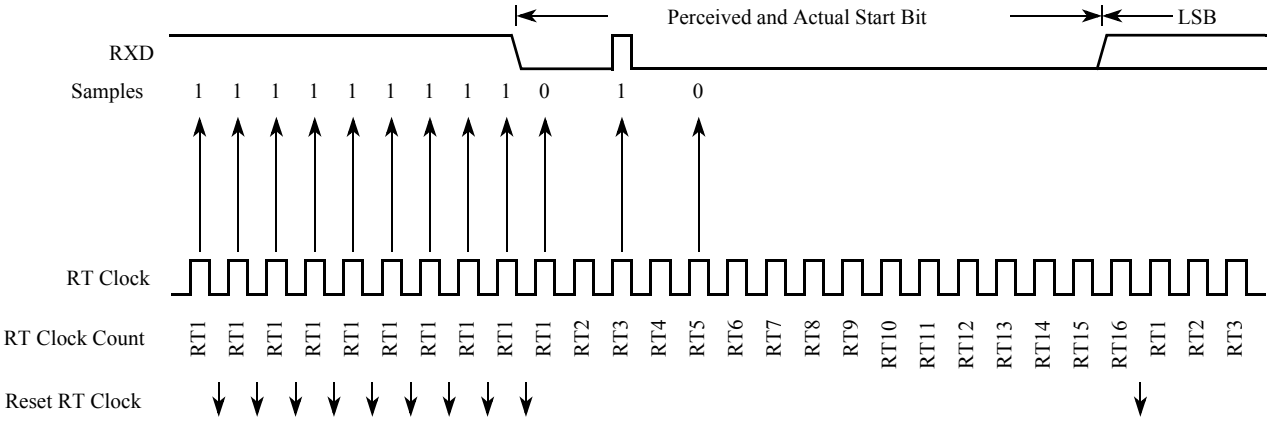


Figure 10-25. Start Bit Search Example 4

Table 11-7. Example SPI Baud Rate Selection (25 MHz Bus Clock) (Sheet 2 of 3)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
0	0	1	0	1	0	16	1.5625 Mbit/s
0	0	1	0	1	1	32	781.25 kbit/s
0	0	1	1	0	0	64	390.63 kbit/s
0	0	1	1	0	1	128	195.31 kbit/s
0	0	1	1	1	0	256	97.66 kbit/s
0	0	1	1	1	1	512	48.83 kbit/s
0	1	0	0	0	0	6	4.16667 Mbit/s
0	1	0	0	0	1	12	2.08333 Mbit/s
0	1	0	0	1	0	24	1.04167 Mbit/s
0	1	0	0	1	1	48	520.83 kbit/s
0	1	0	1	0	0	96	260.42 kbit/s
0	1	0	1	0	1	192	130.21 kbit/s
0	1	0	1	1	0	384	65.10 kbit/s
0	1	0	1	1	1	768	32.55 kbit/s
0	1	1	0	0	0	8	3.125 Mbit/s
0	1	1	0	0	1	16	1.5625 Mbit/s
0	1	1	0	1	0	32	781.25 kbit/s
0	1	1	0	1	1	64	390.63 kbit/s
0	1	1	1	0	0	128	195.31 kbit/s
0	1	1	1	0	1	256	97.66 kbit/s
0	1	1	1	1	0	512	48.83 kbit/s
0	1	1	1	1	1	1024	24.41 kbit/s
1	0	0	0	0	0	10	2.5 Mbit/s
1	0	0	0	0	1	20	1.25 Mbit/s
1	0	0	0	1	0	40	625 kbit/s
1	0	0	0	1	1	80	312.5 kbit/s
1	0	0	1	0	0	160	156.25 kbit/s
1	0	0	1	0	1	320	78.13 kbit/s
1	0	0	1	1	0	640	39.06 kbit/s
1	0	0	1	1	1	1280	19.53 kbit/s
1	0	1	0	0	0	12	2.08333 Mbit/s
1	0	1	0	0	1	24	1.04167 Mbit/s
1	0	1	0	1	0	48	520.83 kbit/s
1	0	1	0	1	1	96	260.42 kbit/s
1	0	1	1	0	0	192	130.21 kbit/s
1	0	1	1	0	1	384	65.10 kbit/s
1	0	1	1	1	0	768	32.55 kbit/s
1	0	1	1	1	1	1536	16.28 kbit/s
1	1	0	0	0	0	14	1.78571 Mbit/s
1	1	0	0	0	1	28	892.86 kbit/s
1	1	0	0	1	0	56	446.43 kbit/s
1	1	0	0	1	1	112	223.21 kbit/s

Table 17-5. BATIF Register Field Descriptions

Field	Description
1 BVHIF	**BATS Interrupt Flag High Detect** — The flag is set to 1 when BVHC status bit changes. 0 No change of the BVHC status bit since the last clearing of the flag. 1 BVHC status bit has changed since the last clearing of the flag.
0 BVLIF	**BATS Interrupt Flag Low Detect** — The flag is set to 1 when BVLC status bit changes. 0 No change of the BVLC status bit since the last clearing of the flag. 1 BVLC status bit has changed since the last clearing of the flag.

17.3.2.5 Reserved Register

Module Base + 0x0006
Module Base + 0x0007

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 17-8. Reserved Register

[1] Read: Anytime
Write: Only in special mode

NOTE

These reserved registers are designed for factory test purposes only and are not intended for general user access. Writing to these registers when in special mode can alter the module's functionality.

17.4 Functional Description

17.4.1 General

The BATS module allows measuring voltages on the VSENSE and VSUP pins. The VSENSE pin is implemented to allow measurement of the supply Line (Battery) Voltage V_{BAT} directly. By bypassing the device supply capacitor and the external reversed battery protection diode this pin allows to detect under/over voltage conditions without delay. A series resistor (R_{VSENSE_R}) is required to protect the VSENSE pin from fast transients.

The voltage at the VSENSE or VSUP pin can be routed via an internal voltage divider to an internal Analog to Digital Converter Channel. Also the BATS module can be configured to generate a low and high voltage interrupt based on VSENSE or VSUP. The trigger level of the high and low interrupt are selectable.

In a typical application, the module could be used as follows: The voltage at VSENSE is observed via usage of the interrupt feature (BSESE=1, BVHIE=1), while the VSUP pin voltage is routed to the ADC to allow regular measurement (BSUAE=1).

Table 18-49. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 18-27)
		Set if an invalid global address [17:16] is supplied see)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

18.4.6.10 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and EEPROM memory space and, if the erase is successful, will release security.

Table 18-50. Unsecure Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and EEPROM memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security state. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag is set after the Unsecure Flash operation has completed.

Table 18-51. Unsecure Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 18-27)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

18.4.6.11 Verify Backdoor Access Key Command

The Verify Backdoor Access Key command will only execute if it is enabled by the KEYEN bits in the FSEC register (see Table 18-10). The Verify Backdoor Access Key command releases security if user-supplied keys match those stored in the Flash security bytes of the Flash configuration field (see Table 18-4). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

NVM Command Mode — An NVM mode using the CPU to setup the FCCOB register to pass parameters required for Flash command execution.

Phrase — An aligned group of four 16-bit words within the P-Flash memory. Each phrase includes two sets of aligned double words with each set including 7 ECC bits for single bit fault correction and double bit fault detection within each double word.

P-Flash Memory — The P-Flash memory constitutes the main nonvolatile memory store for applications.

P-Flash Sector — The P-Flash sector is the smallest portion of the P-Flash memory that can be erased. Each P-Flash sector contains 512 bytes.

Program IFR — Nonvolatile information register located in the P-Flash block that contains the Version ID, and the Program Once field.

19.1.2 Features

19.1.2.1 P-Flash Features

- 32 Kbytes of P-Flash memory composed of one 32 Kbyte Flash block divided into 64 sectors of 512 bytes
- Single bit fault correction and double bit fault detection within a 32-bit double word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and phrase program operation
- Ability to read the P-Flash memory while programming a word in the EEPROM memory
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

19.1.2.2 EEPROM Features

- 128 bytes of EEPROM memory composed of one 128 byte Flash block divided into 32 sectors of 4 bytes
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Protection scheme to prevent accidental program or erase of EEPROM memory
- Ability to program up to four words in a burst sequence

19.1.2.3 Other Flash Module Features

- No external high-voltage power supply required for Flash memory program and erase operations
- Interrupt generation on Flash command completion and Flash error detection
- Security mechanism to prevent unauthorized access to the Flash memory

Table 19-49. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 19-27)
		Set if an invalid global address [17:16] is supplied see Table 19-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

19.4.6.10 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and EEPROM memory space and, if the erase is successful, will release security.

Table 19-50. Unsecure Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and EEPROM memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security state. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag is set after the Unsecure Flash operation has completed.

Table 19-51. Unsecure Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 19-27)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

19.4.6.11 Verify Backdoor Access Key Command

The Verify Backdoor Access Key command will only execute if it is enabled by the KEYEN bits in the FSEC register (see Table 19-10). The Verify Backdoor Access Key command releases security if user-supplied keys match those stored in the Flash security bytes of the Flash configuration field (see Table 19-4). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

A.1.8 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.8.1 Measurement Conditions

Current is measured on VSUP & VSUPHS pins. VDDX is connected to VDDA. It does not include the current to drive external loads. Unless otherwise noted the currents are measured in special single chip mode and the CPU code is executed from RAM. For Run and Wait current measurements PLL is on and the reference clock is the IRC1M trimmed to 1MHz. The bus frequency is 25MHz and the CPU frequency is 50MHz. Table A-9, Table A-10 and Table A-11 show the configuration of the CPMU module and the peripherals for Run, Wait and Stop current measurement.

Table A-9. CPMU Configuration for Pseudo Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUCLKS	PLLSEL=0, PSTP=1, CSAD=0 PRE=PCE=RTIOSCSEL=COPOSCSEL=1
CPMUOSC	OSCE=1, External Square wave on EXTAL f_{EXTAL}=4MHz, V_{IH}= 1.8V, V_{IL}=0V
CPMURTI	RTDEC=0, RTR[6:4]=111, RTR[3:0]=1111;
CPMUCOP	WCOP=1, CR[2:0]=111

Table A-10. CPMU Configuration for Run/Wait and Full Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUSYNR	VCOFRQ[1:0]=01,SYNDIV[5:0] = 24
CPMUPOSTDIV	POSTDIV[4:0]=0
CPMUCLKS	PLLSEL=1
CPMUOSC	OSCE=0, Reference clock for PLL is f_{ref}=f_{irc1m} trimmed to 1MHz
API settings for STOP current measurement	
CPMUAPICTL	APIEA=0, APIFE=1, APIE=0
CPMUAPITR	trimmed to >=10Khz
CPMUAPIRH/RL	set to $FFFF

Appendix M
FTMRG Electrical Specifications

M.1 Timing Parameters

The time base for all NVM program or erase operations is derived from the bus clock using the FCLKDIV register. The frequency of this derived clock must be set within the limits specified as f_{NVMOP}. The NVM module does not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. When attempting to program or erase the NVM module at a lower frequency, a full program or erase transition is not assured.

All timing parameters are a function of the bus clock frequency, f_{NVMBUS}. All program and erase times are also a function of the NVM operating frequency, f_{NVMOP}. A summary of key timing parameters can be found in **Table M-1.** and **Table M-2.**

Table M-1. Operating frequency

	Symbol	Min	Typ	Max	Unit
Bus Frequency	f_{NVMBUS}	1	25	25	MHz
Operating Frequency	f_{NVMOP}	0,8	1	1.05	MHz

Table M-2. NVM Timing Characteristics for S12FTMRG64K512

#	Command	f_{NVMOP} cycle	f_{NVMBUS} cycle	Symbol	Min[1]	Typ[2]	Max[3]	Lfmax[4]	Unit
1	Erase Verify All Blocks	0	17169	t_{RD1ALL}	0.69	0.69	1.37	34.34	ms
2	Erase Verify Block (Pflash)	0	16924	t_{RD1BLK_P}	0.68	0.68	1.35	33.85	ms
3	Erase Verify Block (EEPROM)	0	744	t_{RD1BLK_D}	0.03	0.03	0.06	1.49	ms
4	Erase Verify P-Flash Section	0	476	t_{RD1SEC}	19.04	19.04	38.08	952.00	us
5	Read Once	0	445	t_{RDONCE}	17.80	17.80	17.80	445.00	us
6	Program P-Flash (4 Word)	164	2896	t_{PGM_4}	0.27	0.28	0.63	11.79	ms
7	Program Once	164	2859	$t_{PGMONCE}$	0.27	0.28	0.28	3.06	ms
8	Erase All Blocks	100066	17505	t_{ERSALL}	96.00	100.77	101.47	160.09	ms
9	Erase Flash Block (Pflash)	100060	17150	t_{ERSBLK_P}	95.98	100.75	101.43	159.38	ms
10	Erase Flash Block (EEPROM)	100060	1033	t_{ERSBLK_D}	95.34	100.10	100.14	127.14	ms

P.13 0x0070-0x009F Analog to Digital Converter 10-Bit 6-Channel (ATD) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x008A	ATDDR5H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x008B	ATDDR5L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x008C-0 x009F	Reserved	R	0	0	0	0	0	0	0	0
		W								

P.14 0x00A0-0x00C7 Pulse Width Modulator 6-Channels (PWM) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00A0	PWME	R	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		W								
0x00A1	PWMPOL	R	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		W								
0x00A2	PWMCLK	R	PCLK7	PCLK6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		W								
0x00A3	PWMPRCLK	R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		W								
0x00A4	PWMCAE	R	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		W								
0x00A5	PWMCTL	R	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		W								
0x00A6	PWMCLKAB	R	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
		W								
0x00A7	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00A8	PWMSCLA	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00A9	PWMSCLB	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00AA	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00AB	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00AC	PWMCNT0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00AD	PWMCNT1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00AE	PWMCNT2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00AF	PWMCNT3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: MC9S12ZVRRM
Rev. 4.2
08 Feb 2016