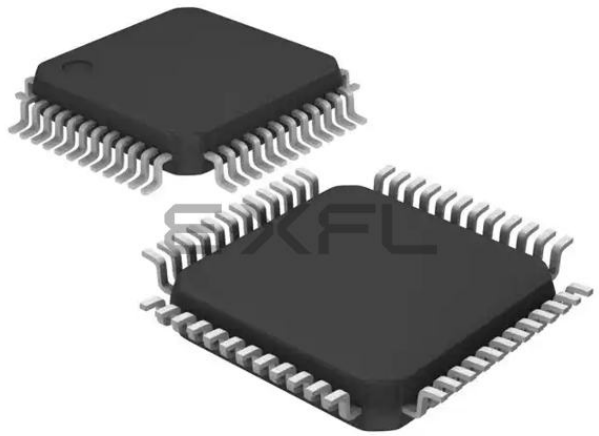

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Core Processor	12V1
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Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vr64af0vlf

Chapter 2
Port Integration Module (S12VRPIMV3)

Global Address	Register Name[1]		Bit 7	6	5	4	3	2	1	Bit 0
0x025A	DDRP	R	0	0	**DDRP5**	**DDRP4**	**DDRP3**	DDRP2	DDRP1	**DDRP0**
		W								
0x025B	RDRP	R	0	0	0	0	0	RDRP2	RDRP1	**RDRP0**
		W								
0x025C	PERP	R	0	0	**PERP5**	**PERP4**	**PERP3**	PERP2	PERP1	**PERP0**
		W								
0x025D	PPSP	R	0	0	**PPSP5**	**PPSP4**	**PPSP3**	PPSP2	PPSP1	**PPSP0**
		W								
0x025E	PIEP	R	OCIE	0	**PIEP5**	**PIEP4**	**PIEP3**	PIEP2	PIEP1	**PIEP0**
		W								
0x025F	PIFP	R	OCIF	0	**PIFP5**	**PIFP4**	**PIFP3**	PIFP2	PIFP1	**PIFP0**
		W								
0x0260–0x0268	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0269	PTIL	R	0	0	0	0	PTIL3	PTIL2	PTIL1	PTIL0
		W								
0x026A	DIENL	R	0	0	0	0	DIENL3	DIENL2	DIENL1	DIENL0
		W								
0x026B	PTAL	R	PTTEL	PTPSL	PTABYPL	PTADIRL	PTAENL	0	PTAL1	PTAL0
		W								
0x026C	PIRL	R	0	0	0	0	PIRL3	PIRL2	PIRL1	PIRL0
		W								
0x026D	PPSL	R	0	0	0	0	PPSL3	PPSL2	PPSL1	PPSL0
		W								
0x026E	PIEL	R	0	0	0	0	PIEL3	PIEL2	PIEL1	PIEL0
		W								
0x026F	PIFL	R	0	0	0	0	PIFL3	PIFL2	PIFL1	PIFL0
		W								
0x0270	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0271	PT1AD	R	0	0	**PT1AD5**	**PT1AD4**	**PT1AD3**	**PT1AD2**	PT1AD1	PT1AD0
		W								

The configuration bit PPS is used for two purposes:

1. Configure the sensitive interrupt edge (rising or falling), if interrupt is enabled.
2. Select either a pullup or pulldown device if PER is active.

Table 2-3. Pin Configuration Summary[1]

DDR	PORT PT	PER	PPS[1]	PIE[2]	Function	Pull Device	Interrupt
0	x	0	x	0	Input	Disabled	Disabled
0	x	1	0	0	Input	Pullup	Disabled
0	x	1	1	0	Input	Pulldown	Disabled
0	x	0	0	1	Input	Disabled	Falling edge
0	x	0	1	1	Input	Disabled	Rising edge
0	x	1	0	1	Input	Pullup	Falling edge
0	x	1	1	1	Input	Pulldown	Rising edge
1	0	x	x	0	Output, drive to 0	Disabled	Disabled
1	1	x	x	0	Output, drive to 1	Disabled	Disabled
1	0	x	0	1	Output, drive to 0	Disabled	Falling edge
1	1	x	1	1	Output, drive to 1	Disabled	Rising edge

1 Always “0” on Port E

2 Applicable only on Port P and AD

NOTE

- All register bits in this module are completely synchronous to internal clocks during a register read.
- Figure of port data registers also display the alternative functions if applicable on the related pin as defined in Table 2-2. Names in parentheses denote the availability of the function when using a specific routing option.
- Figures of module routing registers also display the module instance or module channel associated with the related routing bit.

1. Not applicable for Port L. Refer to register descriptions.

[1] Read: Anytime
Write: Anytime

Table 2-12. DDRT Register Field Descriptions

Field	Description
3 DDRT	**Data Direction Register port T —** This bit determines whether the pin is an input or output Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. The enabled routed LINPHY forces the I/O state to be an input (LPTXD). Else the TIM forces the I/O state to be an output for a TIM port associated with an enabled TIM output compare. In these cases the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
2 DDRT	**Data Direction Register port T —** This bit determines whether the pin is an input or output. Depending on the configuration of the enabled SPI the I/O state will be forced to be input or output. The enabled routed LINPHY forces the I/O state to be an output (LPRXD). Else the TIM forces the I/O state to be an output for a TIM port associated with an enabled TIM output compare. In these cases the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input
1-0 DDRT	**Data Direction Register port T —** This bit determines whether the pin is an input or output. Depending on the configuration of the enabled routed SCI0 the I/O state will be forced to be input or output. The enabled routed LINPHY forces the I/O state to be an output (LPDR[LPDR1]). Else the TIM forces the I/O state to be an output for a TIM port associated with an enabled TIM output compare. In these cases the data direction bit will not change. 1 Associated pin is configured as output 0 Associated pin is configured as input

2.3.14 Port T Pull Device Enable Register (PERT)

Address 0x0244 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PERT3	PERT2	PERT1	PERT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-12. Port T Pull Device Enable Register (PERT)

[1] Read: Anytime
Write: Anytime

Table 2-13. PERT Register Field Descriptions

Field	Description
3-0 PERT	**Pull device Enable Register port T** — Enable pull device on input pin This bit controls whether a pull device on the associated port input pin is active. If a pin is used as output this bit has no effect. The polarity is selected by the related polarity select register bit. 1 Pull device enabled 0 Pull device disabled

Table 2-25. PTP Register Field Descriptions (continued)

Field	Description
1 PTP	**PorT data register port P** — General-purpose input/output data, PWM output, pin interrupt input/output, $\overline{\text{XIRQ}}$ input The $\overline{\text{XIRQ}}$ signal is mapped to this pin when used with the XIRQ interrupt function. The interrupt is enabled by clearing the X mask bit in the CPU Condition Code register. The I/O state of the pin is forced to input level upon the first clearing of the X bit and held in this state even if the bit is set again. A stop or wait recovery with the X bit set (refer to CPU12/CPU12X Reference Manual) is not available. When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read. • The XIRQ function takes precedence over the PWM and the general-purpose I/O function if enabled. • The PWM function takes precedence over the general-purpose I/O function if the related channel is enabled. • Pin interrupts can be generated if enabled in input or output mode.
0 PTP	**PorT data register port P** — General-purpose input/output data, PWM output, pin interrupt input/output When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read. • The PWM function takes precedence over the general-purpose I/O function if the related channel is enabled. • Pin interrupts can be generated if enabled in input or output mode.

2.3.27 Port P Input Register (PTIP)

Address 0x0259 (S12VR64/48) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-35. Port P Input Register (PTIP - S12VR64/48)

[1] Read: Anytime
Write:Never

Address 0x0259 (S12VR32/16) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PTIP2	PTIP1	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-36. Port P Input Register (PTIP - S12VR32/16)

[1] Read: Anytime
Write:Never

voltage divider can be bypassed (PTAL[PTADIRL]=1). Additionally in latter case the impedance converter in the ADC signal path can be configured to be used or bypassed in direct input mode (PTAL[PTABYPL]).

Out of reset the digital input buffer of the selected pin is disabled to avoid shoot-through current. Pin interrupts can only be generated if DIENL[x]=1.

In stop mode the digital input buffer is enabled if DIENL[x]=1 or if the PTAL[PTTEL] bit is set to support wakeup functionality.

Table 2-49 shows the HVI input configuration depending on register bits and operation mode.

Table 2-49. HVI Input Configurations

Mode	DIENL	PTAENL	Digital Input	Analog Input	Resulting Function
Run/Wait	0	0	off	off	Input disabled (Reset)
	0	1	off[1]	enabled	Analog input, interrupt not supported
	1	0	enabled	off	Digital input, interrupt supported
	1	1	off[1]	enabled	Analog input, interrupt not supported
Stop	0	X	off	off	If PTAL[PTTEL] is set: input enabled, wakeup from stop supported. If PTAL[PTTEL] is cleared: input disabled, wakeup from stop not supported.
	1	X	enabled	off	Digital input, wakeup from stop supported

[1] Enabled if (PTAL[PTTEL]=1 & PTAL[PTADIRL]=0)

NOTE

An external resistor R_{EXT_HVI} must always be connected to the high-voltage inputs to protect the device pins from fast transients and to achieve the specified pin input divider ratios when using the HVI in analog mode.

2.4.3.7 Port AD

This port is associated with the ADC.

Port AD pins can be used for either general-purpose I/O, or with the ADC subsystem.

2.4.4 Interrupts

This section describes the interrupts generated by the PIM and their individual sources. Vector addresses and interrupt priorities are defined at MCU level.

Table 2-50. PIM Interrupt Sources

Module Interrupt Sources	Local Enable (S12VR64/48)	Local Enable (S12VR32/16)
$\overline{\text{XIRQ}}$	None	None

VDDX has to be connected externally to VDDA.

4.2.6 VSS— Ground Pin

VSS is the ground pin for the core logic. On the board VSSX, VSSA and VSS need to be connected together to the application ground.

4.2.7 API_EXTCLK — API external clock output pin

This pin provides the signal selected via APIES and is enabled with APIEA bit. See the device specification if this clock output is available on this device and to which pin it might be connects.

4.2.8 VDD— Internal Regulator Output Supply (Core Logic)

Node VDD is a device internal supply output of the voltage regulator that provides the power supply for the core logic.

This supply domain is monitored by the Low Voltage Reset circuit.

4.2.9 VDDF— Internal Regulator Output Supply (NVM Logic)

Node VDDF is a device internal supply output of the voltage regulator that provides the power supply for the NVM logic.

This supply domain is monitored by the Low Voltage Reset circuit.

4.2.10 TEMPSENSE — Internal Temperature Sensor Output Voltage

Depending on the VSEL setting either the voltage level generated by the temperature sensor or the VREG bandgap voltage is driven to a special channel input of the ADC Converter. See device level specification for connectivity of ADC special channels.

4.3.2.12 S12CPMU_UHV_V8 COP Timer Arm/Reset Register (CPMUARMCOP)

This register is used to restart the COP time-out period.

0x003F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	ARMCOP-Bit 7	ARMCOP-Bit 6	ARMCOP-Bit 5	ARMCOP-Bit 4	ARMCOP-Bit 3	ARMCOP-Bit 2	ARMCOP-Bit 1	ARMCOP-Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 4-15. S12CPMU_UHV_V8 CPMUARMCOP Register

Read: Always reads $00

Write: Anytime

When the COP is disabled (CR[2:0] = “000”) writing to this register has no effect.

When the COP is enabled by setting CR[2:0] nonzero, the following applies:

Writing any value other than $55 or $AA causes a COP reset. To restart the COP time-out period write $55 followed by a write of $AA. These writes do not need to occur back-to-back, but the sequence ($55, $AA) must be completed prior to COP end of time-out period to avoid a COP reset. Sequences of $55 writes are allowed. When the WCOP bit is set, $55 and $AA writes must be done in the last 25% of the selected time-out period; writing any value in the first 75% of the selected period will cause a COP reset.

4.3.2.13 High Temperature Control Register (CPMUHTCTL)

The CPMUHTCTL register configures the temperature sense features.

0x02F0

	7	6	5	4	3	2	1	0
R	0	0	VSEL	0	HTE	HTDS	HTIE	HTIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 4-16. High Temperature Control Register (CPMUHTCTL)

Read: Anytime

Write: VSEL, HTE, HTIE and HTIF are write anytime, HTDS is read only

intended for general user access. Writing to this register when in special mode can alter the module's functionality.

Table 14-7. Reserved Register Field Descriptions

Field	Description
7-0 Reserved	These reserved bits are used for test purposes. Writing to these bits can alter the module functionality.

14.3.7 HSDRV1C Status Register (HSSR)

Module Base + 0x0005 Access: User read[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	HSOL0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-6. HSDRV1C Status Register (HSSR)

[1] Read: Anytime
Write: No Write

Table 14-8. HSDRV Status Register (HSSR) Field Descriptions

Field	Description
0 HSOL0	HSDRV1C Open-Load Status Bit This bit reflects the open-load condition on the driver pin. A delay of $t_{HLROLDT}$ must be granted after enabling the high-load resistance open-load detection function in order to read valid data. 0 No open-load condition, $\lvert I_{HS} \rvert \geq \lvert I_{HLROLDC} \rvert$ 1 Open-load condition, $\lvert I_{HS} \rvert < \lvert I_{HLROLDC} \rvert$

15.3.7 LSDRV Interrupt Flag Register (LSIF)

Module Base + 0x0007 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	LSOCIF1	LSOCIF0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 15-6. LSDRV Interrupt Flag Register (LSIF)

[1] Read: Anytime
Write: Write 1 to clear, writing 0 has no effect

Table 15-8. LSIF Register Field Descriptions

Field	Description
1-0 LSOCIFx	**LSDRV Over-Current Interrupt Flag** These flags are set to 1 when an over-current event occurs on the related low-side driver ($I_{LS} > I_{LIMLSX}$). While set the related low-side driver is turned off. Once these flags are cleared, the related driver is again driven by the source selected in PIM module. 0 No over-current event occurred since last clearing of flag 1 An over-current event occurred since last clearing of flag

16.4.4 Interrupts

The interrupt vector requested by the LIN Physical Layer is listed in Table 16-10. Vector address and interrupt priority is defined at the MCU level.

The module internal interrupt sources are combined into a single interrupt request at the device level.

Table 16-10. Interrupt Vectors

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
LIN Interrupt (LPI)	LIN Txd-Dominant Timeout Interrupt (LPDTIF)	LPDTIE = 1
	LIN Overcurrent Interrupt (LPOCIF)	LPOCIE = 1

16.4.4.1 Overcurrent Interrupt

The transmitter is protected against overcurrent. In case of an overcurrent condition occurring within a time frame called t_{OCLIM} starting from LPTxD falling edge, the current through the transmitter is limited (the transmitter is not shut down). The masking of an overcurrent event within the time frame t_{OCLIM} is meant to avoid “false” overcurrent conditions that can happen during the discharging of the LIN bus. If an overcurrent event occurs out of this time frame, the transmitter is disabled and the LPOCIF flag is set.

In order to re-enable the transmitter again, the following prerequisites must be met:

1) Overcurrent condition is over

2) LPTxD is recessive or the LIN Physical Layer is in shutdown or receive only mode for a minimum of a transmit bit time.

To re-enable the transmitter then, the LPOCIF flag must be cleared (by writing a 1).

NOTE

Please make sure that LPOCIF=1 before trying to clear it. It is not allowed to try to clear LPOCIF if LPOCIF=0 already.

After clearing LPOCIF, if the overcurrent condition is still present or the LPTxD pin is dominant while being in normal mode, the transmitter remains disabled and the LPOCIF flag is set again after a time to indicate that the attempt to re-enable has failed. This time is equal to:

- minimum 1 IRC period (1 us) + 2 bus periods
- maximum 2 IRC periods (2 us) + 3 bus periods

If the bit LPOCIE is set in the LPIE register, an interrupt is requested.

Figure 16-12 shows the different scenarios for overcurrent interrupt handling.

16.5 Application Information

16.5.1 Module Initialization

The following steps should be used to configure the module before starting the transmission:

1. Set the slew rate in the LPSLRM register to the desired transmission baud rate.
2. When using the LIN Physical Layer for other purposes than LIN transmission, de-activate the dominant timeout feature in the LPSLRM register if needed.
3. In most cases, the internal pullup should be enabled in the LPCR register.
4. Route the desired source in the PIM module to the LIN Physical Layer.
5. Select the transmit mode (Receive only mode or Normal mode) in the LPCR register.
6. If the SCI is selected as source, activate the wake-up feature in the LPCR register if needed for the application (SCI active edge interrupt must also be enabled).
7. Enable the LIN Physical Layer in the LPCR register.
8. Wait for a minimum of a transmit bit.
9. Begin transmission if needed.

NOTE

It is not allowed to try to clear LPOCIF or LPDTIF if they are already cleared. Before trying to clear an error flag, always make sure that it is already set.

16.5.2 Interrupt handling in Interrupt Service Routine (ISR)

Both interrupts (TxD-dominant timeout and overcurrent) represent a failure in transmission. To avoid more disturbances on the transmission line, the transmitter is de-activated in both cases. The interrupt subroutine must take care of clearing the error condition and starting the routine that re-enables the transmission. For that purpose, the following steps are recommended:

1. First, the cause of the interrupt must be cleared:
   — The overcurrent will be gone after the transmitter has been disabled.
   — The TxD-dominant timeout condition will be gone once the selected source for LPTxD has turned recessive.
2. Clear the corresponding enable bit (LPDTIE or LPOCIE) to avoid entering the ISR again until the flags are cleared.
3. Notify the application of the error condition (LIN Error handler) and leave the ISR.

In the LIN Error handler, the following sequence is recommended:

1. Disable the LIN Physical Layer (LPCR) while re-configuring the transmission.
   — If the receiver must remain enabled, set the LIN Physical Layer into receive only mode instead.
2. Do all required configurations (SCI, etc.) to re-enable the transmission.
3. Wait for a transmit bit (this is needed to successfully re-enable the transmitter).

Address & Name		7	6	5	4	3	2	1	0
FRSV5	R	0	0	0	0	0	0	0	0
	W								
FRSV6	R	0	0	0	0	0	0	0	0
	W								
FRSV7	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Figure 18-3. FTMRG64K512 Register Summary (continued)

18.3.2.1 Flash Clock Divider Register (FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

	7	6	5	4	3	2	1	0
R	FDIVLD	FDIVLCK	FDIV[5:0]					
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-4. Flash Clock Divider Register (FCLKDIV)

All bits in the FCLKDIV register are readable, bit 7 is not writable, bit 6 is write-once-hi and controls the writability of the FDIV field in normal mode. In special mode, bits 6-0 are writable any number of times but bit 7 remains unwritable.

CAUTION

The FCLKDIV register should never be written while a Flash command is executing (CCIF=0).

Table 18-7. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	**Clock Divider Loaded** 0 FCLKDIV register has not been written since the last reset 1 FCLKDIV register has been written since the last reset

19.1.3 Block Diagram

The block diagram of the Flash module is shown in .

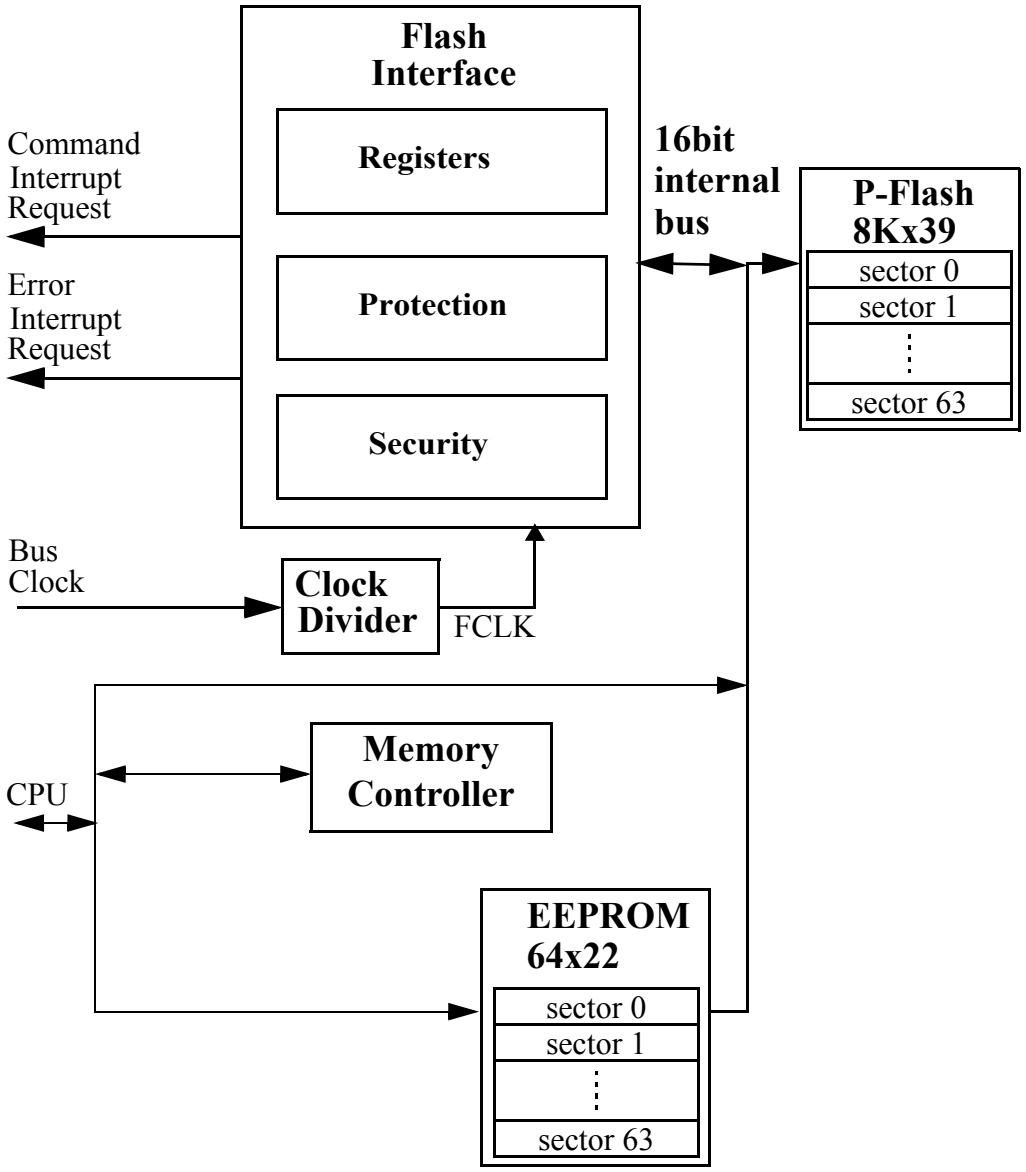

Figure 19-1. FTMRG32K128 Block Diagram

19.2 External Signal Description

The Flash module contains no signals that connect off-chip.

the remaining addresses in the Flash memory, can be activated for protection. The Flash memory addresses covered by these protectable regions are shown in the P-Flash memory map. The higher address region is mainly targeted to hold the boot loader code since it covers the vector space. Default protection settings as well as security information that allows the MCU to restrict access to the Flash module are stored in the Flash configuration field as described in Table 19-4.

Table 19-4. Flash Configuration Field

Global Address	Size (Bytes)	Description
0x3_FF00-0x3_FF07	8	Backdoor Comparison Key Refer to Section 19.4.6.11, "Verify Backdoor Access Key Command," and Section 19.5.1, "Unsecuring the MCU using Backdoor Key Access"
0x3_FF08-0x3_FF0B[1]	4	Reserved
0x3_FF0C[1]	1	P-Flash Protection byte. Refer to Section 19.3.2.9, "P-Flash Protection Register (FPROT)"
0x3_FF0D[1]	1	EEPROM Protection byte. Refer to Section 19.3.2.10, "EEPROM Protection Register (EEPROT)"
0x3_FF0E[1]	1	Flash Nonvolatile byte Refer to Section 19.3.2.16, "Flash Option Register (FOPT)"
0x3_FF0F[1]	1	Flash Security byte Refer to Section 19.3.2.2, "Flash Security Register (FSEC)"

1 0x3FF08-0x3_FF0F form a Flash phrase and must be programmed in a single command write sequence. Each byte in the 0x3_FF08 - 0x3_FF0B reserved field should be programmed to 0xFF.

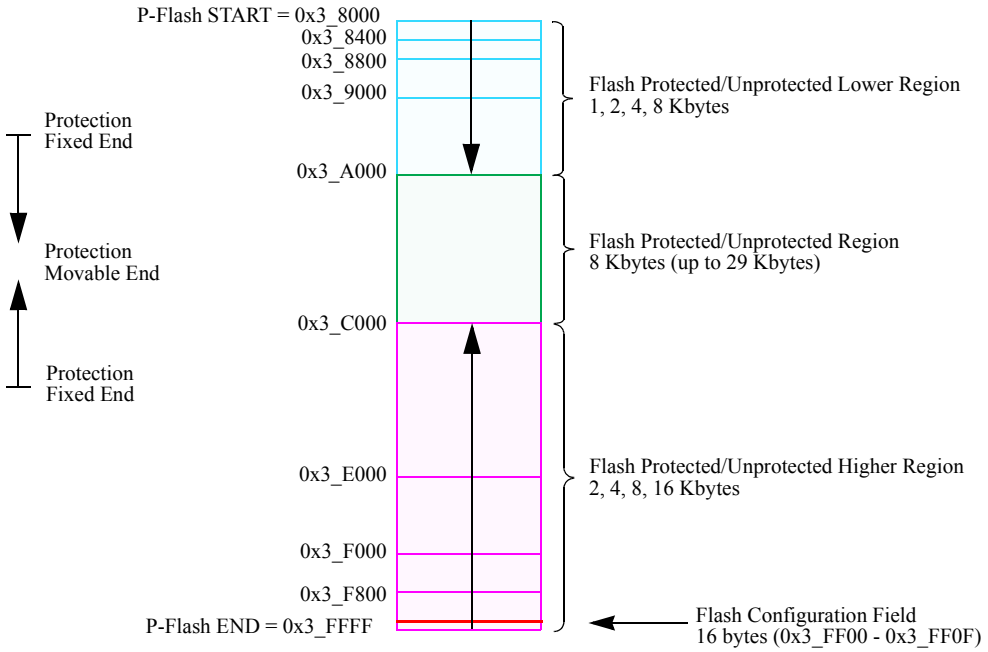

Figure 19-2. P-Flash Memory Map

Appendix B
VREG Electrical Specifications

Table B-1. Voltage Regulator Electrical Characteristics

-40°C <= T_J <= 150°C unless noted otherwise, VDDA and VDDX must be shorted on the application board.						
Num	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
1	Input Voltages	V_{SUP}	3.5	—	40	V
4	Output Voltage VDDX Full Performance Mode V_{SUP} > 6V Full Performance Mode 5.5V < V_{SUP} <=6V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode) V_{SUP} > =3.5V	V_{DDX}	 4.75 4.50 3.13 2.5	 5.0 5.0 — 5.5	 5.25 5.25 5.25 5.75	 V V V V
5	Load Current VDDX[1] [2,3] Full Performance Mode V_{SUP} > 6V Full Performance Mode 3.5V <= V_{SUP} <=6V Reduced Performance Mode (stopmode)	I_{DDX}	 0 0 0	 — — —	 70 25 5	 mA mA mA
6	Low Voltage Interrupt Assert Level[4] Low Voltage Interrupt Deassert Level	V_{LVIA} V_{LVID}	4.04 4.19	4.23 4.38	4.40 4.49	V V
7a	VDDX Low Voltage Reset deassert[5]	V_{LVRXD}	—	—	3.13	V
7b	VDDX Low Voltage Reset assert	V_{LVRXA}	2.95	3.02	—	V
8	Trimmed ACLK output frequency	f_{ACLK}	—	20	—	kHz
9	Trimmed ACLK internal clock $\Delta f / f_{nominal}$ [6]	df_{ACLK}	- 6%	—	+ 6%	—
10	The first period after enabling the counter by APIFE might be reduced by API start up delay	t_{sdel}	—	—	100	µs
11	Temperature Sensor Slope	dV_{HT}	5.05	5.25	5.45	mV/°C
12	Temperature Sensor Output Voltage (T_J=150°C)	V_{HT}	—	2.4	—	V
13	High Temperature Interrupt Assert[7] High Temperature Interrupt Deassert	T_{HTIA} T_{HTID}	120 110	132 122	144 134	°C °C

Appendix D
HSDRV Electrical Specifications

This section provides electrical parametric and ratings for the S12HSDRV1CV3 on S12VR32 and S12HSDRV2 on S12VR64. The open-load detection feature is only available on S12VR32. The ratings below which refer to open-load detection feature are only valid for S12VR32.

D.1 Operating Characteristics

Table D-1. Operating Characteristics - HSDRV

Num	Ratings	Symbol	Min	Typ	Max	Unit
1	High Voltage Supply for the high-side drivers.	V_{SUPHS}	7	–	42	V
2	VSUP_HS in case of being connected to VDDX	V_{SUPHS_X}	4.5	–	5.5	V

D.2 Static Characteristics

Table D-2. Static Characteristics - HSDRV (Junction Temperature From -40°C To +150°C)

Characteristics noted under conditions 7V ≤ VSUPHS ≤ 18 V unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_J = 25°C[1] under nominal conditions unless otherwise noted.

Num	Ratings	Symbol	Min	Typ	Max	Unit
1	Output Drain-to-Source On Resistance T_J = 150°C, $I_{PHS0/1}$ = -50 mA	$R_{DS(ON)}$	–	–	18.0	Ω
2	Over-current Threshold. The threshold is valid for each HS-driver output. **Note:** **The high-side driver is NOT intended to switch capacitive loads. A significant capacitive load on HS0/1 would induce a current when the high-side driver gate is turned on. This current will be sensed by the over-current circuitry and eventually lead to an immediate over-current shut down. In such cases of capacitive loads you can leverage the over current masking feature or handle it by software.**	I_{OCTHSX}	90	120	150	mA
3	Nominal Current for continuous operation. This value is valid for each HS-driver output.	I_{NOMHSX}	–	–	50	mA

In **Table K-3.** the timing characteristics for slave mode are listed.

Table K-3. SPI Slave Mode Timing Characteristics

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	SCK Frequency	f_{sck}	DC	—	1/4	f_{bus}
1	SCK Period	t_{sck}	4	—	∞	t_{bus}
2	Enable Lead Time	t_{lead}	4	—	—	t_{bus}
3	Enable Lag Time	t_{lag}	4	—	—	t_{bus}
4	Clock (SCK) High or Low Time	t_{wsck}	4	—	—	t_{bus}
5	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
7	Slave Access Time (time to data active)	t_a	—	—	20	ns
8	Slave MISO Disable Time	t_{dis}	—	—	22	ns
9	Data Valid after SCK Edge	t_{vsck}	—	—	$28 + 0.5 \cdot t_{bus}$ [1]	ns
10	Data Valid after $\overline{SS}$ fall	t_{vss}	—	—	$28 + 0.5 \cdot t_{bus}$ [1]	ns
11	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

[1] $0.5t_{bus}$ added due to internal synchronization delay

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

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