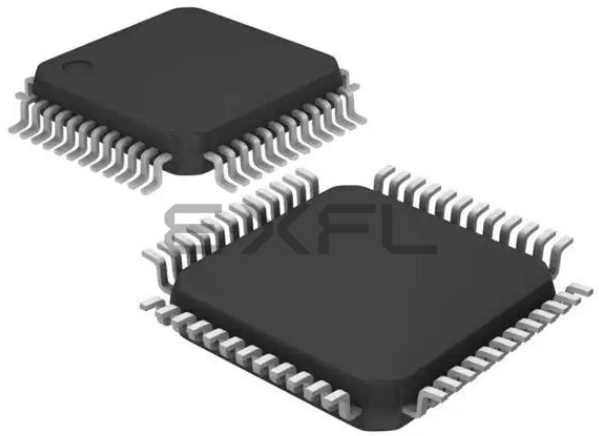

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Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
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Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vrp64f0mlf

Table 1-7. Pin Summary

LQFP			Function					Power Supply	Internal Pull Resistor	
48	32 [1]	Pin	1th Func.	2nd Func.	3rd Func.	4th Func.	5th Func.		CTRL	Reset State
1	1	LGND	—	—	—	—	—	—	—	—
2	2	LIN	—	—	—	—	—	—	—	—
3	3	LS0	OC0[2]	PWM5	PWM6	—	—	—	—	—
4	4	LSGND	—	—	—	—	—	—	—	—
5	5	LS1	OC1[3]	PWM7	—	—	—	—	—	—
6	—	VSSX1	—	—	—	—	—	—	—	—
7	—	VDDX1	—	—	—	—	—	V_{DDX}	—	—
8	6	PS2	ETRIG0	PWM4	RXD1	MISO	API_ EXTCK	V_{DDX}	PERS/PPSS	Up
9	7	PS3	ETRIG1	PWM5	TXD1	MOSI	ECLK	V_{DDX}	PERS/PPSS	Up
10	—	PS4	SCK	—	—	—	—	V_{DDX}	PERS/PPSS	Up
11	—	PS5	$\overline{SS}$	—	—	—	—	V_{DDX}	PERS/PPSS	Up
12	8	BKGD	MODC	—	—	—	—	V_{DDX}	PUCR/BKPUE	Up
13	9	TEST	—	—	—	—	—	N.A	$\overline{RESET}$ pin	Down
14	10	$\overline{RESET}$	—	—	—	—	—	V_{DDX}	TEST pin	Up
15	—	PP3	KWP3	PWM3	—	—	—	V_{DDX}	PERP/PPSP	Disabled
16	—	PP4	KWP4	ETRIG0	PWM4	—	—	V_{DDX}	PERP/PPSP	Disabled
17	—	PP5	KWP5	ETRIG1	PWM5	$\overline{IRQ}$	—	V_{DDX}	PERP/PPSP	Disabled
18	11	VSS	—	—	—	—	—	—	—	—
19	12	PE0	EXTAL	—	—	—	—	V_{DDX}	PUCR/PUPEE	Down
20	13	PE1	XTAL	—	—	—	—	V_{DDX}	PUCR/PUPEE	Down
21	14	VDDX2	—	—	—	—	—	—	—	—
22	—	PP0	KWP0	PWM0	—	—	—	V_{DDX}	PERP/PPSP	Disabled
23	15	PP1	KWP1	PWM1	$\overline{XIRQ}$	—	—	V_{DDX}	PERP/PPSP	Disabled
24	16	PP2	KWP2	EVDD	PWM2	—	—	V_{DDX}	PERP/PPSP	Disabled
25	17	VSUP	—	—	—	—	—	—	—	—
26	—	VSUPHS	—	—	—	—	—	—	—	—
27	18	HS0	OC2[4]	PWM3	—	—	—	V_{SUPHS}	—	—

Port	Pin Name	Pin Function & Priority[1]	I/O	Description	Pin Function after Reset
P	**PP5**	**$\overline{\text{IRQ}}$**	**I**	**Maskable level- or falling edge-sensitive interrupt**	GPIO
		PWM5	**O**	**Pulse Width Modulator channel 5**	
		ETRIG1	**I**	**ADC external trigger input**	
		PTP[5]/ KWP[5]	**I/O**	**General-purpose; with pin interrupt and wakeup**	
	PP4	**PWM4**	**O**	**Pulse Width Modulator channel 4**	
		ETRIG0	**I**	**ADC external trigger input**	
		PTP[4]/ KWP[4]	**I/O**	**General-purpose; with pin interrupt and wakeup**	
	PP3	**PWM3**	**O**	**Pulse Width Modulator channel 3**	
		PTP[3]/ KWP[3]	**I/O**	**General-purpose; with pin interrupt and wakeup**	
	PP2[3]	PWM2	O	Pulse Width Modulator channel 2	
		PTP[2]/ KWP[2]/ EVDD	I/O	General-purpose; with pin interrupt and wakeup	
	PP1[4]	$\overline{\text{XIRQ}}$	I	Non-maskable level-sensitive interrupt	
		PWM1	O	Pulse Width Modulator channel 1	
		PTP[1]/ KWP[1]	I/O	General-purpose; with interrupt and wakeup	
	PP0[4]	**PWM0**	**O**	**Pulse Width Modulator channel 0**	
		PTP[0]/ KWP[0]	**I/O**	**General-purpose; with interrupt and wakeup**	
L	PL3-0	PTL[3:0]/ KWL[3:0]	I	General-purpose high-voltage input (HVI); with interrupt and wakeup; optional ADC link	GPI (HVI)
AD	**PAD5-2**	**AN[5:2]**	**I**	**ADC analog**	GPIO
		PTAD[5:2]/ KWAD[5:2]	**I/O**	**General-purpose; with interrupt and wakeup**	
	PAD1-0	AN[1:0]	I	ADC analog	
		PTAD[1:0]/ KWAD[1:0]	I/O	General-purpose; with interrupt and wakeup	

1 Signals in parentheses denote alternative module routing pins. Signals in **bold underlined** are only available on S12VR64/48.

2 Function active when $\overline{\text{RESET}}$ asserted

3 High current capable high-side output (20mA) with over-current interrupt and protection for all sources (see 2.4.4.3/2-112)

4 High-current capable output (10 mA)

2.3 Memory Map and Register Definition

This section provides a detailed description of all PIM registers.

2.3.26 Port P Data Register (PTP)

Address 0x0258 (S12VR64/48) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
W								
Altern. Function	—	—	PWM5[2,3]	PWM4[2,3]	PWM3[2]	PWM2	PWM1[2]	PWM0
	—	—	$\overline{\text{IRQ}}$	—	—	EVDD	$\overline{\text{XIRQ}}$	—
	—	—	ETRIG1	ETRIG0	—	—	—	—
Reset	0	0	0	0	0	0	0	0

Figure 2-33. Port P Data Register (PTP - S12VR64/48)

1 Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

2 PWM function available on this pin only if not used with a routed HSDRV or LSDRV function. Refer to Section 2.3.16, “Module Routing Register 0 (MODRR0)”

3 PWM function available on this pin only if not routed to port S. Refer to Section 2.3.17, “Module Routing Register 1 (MODRR1)”

Address 0x0258 (S12VR32/16) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PTP2	PTP1	0
W								
Altern. Function	—	—	—	—	—	PWM2	PWM1[2]	—
	—	—	—	—	—	EVDD	$\overline{\text{XIRQ}}$	—
Reset	0	0	0	0	0	0	0	0

Figure 2-34. Port P Data Register (PTP - S12VR32/16)

1 Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

3.1.3 Features

The main features of this block are:

- Paging capability to support a global 256 KByte memory address space
- Bus arbitration between the masters CPU12, S12SBDM to different resources.
- MCU operation mode control
- MCU security control
- Generation of system reset when CPU12 accesses an unimplemented address (i.e., an address which does not belong to any of the on-chip modules) in single-chip modes

3.1.4 Modes of Operation

The S12GMMC selects the MCU's functional mode. It also determines the devices behavior in secured and unsecured state.

3.1.4.1 Functional Modes

Two functional modes are implemented on devices of the S12VR product family:

- Normal Single Chip (NS)
  The mode used for running applications.
- Special Single Chip Mode (SS)
  A debug mode which causes the device to enter BDM Active Mode after each reset. Peripherals may also provide special debug features in this mode.

3.1.4.2 Security

S12VR devices can be secured to prohibit external access to the on-chip flash. The S12GMMC module determines the access permissions to the on-chip memories in secured and unsecured state.

3.1.5 Block Diagram

Figure 3-1 shows a block diagram of the S12GMMC.

Table 4-4. CPMUFLG Field Descriptions

Field	Description
7 RTIF	**Real Time Interrupt Flag** — RTIF is set to 1 at the end of the RTI period. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (RTIE=1), RTIF causes an interrupt request. 0 RTI time-out has not yet occurred. 1 RTI time-out has occurred.
6 PORF	**Power on Reset Flag** — PORF is set to 1 when a power on reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Power on reset has not occurred. 1 Power on reset has occurred.
5 LVRF	**Low Voltage Reset Flag** — LVRF is set to 1 when a low voltage reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Low voltage reset has not occurred. 1 Low voltage reset has occurred.
4 LOCKIF	**PLL Lock Interrupt Flag** — LOCKIF is set to 1 when LOCK status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect.If enabled (LOCKIE=1), LOCKIF causes an interrupt request. 0 No change in LOCK bit. 1 LOCK bit has changed.
3 LOCK	**Lock Status Bit** — LOCK reflects the current state of PLL lock condition. Writes have no effect.While PLL is unlocked (LOCK=0) f_{PLL} is f_{VCO} / 4 to protect the system from high core clock frequencies during the PLL stabilization time tlock. 0 VCOCLK is not within the desired tolerance of the target frequency. $f_{PLL} = f_{VCO}/4$. 1 VCOCLK is within the desired tolerance of the target frequency. $f_{PLL} = f_{VCO}/(POSTDIV+1)$.
2 ILAF	**Illegal Address Reset Flag** — ILAF is set to 1 when an illegal address reset occurs.Refer to MMC chapter for details.This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Illegal address reset has not occurred. 1 Illegal address reset has occurred.
1 OSCIF	**Oscillator Interrupt Flag** — OSCIF is set to 1 when UPOSC status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect.If enabled (OSCIE=1), OSCIF causes an interrupt request. 0 No change in UPOSC bit. 1 UPOSC bit has changed.
0 UPOSC	**Oscillator Status Bit** — UPOSC reflects the status of the oscillator. Writes have no effect. Entering Full Stop Mode UPOSC is cleared. 0 The oscillator is off or oscillation is not qualified by the PLL. 1 The oscillator is qualified by the PLL.

earlier. Synchronization between the host and target is established in this manner at the start of every bit time.

Figure 5-7 shows an external host transmitting a logic 1 and transmitting a logic 0 to the BKGD pin of a target system. The host is asynchronous to the target, so there is up to a one clock-cycle delay from the host-generated falling edge to where the target recognizes this edge as the beginning of the bit time. Ten target clock cycles later, the target senses the bit level on the BKGD pin. Internal glitch detect logic requires the pin be driven high no later that eight target clock cycles after the falling edge for a logic 1 transmission.

Since the host drives the high speedup pulses in these two cases, the rising edges look like digitally driven signals.

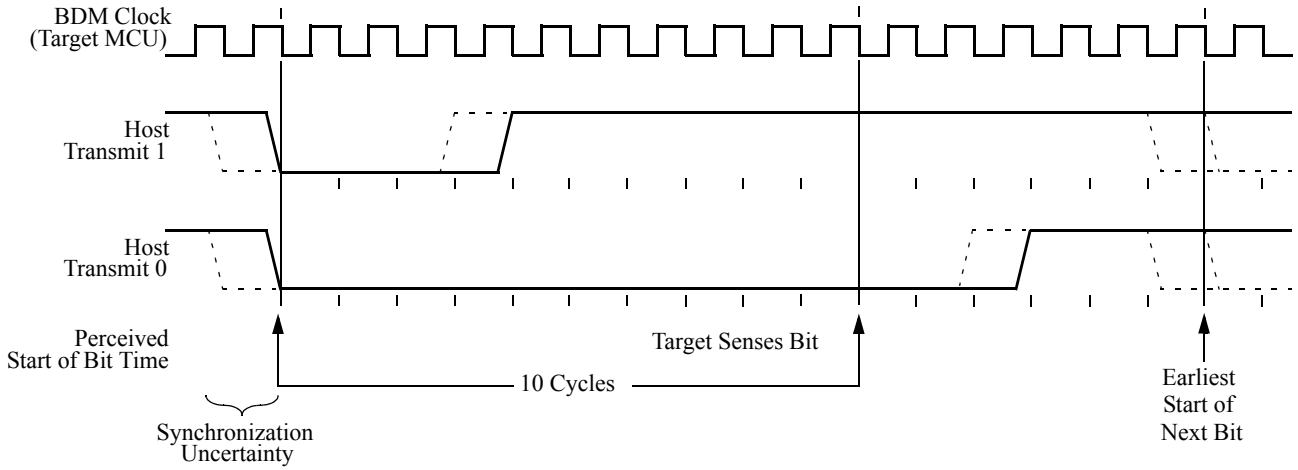

Figure 5-7. BDM Host-to-Target Serial Bit Timing

The receive cases are more complicated. Figure 5-8 shows the host receiving a logic 1 from the target system. Since the host is asynchronous to the target, there is up to one clock-cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target. The host holds the BKGD pin low long enough for the target to recognize it (at least two target clock cycles). The host must release the low drive before the target drives a brief high speedup pulse seven target clock cycles after the perceived start of the bit time. The host should sample the bit level about 10 target clock cycles after it started the bit time.

NOTE

This information is being provided so that the MCU integrator will be aware that such a conflict could occur.

The hardware handshake protocol is enabled by the ACK_ENABLE and disabled by the ACK_DISABLE BDM commands. This provides backwards compatibility with the existing POD devices which are not able to execute the hardware handshake protocol. It also allows for new POD devices, that support the hardware handshake protocol, to freely communicate with the target device. If desired, without the need for waiting for the ACK pulse.

The commands are described as follows:

- ACK_ENABLE — enables the hardware handshake protocol. The target will issue the ACK pulse when a CPU command is executed by the CPU. The ACK_ENABLE command itself also has the ACK pulse as a response.
- ACK_DISABLE — disables the ACK pulse protocol. In this case, the host needs to use the worst case delay time at the appropriate places in the protocol.

The default state of the BDM after reset is hardware handshake protocol disabled.

All the read commands will ACK (if enabled) when the data bus cycle has completed and the data is then ready for reading out by the BKGD serial pin. All the write commands will ACK (if enabled) after the data has been received by the BDM through the BKGD serial pin and when the data bus cycle is complete. See Section 5.4.3, “BDM Hardware Commands” and Section 5.4.4, “Standard BDM Firmware Commands” for more information on the BDM commands.

The ACK_ENABLE sends an ACK pulse when the command has been completed. This feature could be used by the host to evaluate if the target supports the hardware handshake protocol. If an ACK pulse is issued in response to this command, the host knows that the target supports the hardware handshake protocol. If the target does not support the hardware handshake protocol the ACK pulse is not issued. In this case, the ACK_ENABLE command is ignored by the target since it is not recognized as a valid command.

The BACKGROUND command will issue an ACK pulse when the CPU changes from normal to background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO command will issue an ACK pulse when the CPU exits from background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO_UNTIL command is equivalent to a GO command with exception that the ACK pulse, in this case, is issued when the CPU enters into background mode. This command is an alternative to the GO command and should be used when the host wants to trace if a breakpoint match occurs and causes the CPU to enter active background mode. Note that the ACK is issued whenever the CPU enters BDM, which could be caused by a breakpoint match or by a BGND instruction being executed. The ACK pulse related to this command could be aborted using the SYNC command.

The TRACE1 command has the related ACK pulse issued when the CPU enters background active mode after one instruction of the application program is executed. The ACK pulse related to this command could be aborted using the SYNC command.

5.4.9 SYNC — Request Timed Reference Pulse

The SYNC command is unlike other BDM commands because the host does not necessarily know the correct communication speed to use for BDM communications until after it has analyzed the response to the SYNC command. To issue a SYNC command, the host should perform the following steps:

1. Drive the BKGD pin low for at least 128 cycles at the lowest possible BDM serial communication frequency (The lowest serial communication frequency is determined by the settings for the VCO clock (CPMUSYNR). The BDM clock frequency is always VCO clock frequency divided by 8.)
2. Drive BKGD high for a brief speedup pulse to get a fast rise time (this speedup pulse is typically one cycle of the host clock.)
3. Remove all drive to the BKGD pin so it reverts to high impedance.
4. Listen to the BKGD pin for the sync response pulse.

Upon detecting the SYNC request from the host, the target performs the following steps:

1. Discards any incomplete command received or bit retrieved.
2. Waits for BKGD to return to a logic one.
3. Delays 16 cycles to allow the host to stop driving the high speedup pulse.
4. Drives BKGD low for 128 cycles at the current BDM serial communication frequency.
5. Drives a one-cycle high speedup pulse to force a fast rise time on BKGD.
6. Removes all drive to the BKGD pin so it reverts to high impedance.

The host measures the low time of this 128 cycle SYNC response pulse and determines the correct speed for subsequent BDM communications. Typically, the host can determine the correct communication speed within a few percent of the actual target speed and the communication protocol can easily tolerate speed errors of several percent.

As soon as the SYNC request is detected by the target, any partially received command or bit retrieved is discarded. This is referred to as a soft-reset, equivalent to a time-out in the serial communication. After the SYNC response, the target will consider the next negative edge (issued by the host) as the start of a new BDM command or the start of new SYNC request.

Another use of the SYNC command pulse is to abort a pending ACK pulse. The behavior is exactly the same as in a regular SYNC command. Note that one of the possible causes for a command to not be acknowledged by the target is a host-target synchronization problem. In this case, the command may not have been understood by the target and so an ACK response pulse will not be issued.

5.4.10 Instruction Tracing

When a TRACE1 command is issued to the BDM in active BDM, the CPU exits the standard BDM firmware and executes a single instruction in the user code. Once this has occurred, the CPU is forced to return to the standard BDM firmware and the BDM is active and ready to receive a new command. If the TRACE1 command is issued again, the next user instruction will be executed. This facilitates stepping or tracing through the user code one instruction at a time.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x002C	DBGADH	R W	Bit 15	14	13	12	11	10	9	Bit 8
0x002D	DBGADL	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x002E	DBGADHM	R W	Bit 15	14	13	12	11	10	9	Bit 8
0x002F	DBGADLM	R W	Bit 7	6	5	4	3	2	1	Bit 0

1 This bit is visible at DBGCNT[7] and DBGSR[7]

2 This represents the contents if the Comparator A control register is blended into this address.

3 This represents the contents if the Comparator B control register is blended into this address

4 This represents the contents if the Comparator C control register is blended into this address

Figure 6-2. Quick Reference to DBG Registers

6.3.2 Register Descriptions

This section consists of the DBG control and trace buffer register descriptions in address order. Each comparator has a bank of registers that are visible through an 8-byte window between 0x0028 and 0x002F in the DBG module register address map. When ARM is set in DBGC1, the only bits in the DBG module registers that can be written are ARM, TRIG, and COMRV[1:0].

6.3.2.1 Debug Control Register 1 (DBGC1)

Address: 0x0020

	7	6	5	4	3	2	1	0
R	ARM	0	0	BDM	DBGBRK	0	COMRV	
W		TRIG						
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-3. Debug Control Register (DBGC1)

Read: Anytime

Write: Bits 7, 1, 0 anytime
Bit 6 can be written anytime but always reads back as 0.
Bits 4:3 anytime DBG is not armed.

NOTE

When disarming the DBG by clearing ARM with software, the contents of bits[4:3] are not affected by the write, since up until the write operation, ARM = 1 preventing these bits from being written. These bits must be cleared using a second write if required.

8.3.2.10 ATD Input Enable Register (ATDDIEN)

Module Base + 0x000C

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	1	1	1	1	1	1	1	1	1	1	IEN[5:0]					
W																
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-12. ATD Input Enable Register (ATDDIEN)

Read: Anytime

Write: Anytime

Table 8-19. ATDDIEN Field Descriptions

Field	Description
5–0 IEN[5:0]	**ATD Digital Input Enable on channel *x* (*x*= 5, 4, 3, 2, 1, 0)** — This bit controls the digital input buffer from the analog input pin (AN*x*) to the digital data register. 0 Disable digital input buffer to AN*x* pin 1 Enable digital input buffer on AN*x* pin. **Note:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

8.3.2.11 ATD Compare Higher Than Register (ATDCMPHT)

Writes to this register will abort current conversion sequence.

Read: Anytime

Write: Anytime

Module Base + 0x000E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	CMPHT[5:0]					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-13. ATD Compare Higher Than Register (ATDCMPHT)

Table 8-20. ATDCMPHT Field Descriptions

Field	Description
5–0 CMPHT[5:0]	**Compare Operation Higher Than Enable for conversion number *n* (*n*= 5, 4, 3, 2, 1, 0) of a Sequence (*n conversion number, NOT channel number!)*** — This bit selects the operator for comparison of conversion results. 0 If result of conversion *n* is **lower or same than** compare value in ATDDR*n*, this is flagged in ATDSTAT2 1 If result of conversion *n* is **higher than** compare value in ATDDR*n*, this is flagged in ATDSTAT2

8.5 Resets

At reset the ADC12B6CV2 is in a power down state. The reset state of each individual bit is listed within the Register Description section (see Section 8.3.2, “Register Descriptions”) which details the registers and their bit-field.

8.6 Interrupts

The interrupts requested by the ADC12B6CV2 are listed in Table 8-24. Refer to MCU specification for related vector address and priority.

Table 8-24. ATD Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Sequence Complete Interrupt	I bit	ASCIE in ATDCTL2
Compare Interrupt	I bit	ACMPIE in ATDCTL2

See Section 8.3.2, “Register Descriptions” for further details.

10.4.6.5.2 Fast Data Tolerance

Figure 10-29 shows how much a fast received frame can be misaligned. The fast stop bit ends at RT10 instead of RT16 but is still sampled at RT8, RT9, and RT10.

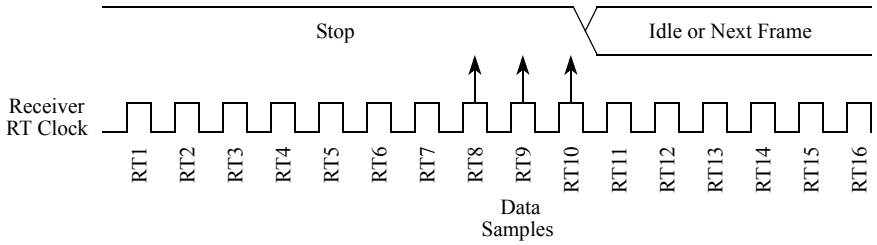

Figure 10-29. Fast Data

For an 8-bit data character, it takes the receiver 9 bit times x 16 RTr cycles + 9 RTr cycles = 153 RTr cycles to finish data sampling of the stop bit.

With the misaligned character shown in Figure 10-29, the receiver counts 153 RTr cycles at the point when the count of the transmitting device is 10 bit times x 16 RTt cycles = 160 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit character with no errors is:

((160 – 153) / 160) x 100 = 4.375%

For a 9-bit data character, it takes the receiver 10 bit times x 16 RTr cycles + 9 RTr cycles = 169 RTr cycles to finish data sampling of the stop bit.

With the misaligned character shown in Figure 10-29, the receiver counts 169 RTr cycles at the point when the count of the transmitting device is 11 bit times x 16 RTt cycles = 176 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit character with no errors is:

((176 – 169) /176) x 100 = 3.98%

NOTE

Due to asynchronous sample and internal logic, there is maximal 2 bus cycles between startbit edge and 1st RT clock, and cause to additional tolerance loss at worst case. The loss should be 2/SBR/10*100%, it is small.For example, for highspeed baud=230400 with 25MHz bus, SBR should be 109, and the tolerance loss is 2/109/10*100=0.18%, and fast data tolerance is 4.375%-0.18%=4.195%.

10.4.6.6 Receiver Wakeup

To enable the SCI to ignore transmissions intended only for other receivers in multiple-receiver systems, the receiver can be put into a standby state. Setting the receiver wakeup bit, RWU, in SCI control register 2 (SCICR2) puts the receiver into standby state during which receiver interrupts are disabled.The SCI will still load the receive data into the SCIDRH/L registers, but it will not set the RDRF flag.

Only bits related to implemented channels are valid.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 TIOS	R	RESERVED	RESERVED	RESERVED	RESERVED	IOS3	IOS2	IOS1	IOS0
	W								
0x0001 CFORC	R	0	0	0	0	0	0	0	0
	W	RESERVED	RESERVED	RESERVED	RESERVED	FOC3	FOC2	FOC1	FOC0
0x0004 TCNTH	R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
	W								
0x0005 TCNTL	R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
	W								
0x0006 TSCR1	R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
	W								
0x0007 TTOV	R	RESERVED	RESERVED	RESERVED	RESERVED	TOV3	TOV2	TOV1	TOV0
	W								
0x0008 TCTL1	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	W								
0x0009 TCTL2	R	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
	W								
0x000A TCTL3	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	W								
0x000B TCTL4	R	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
	W								
0x000C TIE	R	RESERVED	RESERVED	RESERVED	RESERVED	C3I	C2I	C1I	C0I
	W								
0x000D TSCR2	R	TOI	0	0	0	RESERVED	PR2	PR1	PR0
	W								
0x000E TFLG1	R	RESERVED	RESERVED	RESERVED	RESERVED	C3F	C2F	C1F	C0F
	W								
0x000F TFLG2	R	TOF	0	0	0	0	0	0	0
	W								
0x0010–0x001F TCxH–TCxL[1]	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
0x0024–0x002B Reserved	R								
	W								
0x002C OCPD	R	RESERVED	RESERVED	RESERVED	RESERVED	OCPD3	OCPD2	OCPD1	OCPD0
	W								
0x002D Reserved	R								
0x002E PTPSR	R	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
	W								
0x002F Reserved	R								
	W								

Figure 12-3. TIM16B4CV3 Register Summary

Table 18-17. FPROT Field Descriptions (continued)

Field	Description
2 FPLDIS	**Flash Protection Lower Address Range Disable** — The FPLDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory beginning with global address 0x3_8000. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
1–0 FPLS[1:0]	**Flash Protection Lower Address Size** — The FPLS bits determine the size of the protected/unprotected area in P-Flash memory as shown in Table 18-20. The FPLS bits can only be written to while the FPLDIS bit is set.

Table 18-18. P-Flash Protection Function

FPOPEN	FPHDIS	FPLDIS	Function[1]
1	1	1	No P-Flash Protection
1	1	0	Protected Low Range
1	0	1	Protected High Range
1	0	0	Protected High and Low Ranges
0	1	1	Full P-Flash Memory Protected
0	1	0	Unprotected Low Range
0	0	1	Unprotected High Range
0	0	0	Unprotected High and Low Ranges

1 For range sizes, refer to Table 18-19 and Table 18-20.

Table 18-19. P-Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0x3_F800–0x3_FFFF	2 Kbytes
01	0x3_F000–0x3_FFFF	4 Kbytes
10	0x3_E000–0x3_FFFF	8 Kbytes
11	0x3_C000–0x3_FFFF	16 Kbytes

Table 18-20. P-Flash Protection Lower Address Range

FPLS[1:0]	Global Address Range	Protected Size
00	0x3_8000–0x3_83FF	1 Kbyte
01	0x3_8000–0x3_87FF	2 Kbytes
10	0x3_8000–0x3_8FFF	4 Kbytes
11	0x3_8000–0x3_9FFF	8 Kbytes

All possible P-Flash protection scenarios are shown in Figure 18-13 . Although the protection scheme is loaded from the Flash memory at global address 0x3_FF0C during the reset sequence, it can be changed by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in Normal Single Chip Mode while providing as much protection as possible if reprogramming is not required.

19.1.3 Block Diagram

The block diagram of the Flash module is shown in .

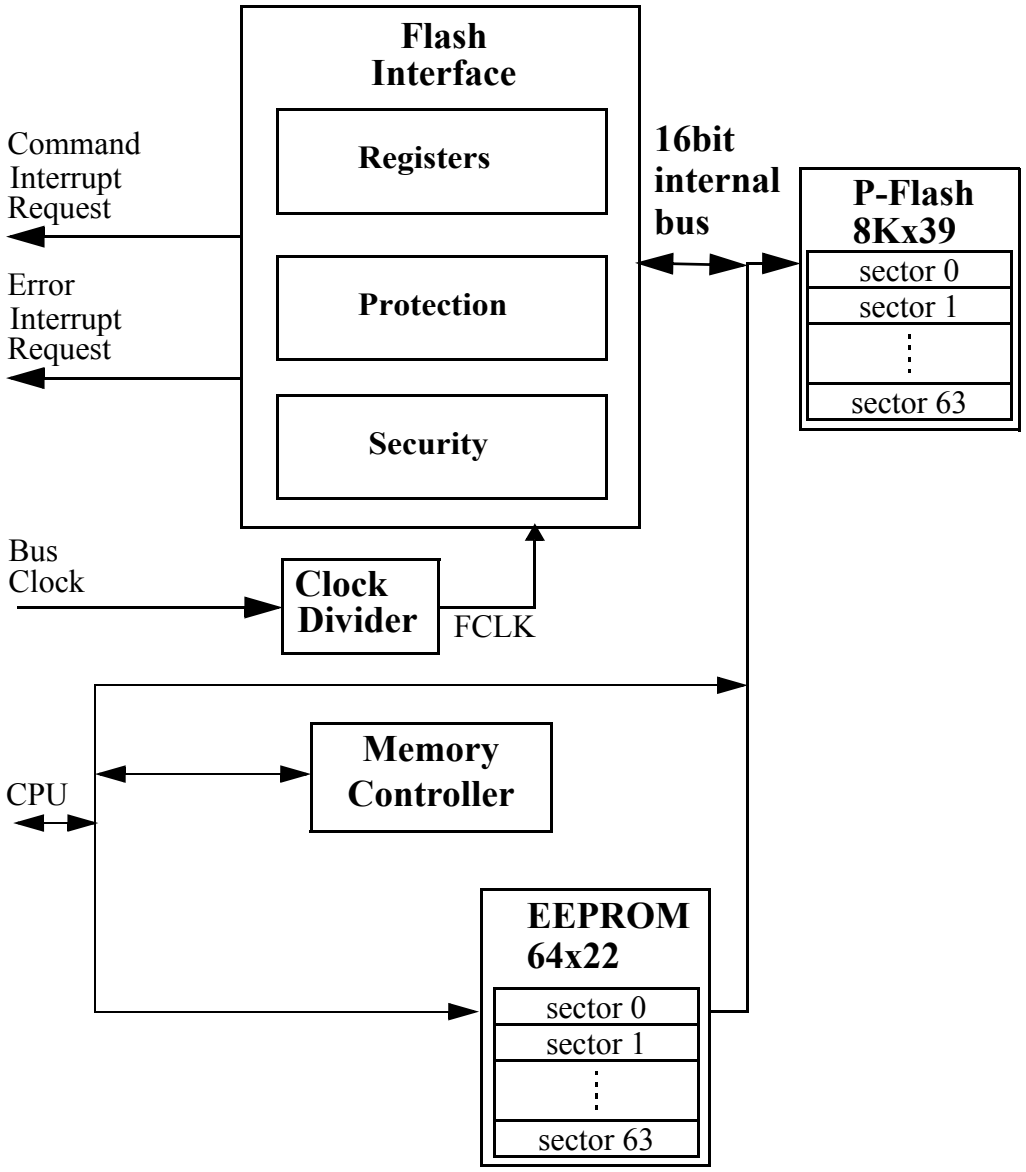

Figure 19-1. FTMRG32K128 Block Diagram

19.2 External Signal Description

The Flash module contains no signals that connect off-chip.

Table 19-5. Program IFR Fields

Global Address	Size (Bytes)	Field Description
0x0_4000 – 0x0_4007	8	Reserved
0x0_4008 – 0x0_40B5	174	Reserved
0x0_40B6 – 0x0_40B7	2	Version ID[1]
0x0_40B8 – 0x0_40BF	8	Reserved
0x0_40C0 – 0x0_40FF	64	Program Once Field Refer to Section 19.4.6.6, “Program Once Command”

1 Used to track firmware patch versions, see Section 19.4.2 IFR Version ID Word

Table 19-6. Memory Controller Resource Fields (NVMRES[1]=1)

Global Address	Size (Bytes)	Description
0x0_4000 – 0x0_40FF	256	P-Flash IFR (see Table 19-5)
0x0_4100 – 0x0_41FF	256	Reserved.
0x0_4200 – 0x0_57FF		Reserved
0x0_5800 – 0x0_59FF	512	Reserved
0x0_5A00 – 0x0_5FFF	1,536	Reserved
0x0_6000 – 0x0_6BFF	3,072	Reserved
0x0_6C00 – 0x0_7FFF	5,120	Reserved

1 NVMRES - See Section 19.4.3 Internal NVM resource (NVMRES) for NVMRES (NVM Resource) detail.

Appendix C
ATD Electrical Specifications

This section describes the characteristics of the analog-to-digital converter.

C.1 ATD Operating Characteristics

The Table C-1 and Table C-2 show conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:

$$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}.$$

This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table C-1. ATD Operating Characteristics

Supply voltage 3.13 V < V_{DDA} < 5.5 V, -40°C < T_J < 150°C						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	ATD Clock Frequency (derived from bus clock via the prescaler bus)	f_{ATDCLk}	0.25		8.0	MHz
2	ATD Conversion Period[1] 10 bit resolution: 8 bit resolution:	 N_{CONV10} N_{CONV8}	 19 17		 41 39	ATD clock Cycles

[1] The minimum time assumes a sample time of 4 ATD clock cycles. The maximum time assumes a sample time of 24 ATD clock cycles and the discharge feature (SMP_DIS) enabled, which adds 2 ATD clock cycles.

C.2 Factors Influencing Accuracy

Source resistance, source capacitance and current injection have an influence on the accuracy of the ATD. A further factor is that PortAD pins that are configured as output drivers switching.

C.2.1 Port AD Output Drivers Switching

PortAD output drivers switching can adversely affect the ATD accuracy whilst converting the analog voltage on other PortAD pins because the output drivers are supplied from the VDDA/VSSA ATD supply pins. Although internal design measures are implemented to minimize the affect of output driver noise, it is recommended to configure PortAD pins as outputs only for low frequency, low load outputs. The impact on ATD accuracy is load dependent and not specified. The values specified are valid under condition that no PortAD output drivers switch during conversion.

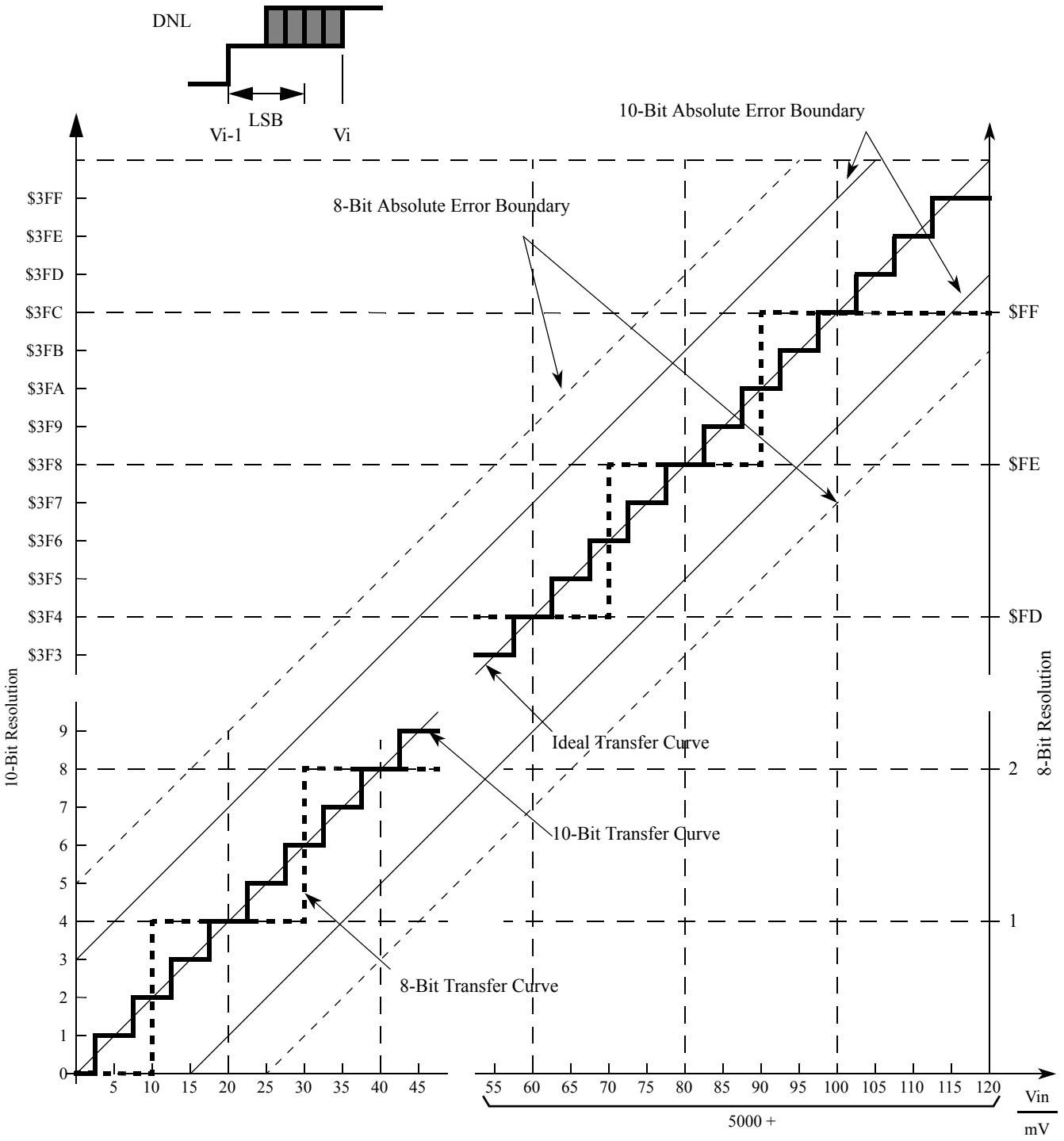

Figure C-1. ATD Accuracy Definitions

NOTE

Figure A-1 shows only definitions, for specification values refer to Table A-3 and Table A-4.

Table C-3. ATD Conversion Performance 5V range

P.31 0x0240 -0x027F Port Integration Module[1] (PIM) Map 4 of 4

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0260-0 x0268	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0269	PTIL	R	0	0	0	0	PTIL3	PTIL2	PTIL1	PTIL0
		W								
0x026A	DDRL	R	0	0	0	0	DDRL3	DDRL2	DDRL1	DDRL0
		W								
0x026B	PTAL	R	0	0	0	0	PTAENL	0	PTAL1	PTAL0
		W								
0x026C	PIRL	R	0	0	0	0	PIRL3	PIRL2	PIRL1	PIRL0
		W								
0x026D	PPSL	R	0	0	0	0	PPSL3	PPSL2	PPSL1	PPSL0
		W								
0x026E	PIEL	R	0	0	0	0	PIEL3	PIEL2	PIEL1	PIEL0
		W								
0x026F	PIFL	R	0	0	0	0	PIFL3	PIFL2	PIFL1	PIFL0
		W								
0x0270	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0271	PT1AD	R	0	0	**PT1AD5**	**PT1AD4**	**PT1AD3**	**PT1AD2**	PT1AD1	PT1AD0
		W								
0x0272	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0273	PTI1AD	R	0	0	**PTI1AD5**	**PTI1AD4**	**PTI1AD3**	**PTI1AD2**	PTI1AD1	PTI1AD0
		W								
0x0274	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0275	DDR1AD	R	0	0	**DDR1AD5**	**DDR1AD4**	**DDR1AD3**	**DDR1AD2**	DDR1AD1	DDR1AD0
		W								
0x0276-0 x0278	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0279	PER1AD	R	0	0	**PER1AD5**	**PER1AD4**	**PER1AD3**	**PER1AD2**	PER1AD1	PER1AD0
		W								
0x027A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x027B	PPS1AD	R	0	0	**PPS1AD5**	**PPS1AD4**	**PPS1AD3**	**PPS1AD2**	PPS1AD1	PPS1AD0
		W								
0x027C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x027D	PIE1AD	R	0	0	**PIE1AD5**	**PIE1AD4**	**PIE1AD3**	**PIE1AD2**	PIE1AD1	PIE1AD0
		W								
0x027E	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x027F	PIF1AD	R	0	0	**PIF1AD5**	**PIF1AD4**	**PIF1AD3**	**PIF1AD2**	PIF1AD1	PIF1AD0
		W								

[1] Register and register bits in **bold underlined** are only available on S12VR64/48. On S12VR32/16 these locations read 0 and write is not implemented.

P.32 0x0280-0x02EF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0280-0x02EF	Reserved	R	0	0	0	0	0	0	0	0
		W								

P.33 0x02F0-0x02FF Clock and Power Management Unit (CPMU) Map 2 of 2

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02F0	CPMUHTCL	R	0	0	VSEL	0	HTE	HTDS	HTIE	HTIF
		W								
0x02F1	CPMULVCTL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								
0x02F2	CPMUAPICTL	R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
		W								
0x02F3	CPMUACLKTR	R	ACLKTR5	ACLKTR4	ACLKTR3	ACLKTR2	ACLKTR1	ACLKTR0	0	0
		W								
0x02F4	CPMUAPIRH	R	APIR15	APIR14	APIR13	APIR12	APIR11	APIR10	APIR9	APIR8
		W								
0x02F5	CPMUAPIRL	R	APIR7	APIR6	APIR5	APIR4	APIR3	APIR2	APIR1	APIR0
		W								
0x02F6	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02F7	CPMUHTTR	R	HTOE	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
		W								
0x02F8	CPMU IRCTRIMH	R	TCTRIM[3:0]					0	IRCTRIM[9:8]	
		W								
0x02F9	CPMU IRCTRIML	R	IRCTRIM[7:0]							
		W								
0x02FA	CPMUOSC	R	OSCE	0	0	Reserved				
		W								
0x02FB	CPMUPROT	R	0	0	0	0	0	0	0	PROT
		W								
0x02FC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02FD	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02FE	**CPMUOSC2**[1]	R	0	0	0	0	0	0	**OMRE**	**OSCMOD**
		W								
0x02FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

[1] CPMUOSC2 Register is only available on S12VR32/16