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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10266asp-x0

Table 1-1. List of Ordering Part Numbers

	Pin count	Package	Data flash	Fields of Application	Part Number
<R>	20 pins	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)	Mounted	A	R5F1026AASP#V5, R5F10269ASP#V5, R5F10268ASP#V5, R5F10267ASP#V5, R5F10266ASP#V5 R5F1026AASP#X5, R5F10269ASP#X5, R5F10268ASP#X5, R5F10267ASP#X5, R5F10266ASP#X5
				D	R5F1026ADSP#V5, R5F10269DSP#V5, R5F10268DSP#V5, R5F10267DSP#V5, R5F10266DSP#V5 R5F1026ADSP#X5, R5F10269DSP#X5, R5F10268DSP#X5, R5F10267DSP#X5, R5F10266DSP#X5
				G	R5F1026AGSP#V5, R5F10269GSP#V5, R5F10268GSP#V5, R5F10267GSP#V5, R5F10266GSP#V5 R5F1026AGSP#X5, R5F10269GSP#X5, R5F10268GSP#X5, R5F10267GSP#X5, R5F10266GSP#X5
			Not mounted	A	R5F1036AASP#V5, R5F10369ASP#V5, R5F10368ASP#V5, R5F10367ASP#V5, R5F10366ASP#V5 R5F1036AASP#X5, R5F10369ASP#X5, R5F10368ASP#X5, R5F10367ASP#X5, R5F10366ASP#X5
				D	R5F1036ADSP#V5, R5F10369DSP#V5, R5F10368DSP#V5, R5F10367DSP#V5, R5F10366DSP#V5 R5F1036ADSP#X5, R5F10369DSP#X5, R5F10368DSP#X5, R5F10367DSP#X5, R5F10366DSP#X5
				G	R5F1036AGSP#V5, R5F10369GSP#V5, R5F10368GSP#V5, R5F10367GSP#V5, R5F10366GSP#V5 R5F1036AGSP#X5, R5F10369GSP#X5, R5F10368GSP#X5, R5F10367GSP#X5, R5F10366GSP#X5
<R>	24 pins	24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)	Mounted	A	R5F1027AANA#U5, R5F10279ANA#U5, R5F10278ANA#U5, R5F10277ANA#U5 R5F1027AANA#W5, R5F10279ANA#W5, R5F10278ANA#W5, R5F10277ANA#W5
				D	R5F1027ADNA#U5, R5F10279DNA#U5, R5F10278DNA#U5, R5F10277DNA#U5 R5F1027ADNA#W5, R5F10279DNA#W5, R5F10278DNA#W5, R5F10277DNA#W5
				G	R5F1027AGNA#U5, R5F10279GNA#U5, R5F10278GNA#U5, R5F10277GNA#U5 R5F1027AGNA#W5, R5F10279GNA#W5, R5F10278GNA#W5, R5F10277GNA#W5
			Not mounted	A	R5F1037AANA#V5, R5F10379ANA#V5, R5F10378ANA#V5, R5F10377ANA#V5 R5F1037AANA#X5, R5F10379ANA#X5, R5F10378ANA#X5, R5F10377ANA#X5
				D	R5F1037ADNA#V5, R5F10379DNA#V5, R5F10378DNA#V5, R5F10377DNA#V5 R5F1037ADNA#X5, R5F10379DNA#X5, R5F10378DNA#X5, R5F10377DNA#X5
				G	R5F1037AGSP#V5, R5F10379GSP#V5, R5F10378GSP#V5, R5F10377GSP#V5 R5F1037AGSP#X5, R5F10379GSP#X5, R5F10378GSP#X5, R5F10377GSP#X5
<R>	30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A	R5F102AAASP#V0, R5F102A9ASP#V0, R5F102A8ASP#V0, R5F102A7ASP#V0 R5F102AAASP#X0, R5F102A9ASP#X0, R5F102A8ASP#X0, R5F102A7ASP#X0
				D	R5F102AADSP#V0, R5F102A9DSP#V0, R5F102A8DSP#V0, R5F102A7DSP#V0 R5F102AADSP#X0, R5F102A9DSP#X0, R5F102A8DSP#X0, R5F102A7DSP#X0
				G	R5F102AAGSP#V0, R5F102A9GSP#V0, R5F102A8GSP#V0, R5F102A7GSP#V0 R5F102AAGSP#X0, R5F102A9GSP#X0, R5F102A8GSP#X0, R5F102A7GSP#X0
			Not mounted	A	R5F103AAASP#V0, R5F103A9ASP#V0, R5F103A8ASP#V0, R5F103A7ASP#V0 R5F103AAASP#X0, R5F103A9ASP#X0, R5F103A8ASP#X0, R5F103A7ASP#X0
				D	R5F103AADSP#V0, R5F103A9DSP#V0, R5F103A8DSP#V0, R5F103A7DSP#V0 R5F103AADSP#X0, R5F103A9DSP#X0, R5F103A8DSP#X0, R5F103A7DSP#X0
				G	R5F103AAGSP#V0, R5F103A9GSP#V0, R5F103A8GSP#V0, R5F103A7GSP#V0 R5F103AAGSP#X0, R5F103A9GSP#X0, R5F103A8GSP#X0, R5F103A7GSP#X0

Note For fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G12**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

2.3.2 Supply current characteristics

(1) 20-, 24-pin products

 $(T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V})$

(1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current ^{Note 1}	I _{DD1}	Operating mode	HS(High-speed main) mode ^{Note 4}	f _{IH} = 24 MHz ^{Note 3}	Basic operation	V _{DD} = 5.0 V		1.5		mA
						V _{DD} = 3.0 V		1.5		
					Normal operation	V _{DD} = 5.0 V		3.3	5.0	mA
						V _{DD} = 3.0 V		3.3	5.0	
						f _{IH} = 16 MHz ^{Note 3}	V _{DD} = 5.0 V		2.5	3.7
				V _{DD} = 3.0 V			2.5	3.7		
				LS(Low-speed main) mode ^{Note 4}	f _{IH} = 8 MHz ^{Note 3}	V _{DD} = 3.0 V		1.2	1.8	mA
						V _{DD} = 2.0 V		1.2	1.8	
				HS(High-speed main) mode ^{Note 4}	f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V	Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	
			f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 3.0 V			Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	
			f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 5.0 V		Square wave input		1.8	2.6	mA	
					Resonator connection		1.8	2.6		
			f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 3.0 V		Square wave input		1.8	2.6	mA	
					Resonator connection		1.8	2.6		
			LS(Low-speed main) mode ^{Note 4}	f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 3.0 V	Square wave input		1.1	1.7	mA	
					Resonator connection		1.1	1.7		
				f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 2.0 V	Square wave input		1.1	1.7	mA	
					Resonator connection		1.1	1.7		

Notes 1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.

3. When high-speed system clock is stopped

4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: $V_{DD} = 2.7\text{ V}$ to 5.5 V @ 1 MHz to 24 MHz

$V_{DD} = 2.4\text{ V}$ to 5.5 V @ 1 MHz to 16 MHz

LS(Low speed main) mode: $V_{DD} = 1.8\text{ V}$ to 5.5 V @ 1 MHz to 8 MHz

Remarks 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH} : high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$.

(2) 30-pin products

 $(T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	IDD2 ^{Note 2}	HALT mode	HS (High-speed main) mode ^{Note 6}	fIH = 24 MHz ^{Note 4}	VDD = 5.0 V		440	1280	μA	
					VDD = 3.0 V		440	1280		
				fIH = 16 MHz ^{Note 4}	VDD = 5.0 V		400	1000	μA	
					VDD = 3.0 V		400	1000		
			LS (Low-speed main) mode ^{Note 6}	fIH = 8 MHz ^{Note 4}	VDD = 3.0 V		260	530	μA	
					VDD = 2.0 V		260	530		
			HS (High-speed main) mode ^{Note 6}	fMX = 20 MHz ^{Note 3} , VDD = 5.0 V	Square wave input		280	1000	μA	
					Resonator connection		450	1170		
				fMX = 20 MHz ^{Note 3} , VDD = 3.0 V	Square wave input		280	1000	μA	
					Resonator connection		450	1170		
				fMX = 10 MHz ^{Note 3} , VDD = 5.0 V	Square wave input		190	600	μA	
					Resonator connection		260	670		
		fMX = 10 MHz ^{Note 3} , VDD = 3.0 V		Square wave input		190	600	μA		
				Resonator connection		260	670			
		LS (Low-speed main) mode ^{Note 6}	fMX = 8 MHz ^{Note 3} , VDD = 3.0 V	Square wave input		95	330	μA		
				Resonator connection		145	380			
			fMX = 8 MHz ^{Note 3} , VDD = 2.0 V	Square wave input		95	330	μA		
				Resonator connection		145	380			
	IDD3 ^{Note 5}	STOP mode	TA = −40°C					0.18	0.50	μA
			TA = +25°C					0.23	0.50	
			TA = +50°C					0.30	1.10	
			TA = +70°C					0.46	1.90	
			TA = +85°C					0.75	3.30	

Notes 1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator clock is stopped.

4. When high-speed system clock is stopped.

5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD} = 2.7\text{ V}$ to 5.5 V @ 1 MHz to 24 MHz

$V_{DD} = 2.4\text{ V}$ to 5.5 V @ 1 MHz to 16 MHz

LS (Low speed main) mode: $V_{DD} = 1.8\text{ V}$ to 5.5 V @ 1 MHz to 8 MHz

Remarks 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH} : high-speed on-chip oscillator clock frequency

3. Except STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$.

(3) Peripheral functions (Common to all products)**(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed onchip oscillator operating current	I _{FIL} ^{Note 1}				0.20		μA
12-bit interval timer operating current	I _{TMKA} ^{Notes 1, 2, 3}				0.02		μA
Watchdog timer operating current	I _{WDT} ^{Notes 1, 2, 4}	f _{IL} = 15 kHz			0.22		μA
A/D converter operating current	I _{ADC} ^{Notes 1, 5}	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.30	1.70	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.50	0.70	mA
A/D converter reference voltage operating current	I _{ADREF} ^{Note 1}				75.0		μA
Temperature sensor operating current	I _{TMPS} ^{Note 1}				75.0		μA
LVD operating current	I _{LVD} ^{Notes 1, 6}				0.08		μA
Self-programming operating current	I _{FSP} ^{Notes 1, 8}				2.00	12.20	mA
BGO operating current	I _{BGO} ^{Notes 1, 7}				2.00	12.20	mA
SNOOZE operating current	I _{SNOZ} ^{Note 1}	ADC operation	The mode is performed ^{Note 9}		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to the V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{FIL} and I_{TMKA} when the 12-bit interval timer operates.4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.6. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.

7. Current flowing only during data flash rewrite.

8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.**Remarks** 1. f_{IL}: Low-speed on-chip oscillator clock frequency2. Temperature condition of the TYP. value is T_A = 25°C

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

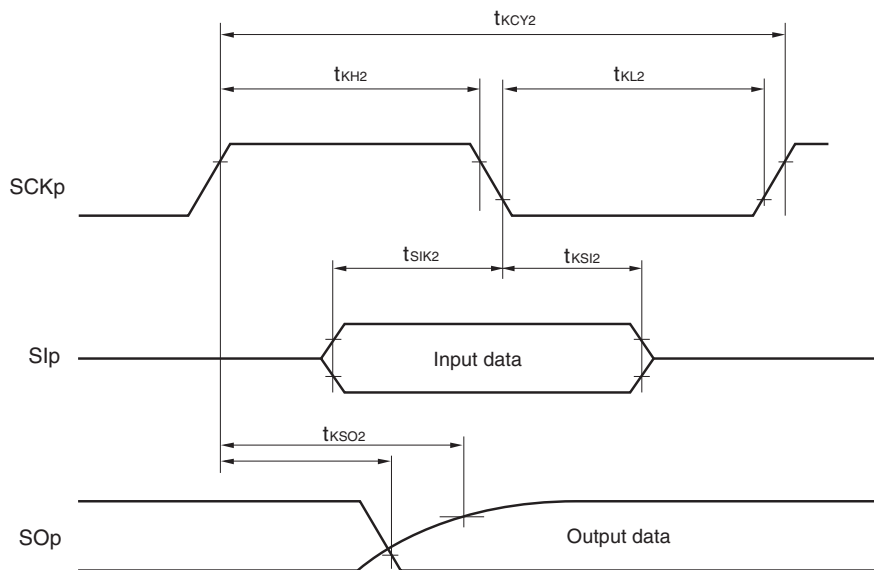
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK}	2.7 V ≤ V _{DD} ≤ 5.5 V	167		500		ns
			2.4 V ≤ V _{DD} ≤ 5.5 V	250		500		ns
			1.8 V ≤ V _{DD} ≤ 5.5 V	–		500		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V		t _{KCY1} /2–12		t _{KCY1} /2–50		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V		t _{KCY1} /2–18		t _{KCY1} /2–50		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V		t _{KCY1} /2–38		t _{KCY1} /2–50		ns
		1.8 V ≤ V _{DD} ≤ 5.5 V		–		t _{KCY1} /2–50		ns
Slp setup time (to SCKp↑) <small>Note 1</small>	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V		44		110		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V		44		110		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V		75		110		ns
		1.8 V ≤ V _{DD} ≤ 5.5 V		–		110		ns
Slp hold time (from SCKp↑) <small>Note 2</small>	t _{SH1}			19		19		ns
Delay time from SCKp↓ to SOp output <small>Note 3</small>	t _{SO1}	C = 30 pF <small>Note 4</small>			25		25	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

- Remarks**
1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products.))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		400 ^{Note1}		300 ^{Note1}	kHz
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		400 ^{Note1}		300 ^{Note1}	kHz
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, ^{Note2} C _b = 100 pF, R _b = 5.5 kΩ		300 ^{Note1}		300 ^{Note1}	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1150		1550		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1150		1550		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, ^{Note2} C _b = 100 pF, R _b = 5.5 kΩ	1550		1550		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	675		610		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	600		610		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, ^{Note2} C _b = 100 pF, R _b = 5.5 kΩ	610		610		ns
Data setup time (reception)	t _{SU:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 190 ^{Note3}		1/f _{MCK} + 190 ^{Note3}		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 ^{Note3}		1/f _{MCK} + 190 ^{Note3}		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, ^{Note2} C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 ^{Note3}		1/f _{MCK} + 190 ^{Note3}		ns
Data hold time (transmission)	t _{HD:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	355	0	355	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	0	355	ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, ^{Note2} C _b = 100 pF, R _b = 5.5 kΩ	0	405	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.2. Use it with V_{DD} ≥ V_b.3. Set t_{SU:DAT} so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

Cautions 1. Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

2. IIC01 and IIC11 cannot communicate at different potential.

(Remarks are listed on the next page.)

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-) = AV_{REFM}
ANI0 to ANI3	Refer to 28.6.1 (1).	Refer to 28.6.1 (3).	Refer to 28.6.1 (4).
ANI16 to ANI22	Refer to 28.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 28.6.1 (1).		—

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}			1.2	± 3.5	LSB
					1.2	± 7.0 ^{Note 4}	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2, ANI3	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
				57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 0.25	%FSR
						± 0.50 ^{Note 4}	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 0.25	%FSR
						± 0.50 ^{Note 4}	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 2.5	LSB
						± 5.0 ^{Note 4}	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 1.5	LSB
						± 2.0 ^{Note 4}	LSB
Analog input voltage	V_{AIN}	ANI2, ANI3		0		AV_{REFP}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} ^{Note 5}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TMPS25} ^{Note 5}			V

(Notes are listed on the next page.)

(2) 30-pin products

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V})$

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current <small>Note 1</small>	I _{DD2} <small>Note 2</small>	HALT mode	HS (High-speed main) mode <small>Note 6</small>	f _{IH} = 24 MHz <small>Note 4</small>	V _{DD} = 5.0 V		440	2300	μA
					V _{DD} = 3.0 V		440	2300	
				f _{IH} = 16 MHz <small>Note 4</small>	V _{DD} = 5.0 V		400	1700	μA
					V _{DD} = 3.0 V		400	1700	
				f _{MX} = 20 MHz <small>Note 3</small> , V _{DD} = 5.0 V	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				f _{MX} = 20 MHz <small>Note 3</small> , V _{DD} = 3.0 V	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				f _{MX} = 10 MHz <small>Note 3</small> , V _{DD} = 5.0 V	Square wave input		190	1020	μA
					Resonator connection		260	1100	
				f _{MX} = 10 MHz <small>Note 3</small> , V _{DD} = 3.0 V	Square wave input		190	1020	μA
					Resonator connection		260	1100	
	I _{DD3} <small>Note 5</small>	STOP mode	T _A = −40°C				0.18	0.50	μA
			T _A = +25°C				0.23	0.50	
			T _A = +50°C				0.30	1.10	
			T _A = +70°C				0.46	1.90	
			T _A = +85°C				0.75	3.30	
			T _A = +105°C				2.94	15.30	

Notes 1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator clock is stopped.

4. When high-speed system clock is stopped.

5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

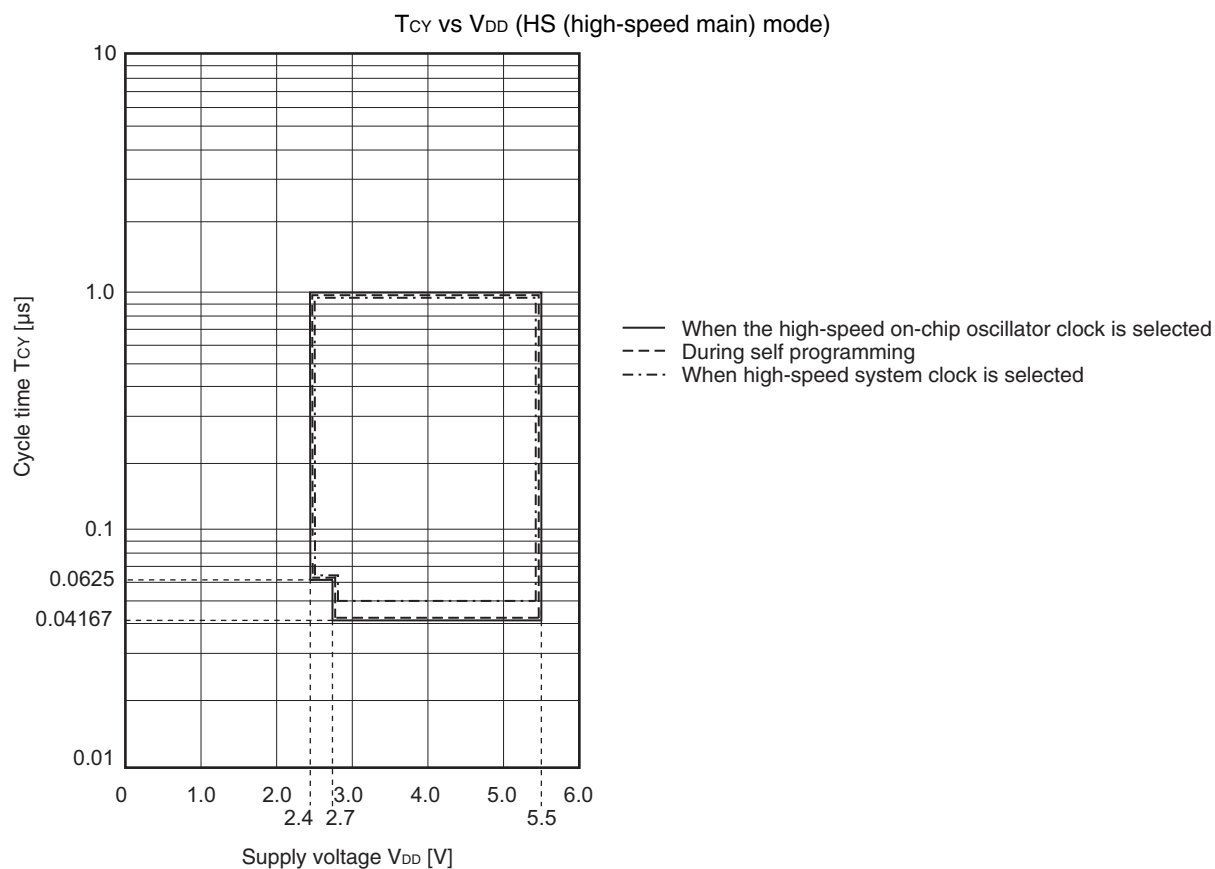
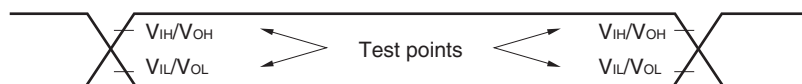
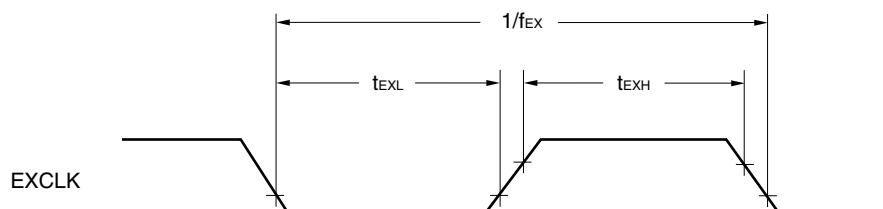
HS (High speed main) mode: $V_{DD} = 2.7\text{ V}$ to 5.5 V @ 1 MHz to 24 MHz

$V_{DD} = 2.4\text{ V}$ to 5.5 V @ 1 MHz to 16 MHz

Remarks 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH} : high-speed on-chip oscillator clock frequency

3. Except STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$.

Minimum Instruction Execution Time during Main System Clock Operation**AC Timing Test Point****External Main System Clock Timing**

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

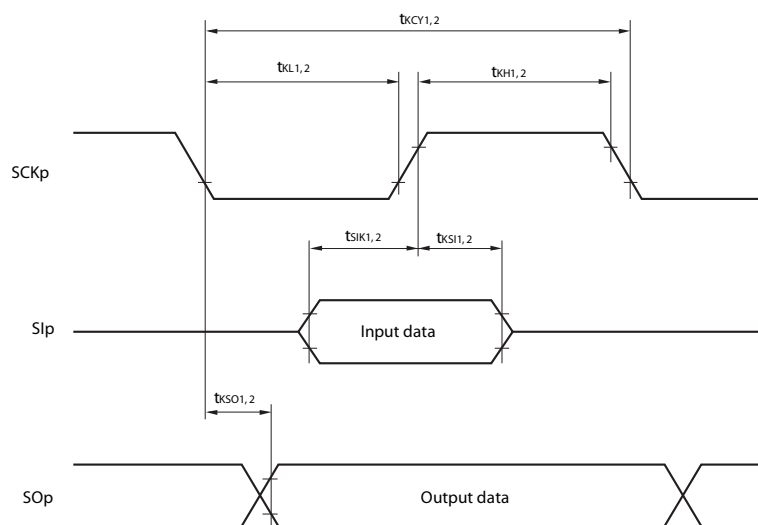
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	334	ns
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	500	ns
SCKp high-/low-level width	t_{KH1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2-24$		ns
	t_{KL1}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2-36$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2-76$		ns
Slp setup time (to SCKp \uparrow) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	113		ns
Slp hold time (from SCKp \uparrow) ^{Note 2}	t_{KSI1}		38		ns
Delay time from SCKp \downarrow to SOp output ^{Note 3}	t_{KSO1}	$C = 30\text{ pF}$ ^{Note 4}		50	ns

- Notes**
1. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 2. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 3. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The delay time to SOp output becomes “from SCKp \uparrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 4. C is the load capacitance of the SCKp and SOp output lines.

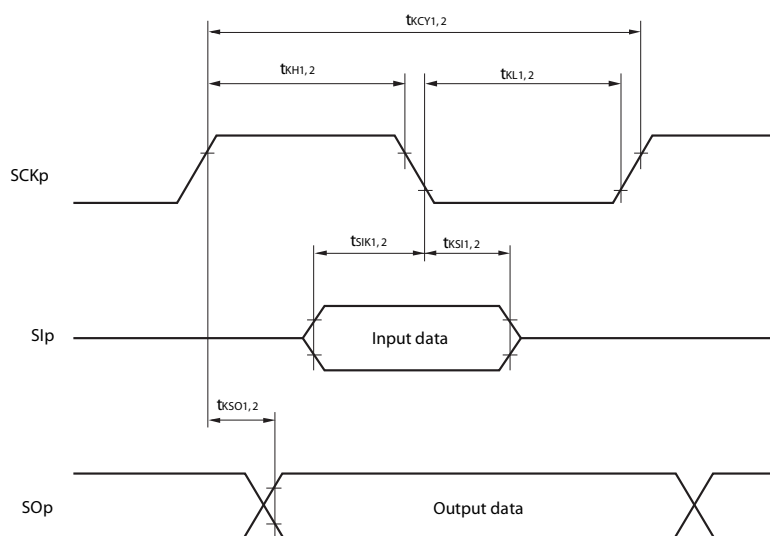
Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

- Remarks**
1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3))

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)
 2. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3))

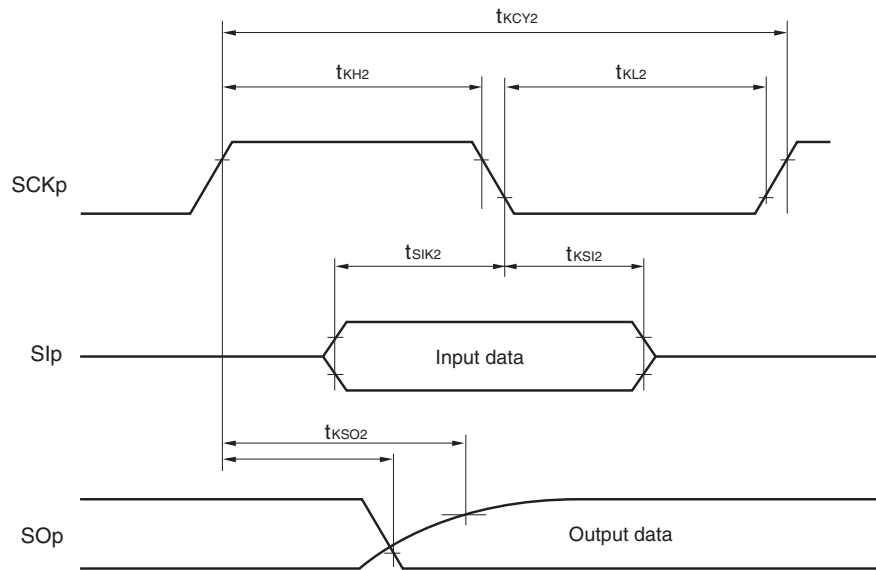
(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp \uparrow) <small>Note</small>	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	162		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	354		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	958		ns
Slp hold time (from SCKp \uparrow) <small>Note</small>	t_{KSI1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp \downarrow to SOp output <small>Note</small>	t_{KSO1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		200	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		390	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		966	ns

Note When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$.

(Cautions and Remarks are listed on the next page.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

3.5.2 Serial interface IICA

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz			0	400	kHz
		Normal mode: f _{CLK} ≥ 1 MHz	0	100			kHz
Setup time of restart condition	t _{SU:STA}		4.7		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}		4.0		0.6		μs
Hold time when SCLA0 = “L”	t _{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t _{HIGH}		4.0		0.6		μs
Data setup time (reception)	t _{SU:DAT}		250		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		0	3.45	0	0.9	μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		μs
Bus-free time	t _{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R> 2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

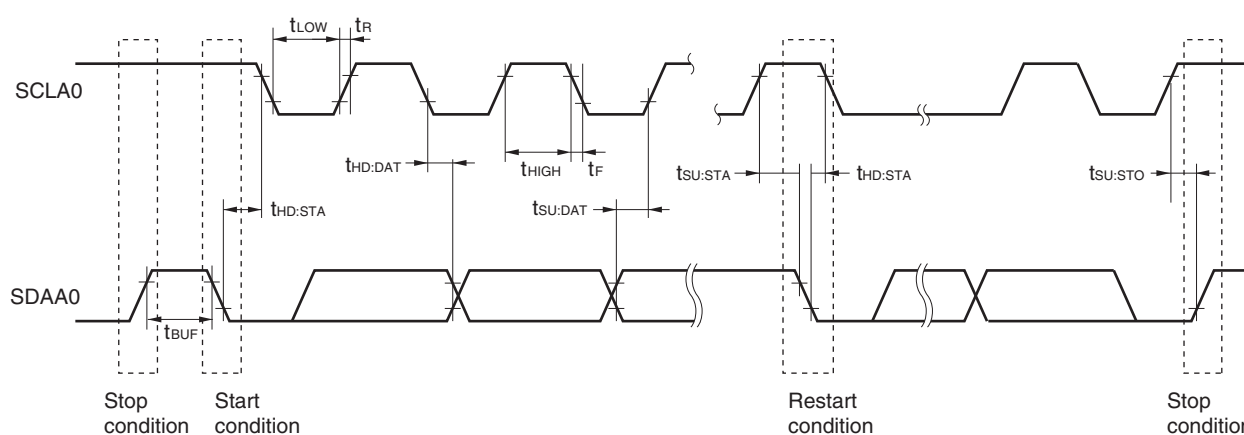
Caution Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1} , I_{OL1} , V_{OH1} , V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: $C_b = 400\text{ pF}$, $R_b = 2.7\text{ k}\Omega$

Fast mode: $C_b = 320\text{ pF}$, $R_b = 1.1\text{ k}\Omega$

IICA serial transfer timing



(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution		1.2	± 7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Conversion time	t_{CONV}	10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution			± 0.60	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution			± 4.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution			± 2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI3, ANI16 to ANI22	0		V_{DD}	V
		Internal reference voltage (HS (high-speed main) mode)	V_{BGR} ^{Note 3}			V
		Temperature sensor output voltage (HS (high-speed main) mode)	V_{TMPS25} ^{Note 3}			V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

LVD detection voltage of interrupt & reset mode**($T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVDD0}	V _{POC2} , V _{POC1} , V _{POC1} = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V _{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising reset release voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V _{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising reset release voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V _{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising reset release voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.5 Power supply voltage rising slope characteristics**($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S _{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 29.4 AC Characteristics.

3.9 Dedicated Flash Memory Programmer Communication (UART)

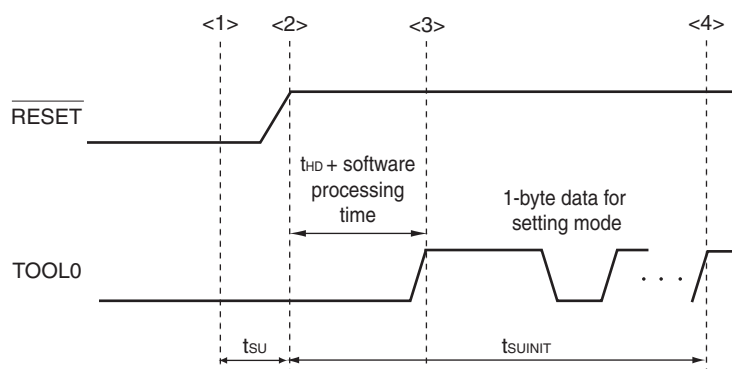
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUNIT}	POR and LVD reset are released before external release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset are released before external release	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset are released before external release	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUNIT} : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

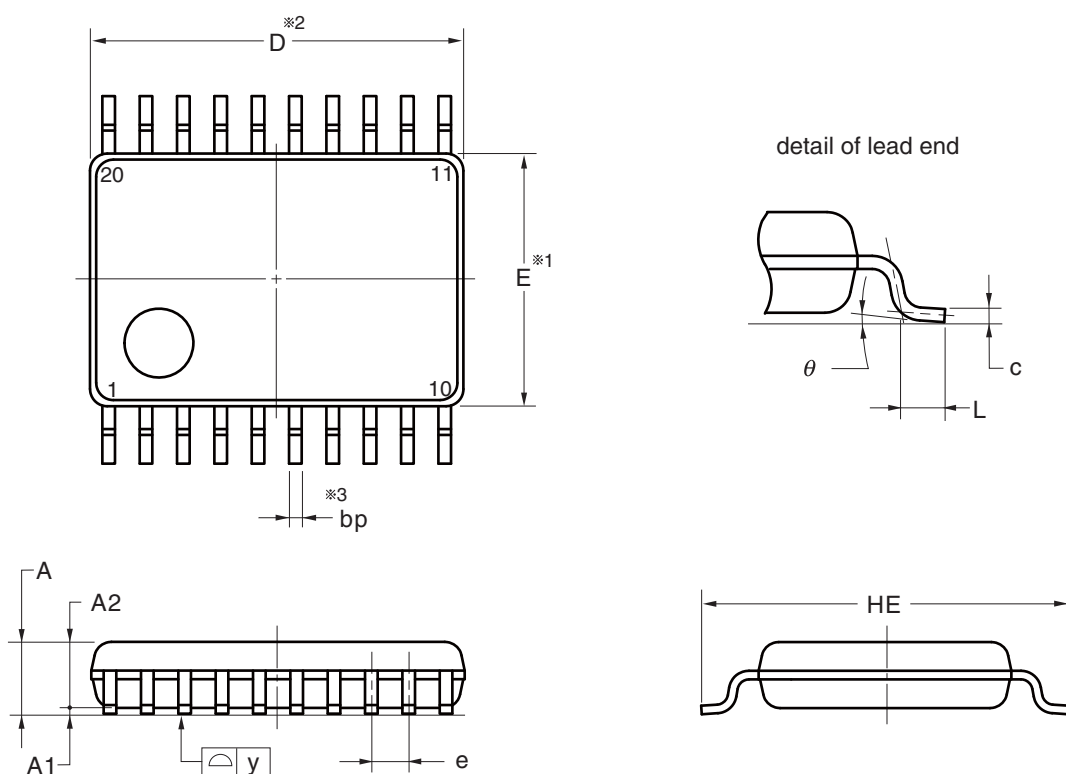
4. PACKAGE DRAWINGS

4.1 20-pin products

R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP
 R5F1036AASP, R5F10369ASP, R5F10368ASP, R5F10367ASP, R5F10366ASP
 R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP
 R5F1036ADSP, R5F10369DSP, R5F10368DSP, R5F10367DSP, R5F10366DSP
 R5F1026AGSP, R5F10269GSP, R5F10268GSP, R5F10267GSP, R5F10266GSP

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1



NOTE

1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include trim offset.

(UNIT:mm)

ITEM	DIMENSIONS
D	6.50±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.45 MAX.
A1	0.10±0.10
A2	1.15
e	0.65±0.12
bp	0.22 ^{+0.10} _{-0.05}
c	0.15 ^{+0.05} _{-0.02}
L	0.50±0.20
y	0.10
θ	0° to 10°

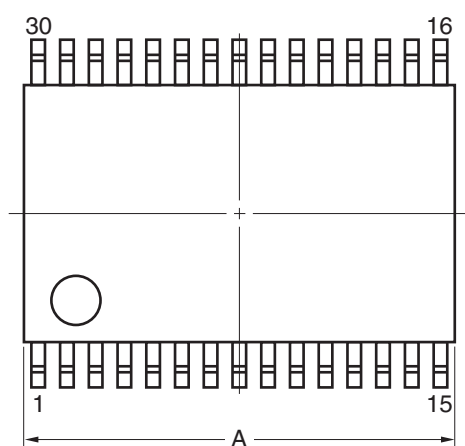
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4.3 30-pin products

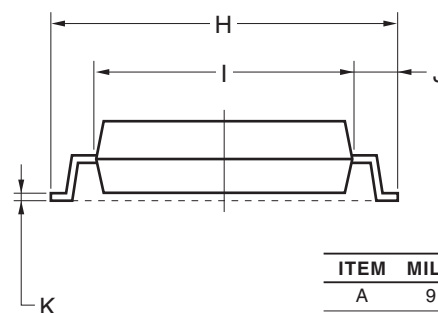
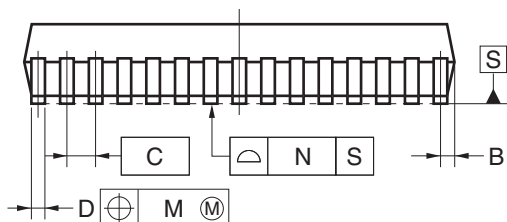
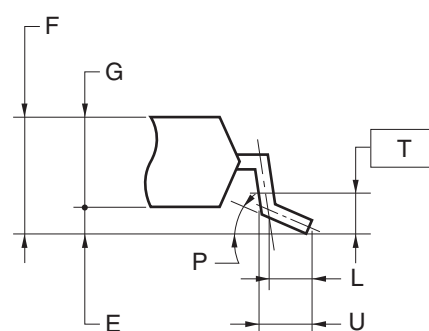
R5F102AAASP, R5F102A9ASP, R5F102A8ASP, R5F102A7ASP
 R5F103AAASP, R5F103A9ASP, R5F103A8ASP, R5F103A7ASP
 R5F102AADSP, R5F102A9DSP, R5F102A8DSP, R5F102A7DSP
 R5F103AADSP, R5F103A9DSP, R5F103A8DSP, R5F103A7DSP
 R5F102AAGSP, R5F102A9GSP, R5F102A8GSP, R5F102A7GSP

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



detail of lead end

**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15