What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10267asp-x0

○ ROM, RAM capacities

Code flash	Data flash	RAM	20 pins	24 pins	30 pins
16 KB	2 KB	2 KB	—	—	R5F102AA
	—		—	—	R5F103AA
	2 KB	1.5 KB	R5F1026A [Note 1]	R5F1027A [Note 1]	—
	—		R5F1036A [Note 1]	R5F1037A [Note 1]	—
12 KB	2KB	1 KB	R5F10269 [Note 1]	R5F10279 [Note 1]	R5F102A9
	—		R5F10369 [Note 1]	R5F10379 [Note 1]	R5F103A9
8 KB	2 KB	768 B	R5F10268 [Note 1]	R5F10278 [Note 1]	R5F102A8
	—		R5F10368 [Note 1]	R5F10378 [Note 1]	R5F103A8
4 KB	2KB	512 B	R5F10267	R5F10277	R5F102A7
	—		R5F10367	R5F10377	R5F103A7
2 KB	2 KB	256 B	R5F10266 [Note 2]	—	—
	—		R5F10366 [Note 2]	—	—

Notes 1. This is 640 bytes when the self-programming function or data flash function is used. (For details, see **CHAPTER 3 CPU ARCHITECTURE**.)

     2. The self-programming function cannot be used for R5F10266 and R5F10366.

Caution   When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

1.3.2 On-chip oscillator characteristics

(1) High-speed on-chip oscillator oscillation frequency of the R5F102 products

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = -20 to +85 °C	-1.0	+1.0	%
	T_A = -40 to -20 °C	-1.5	+1.5	
	T_A = +85 to +105 °C	-2.0	+2.0	

(2) High-speed on-chip oscillator oscillation frequency of the R5F103 products

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = -40 to + 85 °C	-5.0	+5.0	%

1.3.3 Peripheral Functions

The following are differences in peripheral functions between the R5F102 products and the R5F103 products.

RL78/G12		R5F102 product		R5F103 product	
		20, 24 pin product	30 pin product	20, 24 pin product	30 pin product
Serial interface	UART	1 channel	3 channels	1 channel	
	CSI	2 channels	3 channels	1 channel	
	Simplified I²C	2 channels	3 channels	None	
DMA function		2 channels		None	
Safety function	CRC operation	Yes		None	
	RAM guard	Yes		None	
	SFR guard	Yes		None	

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1.6.3 30-pin products
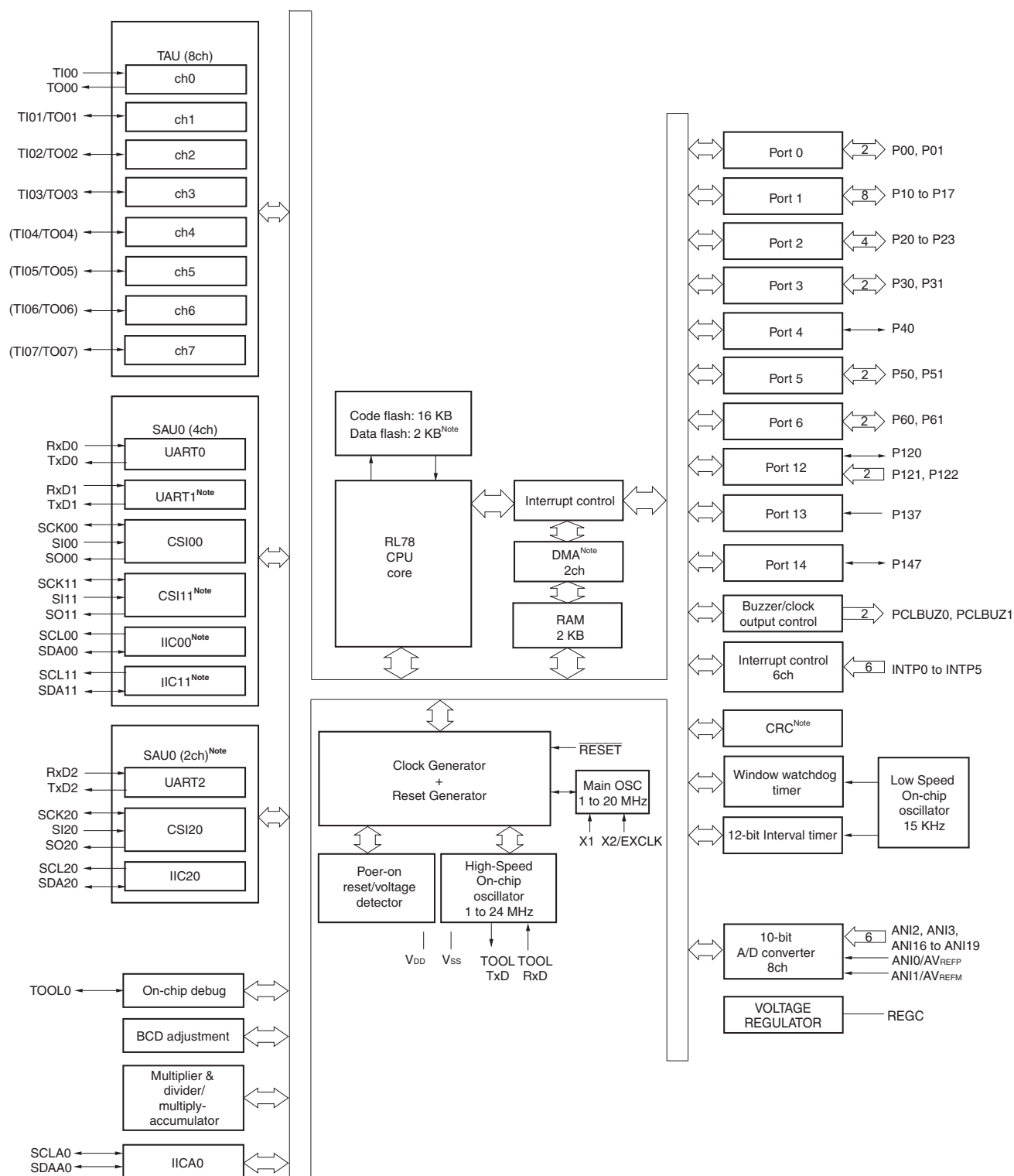
Note   Provided only in the R5F102 products.

Remark   Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

2.2 Oscillator Characteristics

2.2.1 X1 oscillator characteristics

(TA = −40 to +85°C, 1.8 V ≤ VDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx)[Note]	Ceramic resonator / crystal oscillator	2.7 V ≤ VDD ≤ 5.5 V	1.0		20.0	MHz
		1.8 V ≤ VDD < 2.7 V	1.0		8.0	

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **5.4 System Clock Oscillator**.

2.2.2 On-chip oscillator characteristics

(TA = −40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency [Notes 1, 2]	fIH			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		R5F102 products	TA = −20 to +85°C	-1.0		+1.0	%
			TA = −40 to −20°C	-1.5		+1.5	%
		R5F103 products		-5.0		+5.0	%
Low-speed on-chip oscillator clock frequency	fIL				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

(2) 30-pin products

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (High-speed main) mode [Note 6]	f$_{IH}$ = 24 MHz [Note 4]	V$_{DD}$ = 5.0 V		440	1280	μA
					V$_{DD}$ = 3.0 V		440	1280	
				f$_{IH}$ = 16 MHz [Note 4]	V$_{DD}$ = 5.0 V		400	1000	μA
					V$_{DD}$ = 3.0 V		400	1000	
			LS (Low-speed main) mode [Note 6]	f$_{IH}$ = 8 MHz [Note 4]	V$_{DD}$ = 3.0 V		260	530	μA
					V$_{DD}$ = 2.0 V		260	530	
			HS (High-speed main) mode [Note 6]	f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		280	1000	μA
					Resonator connection		450	1170	
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		280	1000	μA
					Resonator connection		450	1170	
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		190	600	μA
					Resonator connection		260	670	
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		190	600	μA
					Resonator connection		260	670	
			LS (Low-speed main) mode [Note 6]	f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
				f$_{MX}$ = 8 MHz [Note 3] V$_{DD}$ = 2.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
	I$_{DD3}$ [Note 5]	STOP mode	T$_A$ = −40°C				0.18	0.50	μA
			T$_A$ = +25°C				0.23	0.50	
			T$_A$ = +50°C				0.30	1.10	
			T$_A$ = +70°C				0.46	1.90	
			T$_A$ = +85°C				0.75	3.30	

Notes 1. Total current flowing into V$_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$ or V$_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator clock is stopped.

4. When high-speed system clock is stopped.

5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: V$_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz

V$_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS (Low speed main) mode: V$_{DD}$ = 1.8 V to 5.5 V @1 MHz to 8 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: high-speed on-chip oscillator clock frequency

3. Except STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C.

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(3) Peripheral functions (Common to all products)

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed onchip oscillator operating current	I$_{FIL}$ [Note 1]				0.20		μA
12-bit interval timer operating current	I$_{TMKA}$ [Notes 1, 2, 3]				0.02		μA
Watchdog timer operating current	I$_{WDT}$ [Notes 1, 2, 4]	f$_{IL}$ = 15 kHz			0.22		μA
A/D converter operating current	I$_{ADC}$ [Notes 1, 5]	When conversion at maximum speed	Normal mode, AV$_{REFP}$ = V$_{DD}$ = 5.0 V		1.30	1.70	mA
			Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		0.50	0.70	mA
A/D converter reference voltage operating current	I$_{ADREF}$ [Note 1]				75.0		μA
Temperature sensor operating current	I$_{TMPS}$ [Note 1]				75.0		μA
LVD operating current	I$_{LVD}$ [Notes 1, 6]				0.08		μA
Self-programming operating current	I$_{FSP}$ [Notes 1, 8]				2.00	12.20	mA
BGO operating current	I$_{BGO}$ [Notes 1, 7]				2.00	12.20	mA
SNOOZE operating current	I$_{SNOZ}$ [Note 1]	ADC operation	The mode is performed [Note 9]		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to the V$_{DD}$.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$, and I$_{FIL}$ and I$_{TMKA}$ when the 12-bit interval timer operates.

4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{WDT}$ when the watchdog timer operates.

5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I$_{DD1}$ or I$_{DD2}$ and I$_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

6. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{LVD}$ when the LVD circuit operates.

7. Current flowing only during data flash rewrite.

8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.

Remarks 1. f$_{IL}$:　　Low-speed on-chip oscillator clock frequency

2. Temperature condition of the TYP. value is T$_A$ = 25°C

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 4/f$_{CLK}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	167		500		ns
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	250		500		ns
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	−		500		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY1}$/2−12		t$_{KCY1}$/2−50		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY1}$/2−18		t$_{KCY1}$/2−50		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY1}$/2−38		t$_{KCY1}$/2−50		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		t$_{KCY1}$/2−50		ns
SIp setup time (to SCKp↑) Note 1	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V		44		110		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V		44		110		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		75		110		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		110		ns
SIp hold time (from SCKp↑) Note 2	t$_{KSI1}$			19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t$_{KSO1}$	C = 30 pF Note4			25		25	ns

Notes **1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

  2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

  3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

  4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products)

  2. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products.))

Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products.)

2. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products.))

(5) During communication at same potential (simplified I^{2}C mode)
(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode LS (low-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ		400 [Note 1]	kHz
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ		300 [Note 1]	kHz
Hold time when SCLr = "L"	t$_{LOW}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1150		ns
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1550		ns
Hold time when SCLr = "H"	t$_{HIGH}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1150		ns
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1550		ns
Data setup time (reception)	t$_{SU:DAT}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1/f$_{MCK}$ + 145 [Note 2]		ns
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1/f$_{MCK}$ + 230 [Note 2]		ns
Data hold time (transmission)	t$_{HD:DAT}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	0	355	ns
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	0	405	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

2. Set t$_{SU:DAT}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

Caution Select the N-ch open drain output (V$_{DD}$ tolerance) mode for SDAr by using port output mode register h (POMh).

(**Remarks** are listed on the next page.)

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(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)**

Parameter	Symbol	Conditions			HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
					MIN.	MAX.	MIN.	MAX.	
Transfer rate [Note4]		Reception	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V			f$_{MCK}$/6 [Note1]		f$_{MCK}$/6 [Note1]	bps
				Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note3]		4.0		1.3	Mbps
			2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V			f$_{MCK}$/6 [Note1]		f$_{MCK}$/6 [Note1]	bps
				Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note3]		4.0		1.3	Mbps
			1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V			f$_{MCK}$/6 [Notes1, 2]		f$_{MCK}$/6 [Notes1, 2]	bps
				Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note3]		4.0		1.3	Mbps
		Transmission	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V			**Note4**		**Note4**	bps
				Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 1.4 kΩ, V$_b$ = 2.7 V		2.8 [Note5]		2.8 [Note5]	Mbps
			2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V,			**Note6**		**Note6**	bps
				Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 2.7 kΩ, V$_b$ = 2.3 V		1.2 [Note7]		1.2 [Note7]	Mbps
			1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V			**Notes 2, 8**		**Notes 2, 8**	bps
				Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 5.5 kΩ, V$_b$ = 1.6 V		0.43 [Note9]		0.43 [Note9]	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

　　　　2. Use it with V$_{DD}$ ≥ V$_b$.

　　　　3. The maximum operating frequencies of the CPU/peripheral hardware clock (f$_{CLK}$) are:

　　　　　　HS (high-speed main) mode: 24 MHz (2.7 V ≤ V$_{DD}$ ≤ 5.5 V)

　　　　　　　　　　　　　　　　　　　16 MHz (2.4 V ≤ V$_{DD}$ ≤ 5.5 V)

　　　　　　LS (low-speed main) mode: 8 MHz (1.8 V ≤ V$_{DD}$ ≤ 5.5 V)

　　　　4. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

　　　　　　Expression for calculating the transfer rate when 4.0 V ≤ V$_{DD}$ ≤ 5.5 V and 2.7 V ≤ V$_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

　　　　* This value is the theoretical value of the relative difference between the transmission and reception sides.

Simplified I^{2}C mode connection diagram (during communication at different potential)
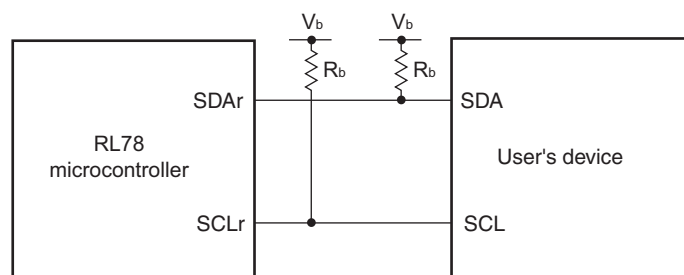
Simplified I^{2}C mode serial transfer timing (during communication at different potential)
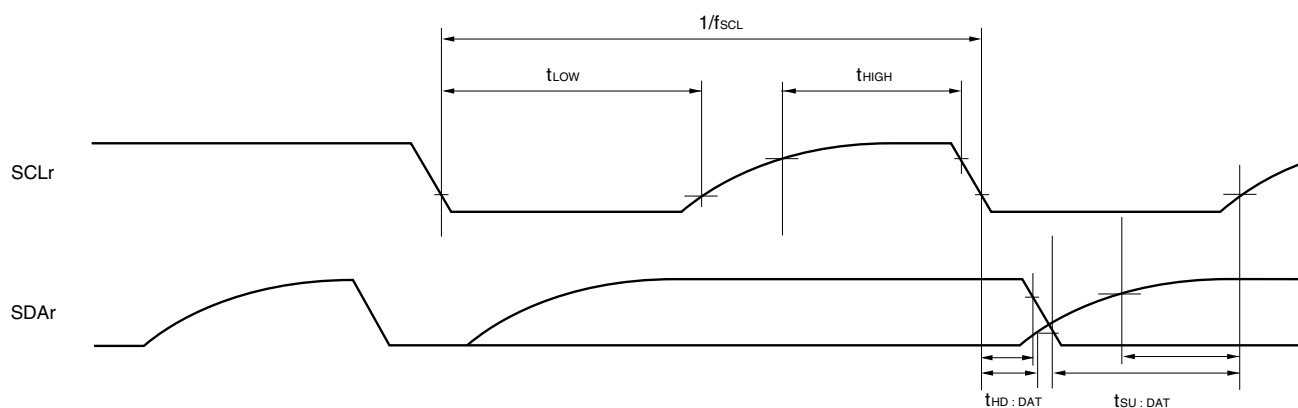
Remarks 1. R$_b$ [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C$_b$ [F]: Communication line (SDAr, SCLr) load capacitance, V$_b$ [V]: Communication line voltage

2. r: IIC Number (r = 00, 20)

3. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0,1), n: Channel number (n = 0))

4. Simplified I^{2}C mode is supported only by the R5F102 products.

2.5.2 Serial interface IICA

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode LS (low-speed main) mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode: f$_{CLK}$ ≥ 3.5 MHz			0	400	kHz
		Normal mode: f$_{CLK}$ ≥ 1 MHz	0	100			kHz
Setup time of restart condition	t$_{SU:STA}$		4.7		0.6		μs
Hold time[Note 1]	t$_{HD:STA}$		4.0		0.6		μs
Hold time when SCLA0 = "L"	t$_{LOW}$		4.7		1.3		μs
Hold time when SCLA0 = "H"	t$_{HIGH}$		4.0		0.6		μs
Data setup time (reception)	t$_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	t$_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	t$_{SU:STO}$		4.0		0.6		μs
Bus-free time	t$_{BUF}$		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

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2. The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I$_{OH1}$, I$_{OL1}$, V$_{OH1}$, V$_{OL1}$) must satisfy the values in the redirect destination.

Remark The maximum value of C$_b$ (communication line capacitance) and the value of R$_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: C$_b$ = 400 pF, R$_b$ = 2.7 kΩ
Fast mode: C$_b$ = 320 pF, R$_b$ = 1.1 kΩ

IICA serial transfer timing
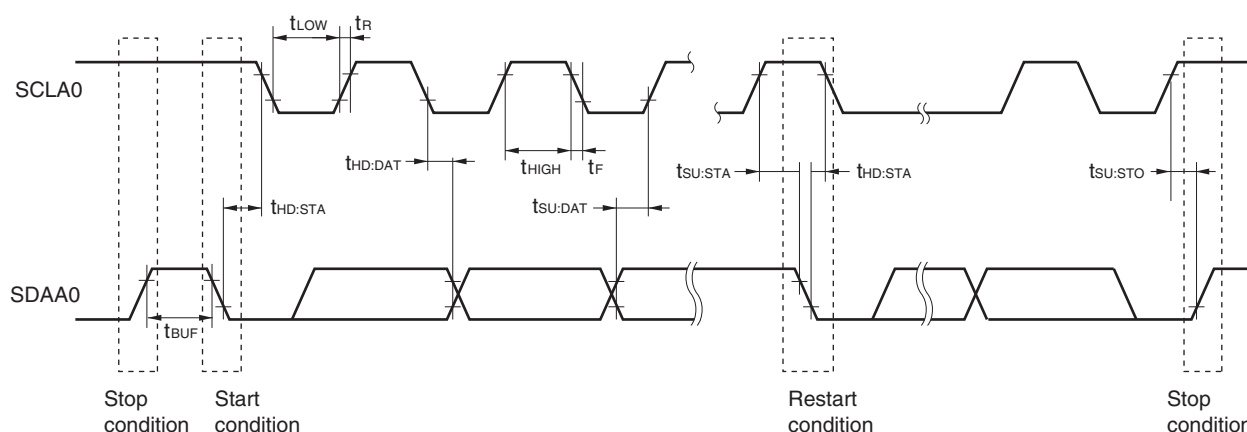
2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (−) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (−) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (−) = AV_{REFM}
ANI0 to ANI3	Refer to **28.6.1 (1)**.	Refer to **28.6.1 (3)**.	Refer to **28.6.1 (4)**.
ANI16 to ANI22	Refer to **28.6.1 (2)**.		
Internal reference voltage	Refer to **28.6.1 (1)**.		−
Temperature sensor output voltage			

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage

(T_A = −40 to +85°C, 1.8 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (−) = AV_{REFM} = 0 V)

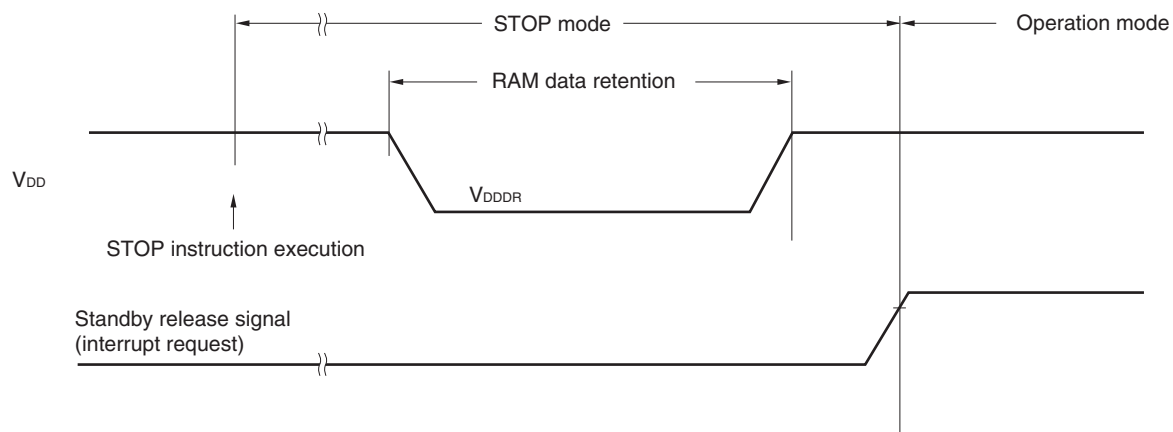| Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD} [Note 3]			1.2	±3.5	LSB
					1.2	±7.0 [Note 4]	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2, ANI3	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
				57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±0.25	%FSR
						±0.50 [Note 4]	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±0.25	%FSR
						±0.50 [Note 4]	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±2.5	LSB
						±5.0 [Note 4]	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±1.5	LSB
						±2.0 [Note 4]	LSB
Analog input voltage	V_{AIN}	ANI2, ANI3		0		AV_{REFP}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)			V_{BGR} [Note 5]		V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)			V_{TMPS25} [Note 5]		V

(**Notes** are listed on the next page.)

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<R> ## 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T$_A$ = −40 to +85°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V$_{DDDR}$		1.46 [Note]		5.5	V

<R>   **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

2.8 Flash Memory Programming Characteristics

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

<R>

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f$_{CLK}$		1		24	MHz
Code flash memory rewritable times [Notes 1, 2, 3]	C$_{erwr}$	Retained for 20 years T$_A$ = 85°C	1,000			Times
Data flash memory rewritable times [Notes 1, 2, 3]		Retained for 1 year T$_A$ = 25°C		1,000,000		
		Retained for 5 years T$_A$ = 85°C	100,000			
		Retained for 20 years T$_A$ = 85°C	10,000			

    Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

          2. When using flash memory programmer and Renesas Electronics self programming library

          3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

<R> # 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = –40 to +105°C)

<R> This chapter describes the following electrical specifications.

Target products   G: Industrial applications T_A = -40 to +105°C

<R>   R5F102xxGxx

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

      2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product.

      3. Please contact Renesas Electronics sales office for derating of operation under T_A = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
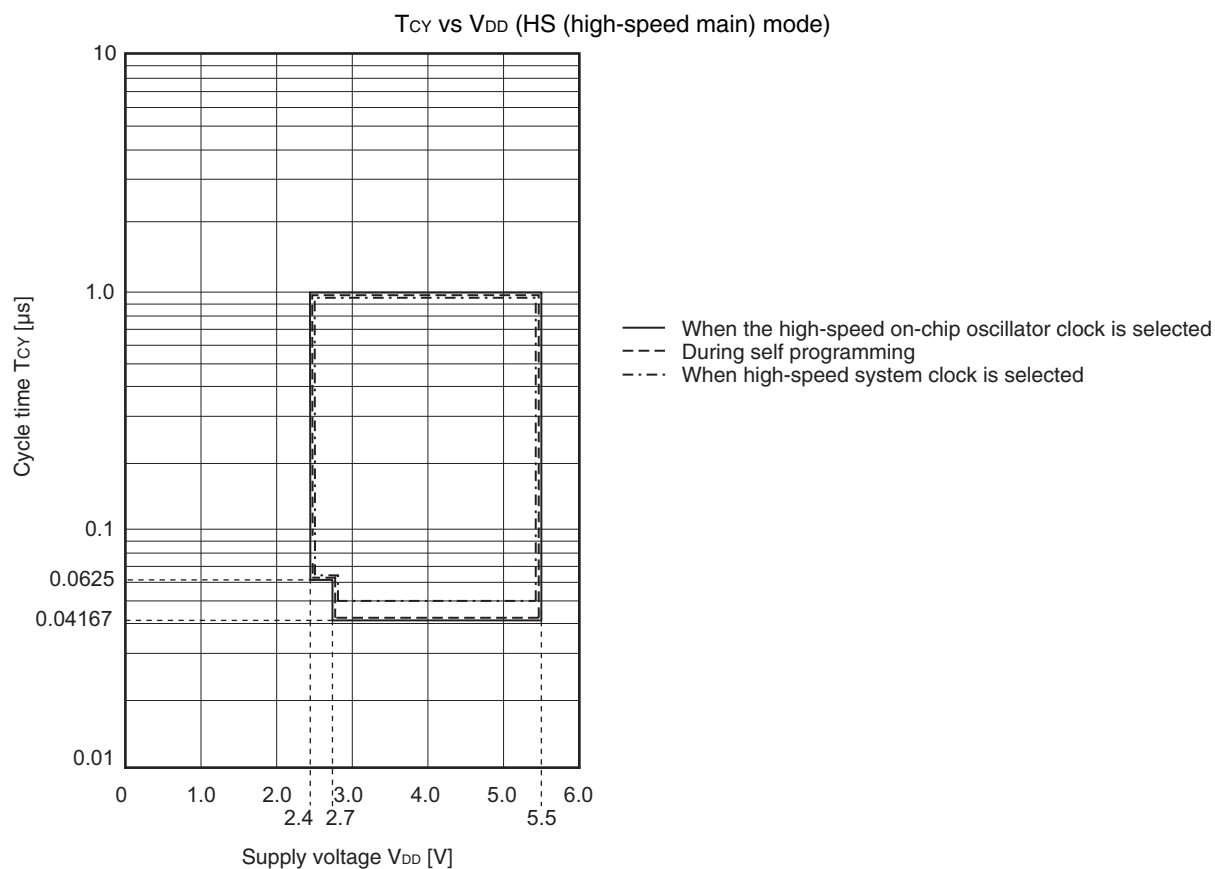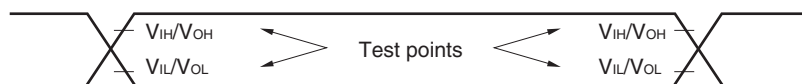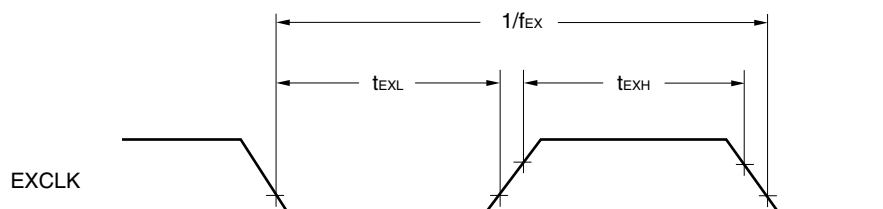
Remark   **When the RL78 microcontroller is used in the range of T_A = -40 to +85 °C, see CHAPTER 28**
<R>   **ELECTRICAL SPECIFICATIONS (A: T_A = -40 to +85 °C).**

There are following differences between the products "G: Industrial applications (T_A = -40 to +105°C)" and the products "A: Consumer applications, and D: Industrial applications".

| Parameter	Application	
	A: Consumer applications, D: Industrial applications	G: Industrial applications
Operating ambient temperature	T_A = -40 to +85°C	T_A = -40 to +105°C
Operating mode Operating voltage range	HS (high-speed main) mode: 2.7 V $\leq V_{DD} \leq$ 5.5 V @ 1 MHz to 24 MHz 2.4 V $\leq V_{DD} \leq$ 5.5 V @ 1 MHz to 16 MHz LS (low-speed main) mode: 1.8 V $\leq V_{DD} \leq$ 5.5 V @ 1 MHz to 8 MHz	HS (high-speed main) mode only: 2.7 V $\leq V_{DD} \leq$ 5.5 V @ 1 MHz to 24 MHz 2.4 V $\leq V_{DD} \leq$ 5.5 V @ 1 MHz to 16 MHz
High-speed on-chip oscillator clock accuracy	R5F102 products, 1.8 V $\leq V_{DD} \leq$ 5.5 V: $\pm$1.0% @ T_A = -20 to +85°C $\pm$1.5% @ T_A = -40 to -20°C R5F103 products, 1.8 V $\leq V_{DD} \leq$ 5.5 V: $\pm$5.0% @ T_A = -40 to +85°C	R5F102 products, 2.4 V $\leq V_{DD} \leq$ 5.5 V: $\pm$2.0% @ T_A = +85 to +105°C $\pm$1.0% @ T_A = -20 to +85°C $\pm$1.5% @ T_A = -40 to -20°C
Serial array unit	UART CSI: f_{CLK}/2 (supporting 12 Mbps), f_{CLK}/4 Simplified I²C communication	UART CSI: f_{CLK}/4 Simplified I²C communication
Voltage detector	Rise detection voltage: 1.88 V to 4.06 V (12 levels) Fall detection voltage: 1.84 V to 3.98 V (12 levels)	Rise detection voltage: 2.61 V to 4.06 V (8 levels) Fall detection voltage: 2.55 V to 3.98 V (8 levels)

Remark   The electrical characteristics of the products G: Industrial applications (T_A = -40 to +105°C) are different from those of the products "A: Consumer applications, and D: Industrial applications". For details, refer to **29.1** to **29.10**.

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Minimum Instruction Execution Time during Main System Clock Operation

T_{CY} vs V_{DD} (HS (high-speed main) mode)

— When the high-speed on-chip oscillator clock is selected
--- During self programming
-·-· When high-speed system clock is selected

AC Timing Test Point

V_{IH}/V_{OH} Test points V_{IH}/V_{OH}
V_{IL}/V_{OL} V_{IL}/V_{OL}

External Main System Clock Timing

$1/f_{EX}$

t_{EXL} t_{EXH}

EXCLK

(4) During communication at same potential (simplified I^{2}C mode)

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	C$_b$ = 100 pF, R$_b$ = 3 kΩ		100 [Note 1]	kHz
Hold time when SCLr = "L"	t$_{LOW}$	C$_b$ = 100 pF, R$_b$ = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t$_{HIGH}$	C$_b$ = 100 pF, R$_b$ = 3 kΩ	4600		ns
Data setup time (reception)	t$_{SU:DAT}$	C$_b$ = 100 pF, R$_b$ = 3 kΩ	1/f$_{MCK}$ + 580 [Note 2]		ns
Data hold time (transmission)	t$_{HD:DAT}$	C$_b$ = 100 pF, R$_b$ = 3 kΩ	0	1420	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

  2. Set t$_{SU:DAT}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

Caution Select the N-ch open drain output (V$_{DD}$ tolerance) mode for SDAr by using port output mode register h (POMh).

Simplified I^{2}C mode connection diagram (during communication at same potential)
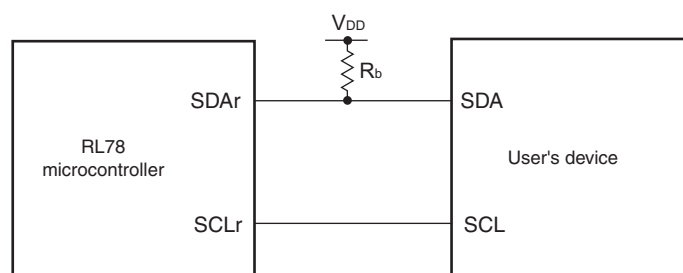
Simplified I^{2}C mode serial transfer timing (during communication at same potential)
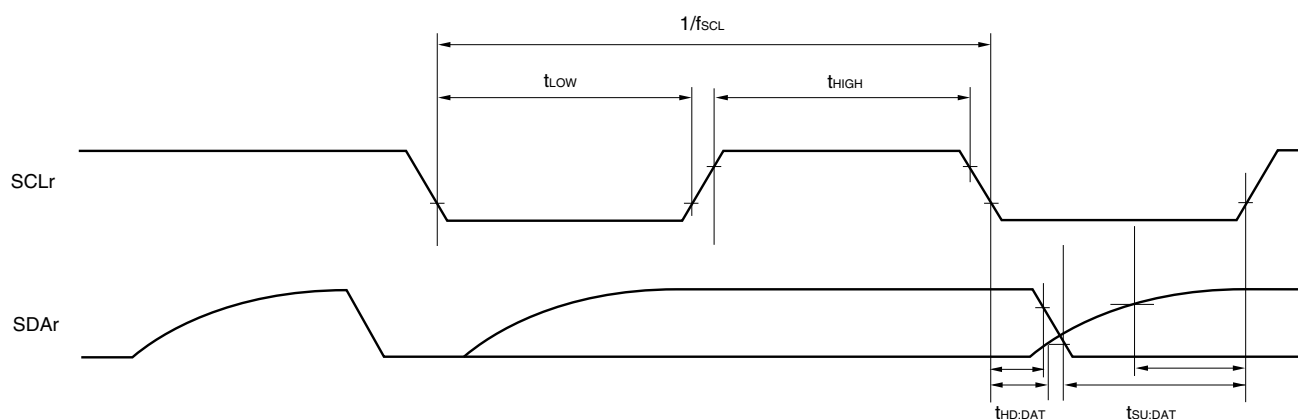
Remarks 1. R$_b$ [Ω]:Communication line (SDAr) pull-up resistance

  C$_b$ [F]: Communication line (SCLr, SDAr) load capacitance

  2. r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1, 4, 5)

  3. f$_{MCK}$: Serial array unit operation clock frequency

  (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

  m: Unit number (m = 0, 1), n: Channel number (0, 1, 3))

Simplified I^{2}C mode connection diagram (during communication at different potential)
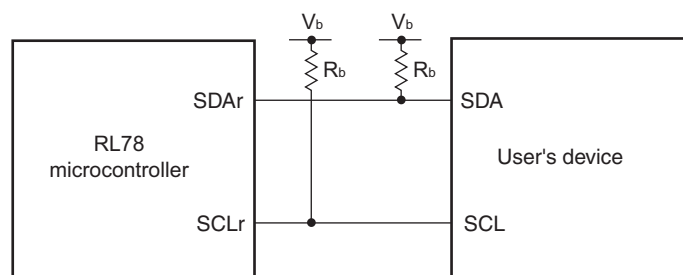
Simplified I^{2}C mode serial transfer timing (during communication at different potential)
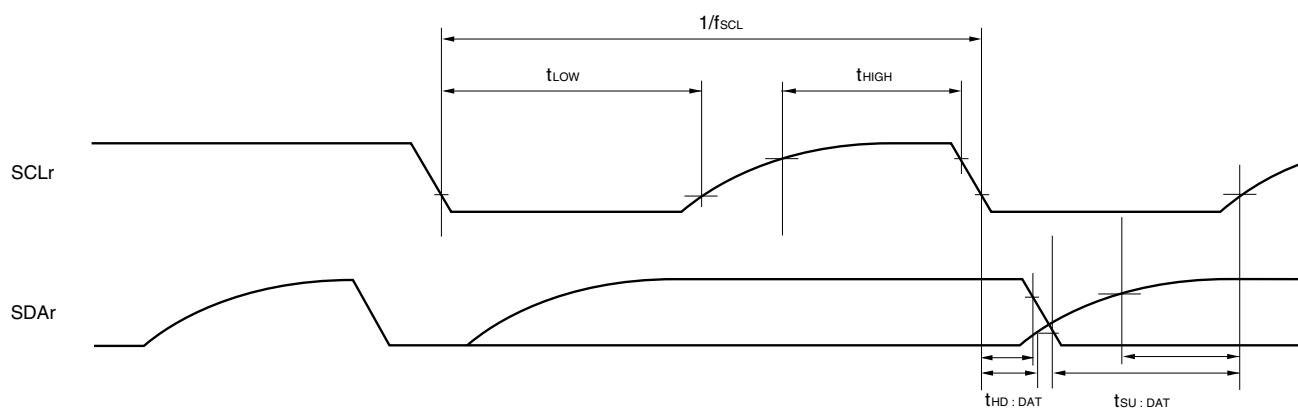
Remarks 1. R$_b$ [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C$_b$ [F]: Communication line (SDAr, SCLr) load capacitance, V$_b$ [V]: Communication line voltage

2. r: IIC Number (r = 00, 20)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number (m = 0,1), n: Channel number (n = 0))

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV$_{REFM}$ (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22

(T$_A$ = –40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = V$_{BGR}$ [Note 3], Reference voltage (–) = AV$_{REFM}$ [Note 4] = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$			8		bit
Conversion time	t$_{CONV}$	8-bit resolution	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	8-bit resolution			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution			±1.0	LSB
Analog input voltage	V$_{AIN}$		0		V$_{BGR}$ [Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V$_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = AV$_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = AV$_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = AV$_{REFM}$.

3.6.2 Temperature sensor/internal reference voltage characteristics

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V$_{TMPS25}$	Setting ADS register = 80H, T$_A$ = +25°C		1.05		V
Internal reference voltage	V$_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F$_{VTMPS}$	Temperature sensor output voltage that depends on the temperature		−3.6		mV/°C
Operation stabilization wait time	t$_{AMP}$		5			μs

3.6.3 POR circuit characteristics

(T$_A$ = −40 to +105°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V$_{POR}$	Power supply rise time	1.45	1.51	1.57	V
	V$_{PDR}$	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width [Note]	T$_{PW}$		300			μs

Note Minimum time required for a POR reset when V$_{DD}$ exceeds below V$_{PDR}$. This is also the minimum time required for a POR reset from when V$_{DD}$ exceeds below 0.7 V to when V$_{DD}$ exceeds V$_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).
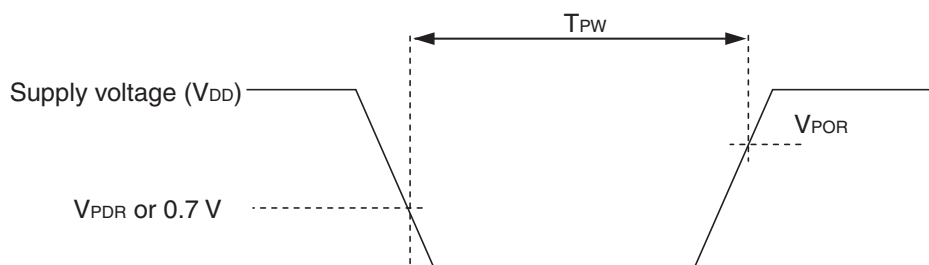
LVD detection voltage of interrupt & reset mode

(T$_A$ = −40 to +105°C, V$_{PDR}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V$_{LVDD0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC1}$ = 0, 1, 1, falling reset voltage			2.64	2.75	2.86	V
	V$_{LVDD1}$	LVIS1, LVIS0 = 1, 0	Rising reset release voltage		2.81	2.92	3.03	V
			Falling interrupt voltage		2.75	2.86	2.97	V
	V$_{LVDD2}$	LVIS1, LVIS0 = 0, 1	Rising reset release voltage		2.90	3.02	3.14	V
			Falling interrupt voltage		2.85	2.96	3.07	V
	V$_{LVDD3}$	LVIS1, LVIS0 = 0, 0	Rising reset release voltage		3.90	4.06	4.22	V
			Falling interrupt voltage		3.83	3.98	4.13	V

3.6.5 Power supply voltage rising slope characteristics

(T$_A$ = −40 to +105°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S$_{VDD}$				54	V/ms

Caution   Make sure to keep the internal reset state by the LVD circuit or an external reset until V$_{DD}$ reaches the operating voltage range shown in 29.4 AC Characteristics.

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