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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

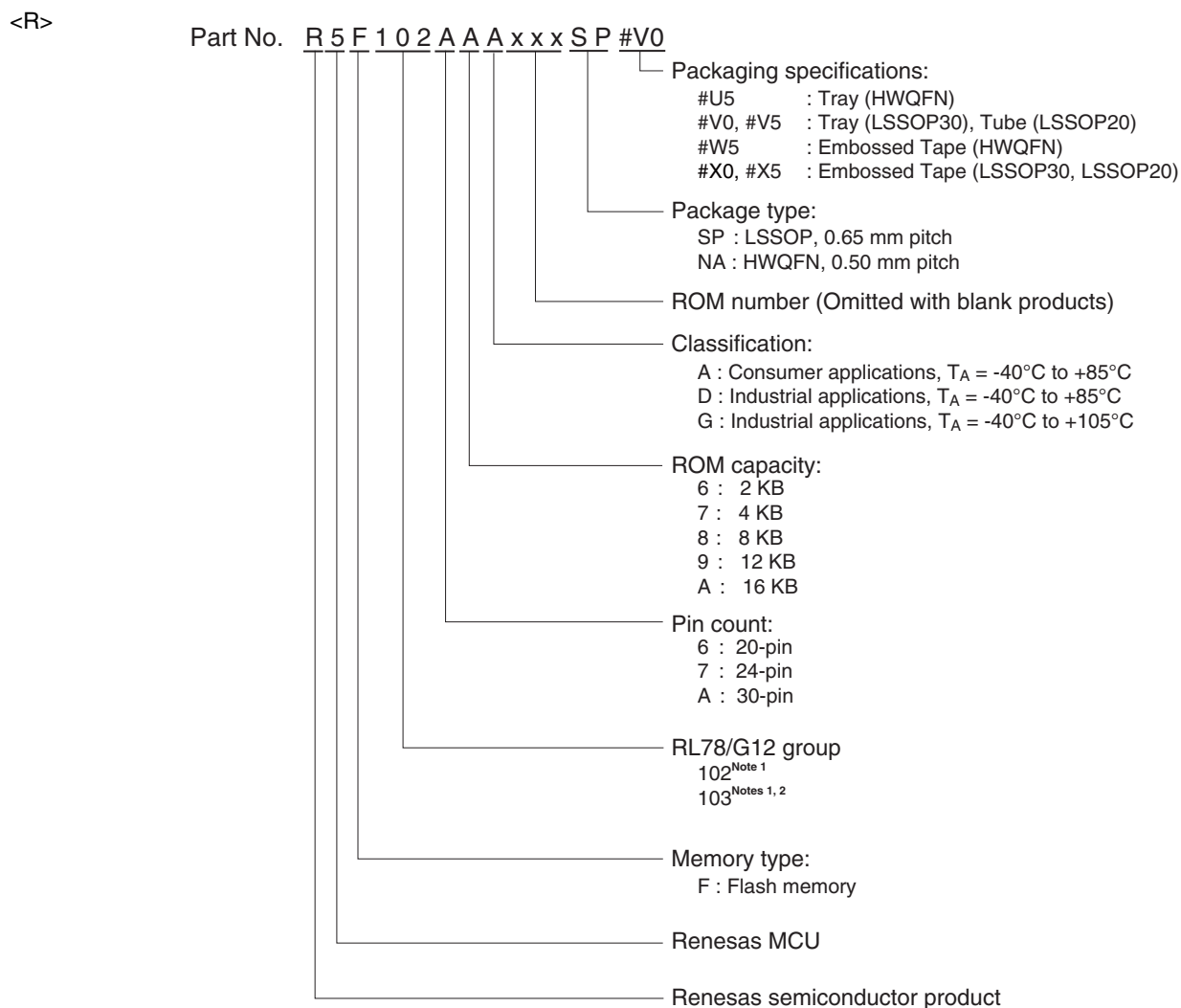
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10268asp-x5

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G12



- Notes**
1. For details about the differences between the R5F102 products and the R5F103 products of RL78/G12, see **1.1 Differences between the R5F102 Products and the R5F103 Products**.
 2. Products only for "A: Consumer applications ($T_A = -40$ to $+85^{\circ}\text{C}$)" and "D: Industrial applications ($T_A = -40$ to $+85^{\circ}\text{C}$)"

(2/2)

Item		20-pin		24-pin		30-pin	
		R5F1026x	R5F1036x	R5F1027x	R5F1037x	R5F102Ax	R5F103Ax
Clock output/buzzer output		1				2	
		2.44 kHz to 10 MHz: (Peripheral hardware clock: f _{MAIN} = 20 MHz operation)					
8/10-bit resolution A/D converter		11 channels				8 channels	
Serial interface		[R5F1026x (20-pin), R5F1027x (24-pin)]					
		• CSI: 2 channels/Simplified I ² C: 2 channels/UART: 1 channel					
		[R5F102Ax (30-pin)]					
		• CSI: 1 channel/Simplified I ² C: 1 channel/UART: 1 channel					
		• CSI: 1 channel/Simplified I ² C: 1 channel/UART: 1 channel					
		• CSI: 1 channel/Simplified I ² C: 1 channel/UART: 1 channel					
		[R5F1036x (20-pin), R5F1037x (24-pin)]					
		• CSI: 1 channel/Simplified I ² C: 0 channel/UART: 1 channel					
		[R5F103Ax (30-pin)]					
		• CSI: 1 channel/Simplified I ² C: 0 channel/UART: 1 channel					
		I ² C bus		1 channel			
		Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (unsigned or signed) • 32 bits × 32 bits = 32 bits (unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (unsigned or signed)			
DMA controller		2 channels	—	2 channels	—	2 channels	—
Vectored interrupt sources	Internal	18	16	18	16	26	19
	External	5				6	
Key interrupt		6		10		—	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access					
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP) • Power-down-reset: 1.50 V (TYP)					
Voltage detector		• Rising edge : 1.88 to 4.06 V (12 stages) • Falling edge : 1.84 to 3.98 V (12 stages)					
On-chip debug function		Provided					
Power supply voltage		V _{DD} = 1.8 to 5.5 V					
Operating ambient temperature		T _A = −40 to +85°C (A: Consumer applications, D: Industrial applications), T _A = −40 to +105°C (G: Industrial applications)					

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

<R> 2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$)

<R> This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A = -40$ to $+85^\circ\text{C}$

<R> R5F102xxAxx, R5F103xxAxx

D: Industrial applications $T_A = -40$ to $+85^\circ\text{C}$

<R> R5F102xxDxx, R5F103xxDxx

G: Industrial applications when $T_A = -40$ to $+105^\circ\text{C}$ products is used in the range of $T_A = -40$ to $+85^\circ\text{C}$

<R> R5F102xxGxx

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			-0.5 to $+6.5$	V
REGC terminal input voltage ^{Note 1}	V_{IREGC}	REGC		-0.3 to $+2.8$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Input Voltage	V_{I1}	Other than P60, P61		-0.3 to $V_{DD} + 0.3$ ^{Note 3}	V
	V_{I2}	P60, P61 (N-ch open drain)		-0.3 to 6.5	V
Output Voltage	V_O			-0.3 to $V_{DD} + 0.3$ ^{Note 3}	V
Analog input voltage	V_{AI}	20-, 24-pin products: ANI0 to ANI3, ANI16 to ANI22 30-pin products: ANI0 to ANI3, ANI16 to ANI19		-0.3 to $V_{DD} + 0.3$ and -0.3 to $AVREF(+)+0.3$ ^{Notes 3, 4}	V
Output current, high	I_{OH1}	Per pin	Other than P20 to P23	-40	mA
		Total of all pins	All the terminals other than P20 to P23	-170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	-70	mA
			20-, 24-pin products: P00 to P03 ^{Note 5} , P10 to P14 30-pin products: P10 to P17, P30, P31, P50, P51, P147	-100	mA
	I_{OH2}	Per pin	P20 to P23	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I_{OL1}	Per pin	Other than P20 to P23	40	mA
		Total of all pins	All the terminals other than P20 to P23	170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	70	mA
			20-, 24-pin products: P00 to P03 ^{Note 5} , P10 to P14, P60, P61 30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147	100	mA
	I_{OL2}	Per pin	P20 to P23	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A			-40 to $+85$	$^\circ\text{C}$
Storage temperature	T_{stg}			-65 to $+150$	$^\circ\text{C}$

Notes 1. 30-pin product only.

2. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.
3. Must be 6.5 V or lower.
4. Do not exceed $AVREF(+) + 0.3$ V in case of A/D conversion target pin.
5. 24-pin products only.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks** 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
2. $AVREF(+)$: + side reference voltage of the A/D converter.
 3. V_{SS} : Reference voltage

(3) Peripheral functions (Common to all products)**(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed onchip oscillator operating current	I _{FIL} ^{Note 1}				0.20		μA
12-bit interval timer operating current	I _{TMKA} ^{Notes 1, 2, 3}				0.02		μA
Watchdog timer operating current	I _{WDT} ^{Notes 1, 2, 4}	f _{IL} = 15 kHz			0.22		μA
A/D converter operating current	I _{ADC} ^{Notes 1, 5}	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.30	1.70	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.50	0.70	mA
A/D converter reference voltage operating current	I _{ADREF} ^{Note 1}				75.0		μA
Temperature sensor operating current	I _{TMPS} ^{Note 1}				75.0		μA
LVD operating current	I _{LVD} ^{Notes 1, 6}				0.08		μA
Self-programming operating current	I _{FSP} ^{Notes 1, 8}				2.00	12.20	mA
BGO operating current	I _{BGO} ^{Notes 1, 7}				2.00	12.20	mA
SNOOZE operating current	I _{SNOZ} ^{Note 1}	ADC operation	The mode is performed ^{Note 9}		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to the V_{DD}.

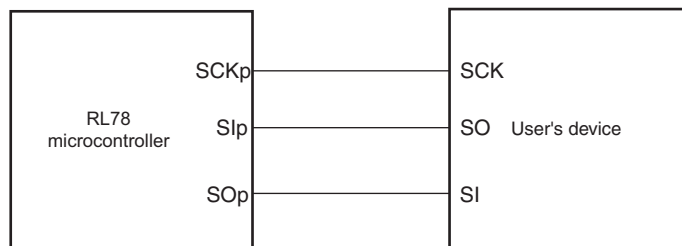
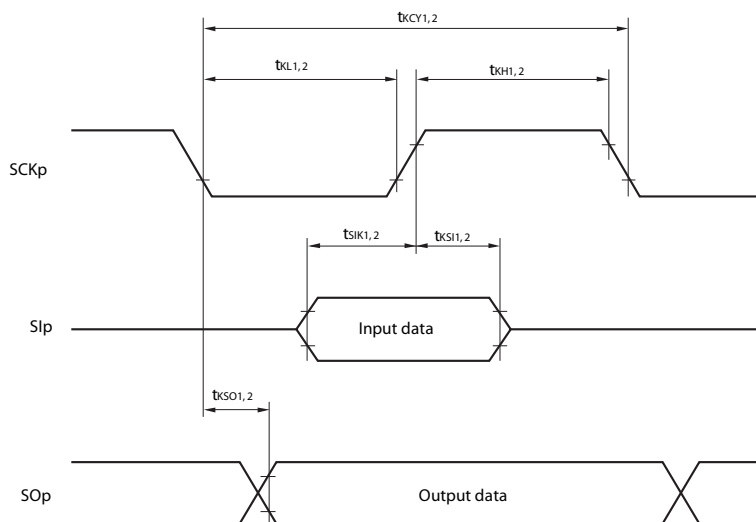
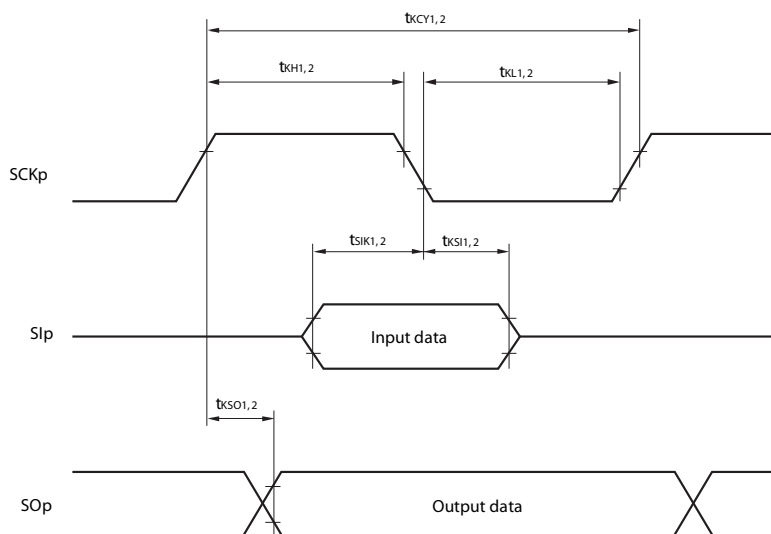
2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{FIL} and I_{TMKA} when the 12-bit interval timer operates.4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.6. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.

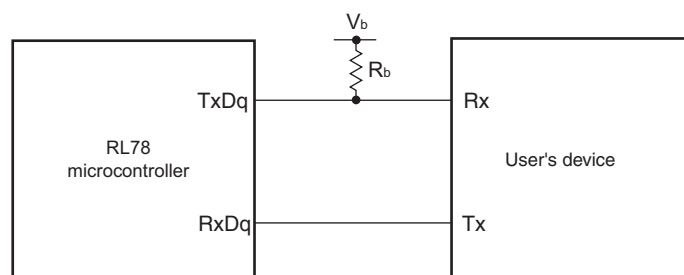
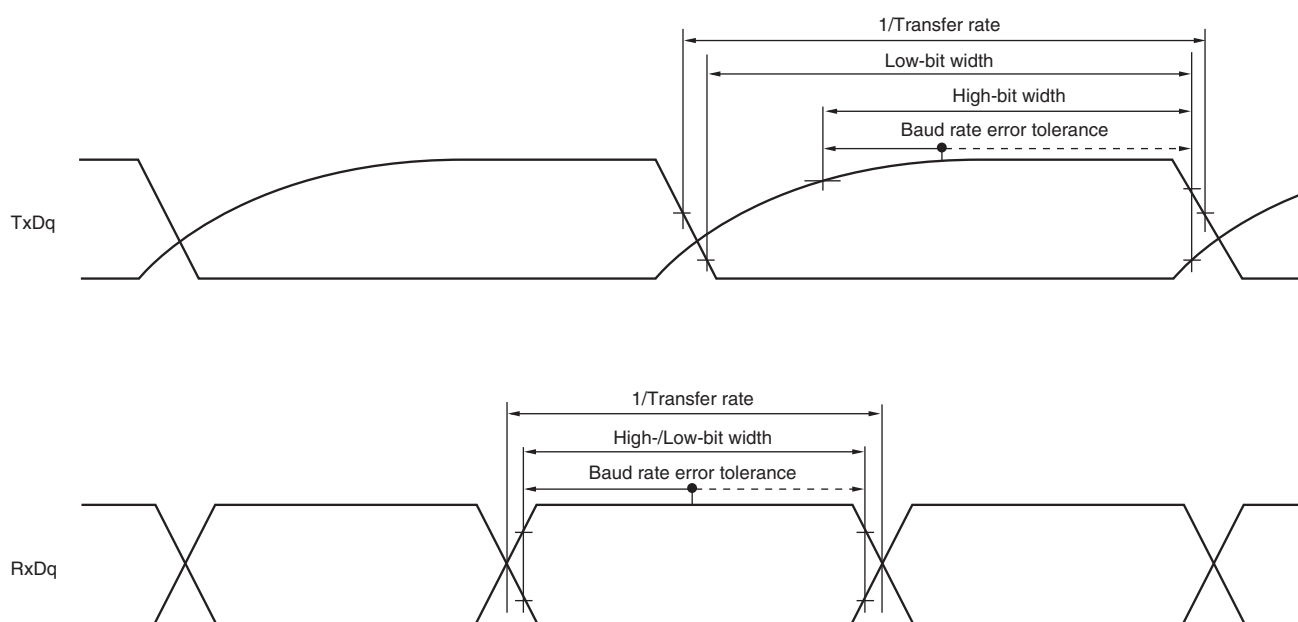
7. Current flowing only during data flash rewrite.

8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.**Remarks** 1. f_{IL}: Low-speed on-chip oscillator clock frequency2. Temperature condition of the TYP. value is T_A = 25°C

CSI mode connection diagram (during communication at same potential)**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)****CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**

(Remarks are listed on the next page.)

UART mode connection diagram (during communication at different potential)**UART mode bit width (during communication at different potential) (reference)**

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[\text{F}]$: Communication line (TxDq) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. q: UART number ($q = 0$ to 2), g: PIM and POM number ($g = 0, 1$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00$ to $03, 10, 11$))
 4. UART0 of the 20- and 24-pin products supports communication at different potential only when the peripheral I/O redirection function is not used.

- Notes**
1. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1
 2. When DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

Caution Select the TTL input buffer for the SI00 pin and the N-ch open drain output (V_{DD} tolerance) mode for the SO00 pin and SCK00 pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).
For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
1. R_b [Ω]: Communication line (SCK00, SO00) pull-up resistance, C_b [F]: Communication line (SCK00, SO00) load capacitance, V_b [V]: Communication line voltage
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS00 bit of serial mode register 00 (SMR00).)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	300		1150		ns
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	500		1150		ns
			$1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note}}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	1150		1150		ns
SCKp high-level width	t_{KH1}		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{KCY1}/2 - 75$		$t_{KCY1}/2 - 75$		ns
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{KCY1}/2 - 170$		$t_{KCY1}/2 - 170$		ns
			$1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note}}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$t_{KCY1}/2 - 458$		$t_{KCY1}/2 - 458$		ns
SCKp low-level width	t_{KL1}		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{KCY1}/2 - 12$		$t_{KCY1}/2 - 50$		ns
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{KCY1}/2 - 18$		$t_{KCY1}/2 - 50$		ns
			$1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note}}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns

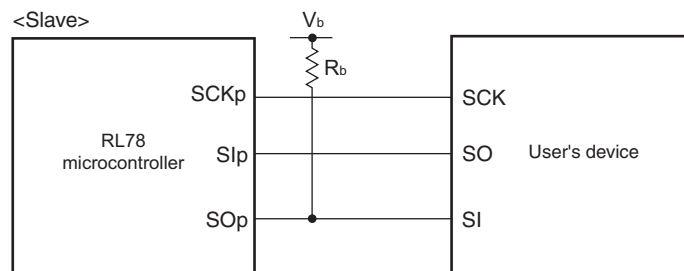
Note Use it with $V_{DD} \geq V_b$.

Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

2. CSI01 and CSI11 cannot communicate at different potential.

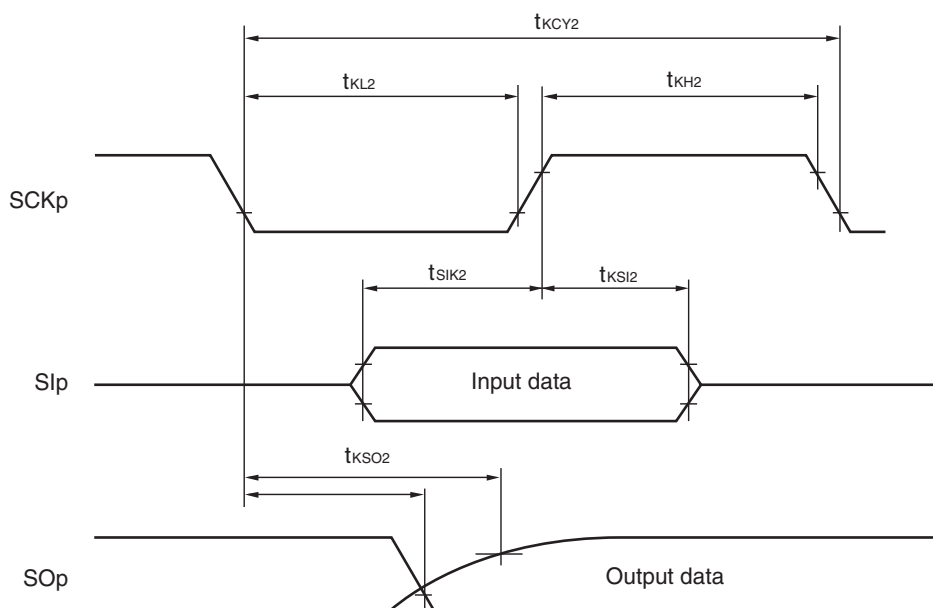
Remarks 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSI number (p = 00, 20)

CSI mode connection diagram (during communication at different potential)

- Remarks**
1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage
 2. p: CSI number ($p = 00, 20$), m: Unit number ($m = 0, 1$), n: Channel number ($n = 0$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number ($mn = 00, 10$))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



2.5.2 Serial interface IICA

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) mode LS (low-speed main) mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz			0	400	kHz
		Normal mode: f _{CLK} ≥ 1 MHz	0	100			kHz
Setup time of restart condition	t _{SU:STA}		4.7		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}		4.0		0.6		μs
Hold time when SCLA0 = “L”	t _{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t _{HIGH}		4.0		0.6		μs
Data setup time (reception)	t _{SU:DAT}		250		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		0	3.45	0	0.9	μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		μs
Bus-free time	t _{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

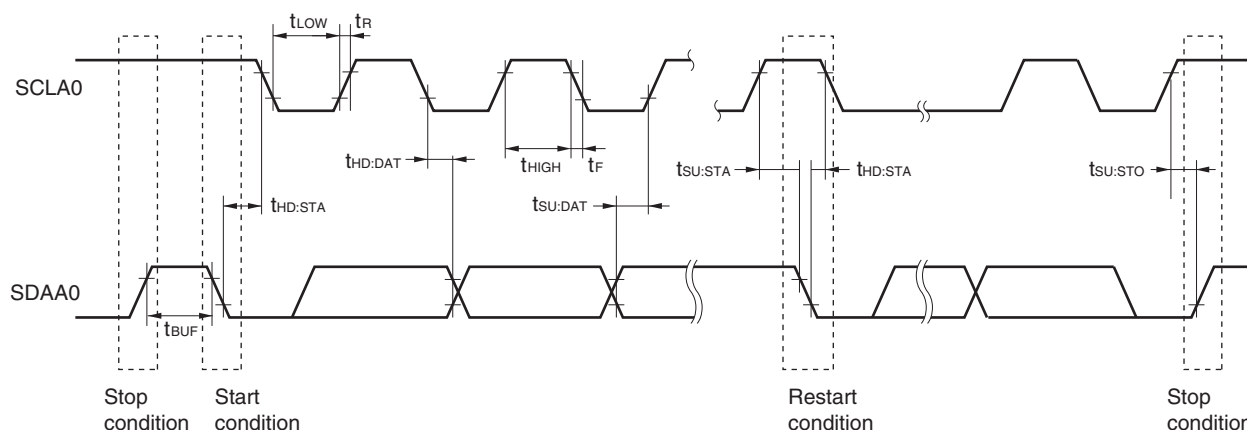
Caution Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1} , I_{OL1} , V_{OH1} , V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: $C_b = 400\text{ pF}$, $R_b = 2.7\text{ k}\Omega$

Fast mode: $C_b = 320\text{ pF}$, $R_b = 1.1\text{ k}\Omega$

IICA serial transfer timing



(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution		1.2	± 7.0	LSB
				1.2	± 10.5 ^{Note 3}	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
				57	95	μs
Conversion time	t_{CONV}	10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error ^{Notes 1, 2}	EZX	10-bit resolution			± 0.60	%FSR
					± 0.85 ^{Note 3}	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution			± 0.60	%FSR
					± 0.85 ^{Note 3}	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution			± 4.0	LSB
					± 6.5 ^{Note 3}	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution			± 2.0	LSB
					± 2.5 ^{Note 3}	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI3, ANI16 to ANI22	0		V_{DD}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)	V_{BGR} ^{Note 4}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)	V_{TSPS25} ^{Note 4}			V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

2.9 Dedicated Flash Memory Programmer Communication (UART)

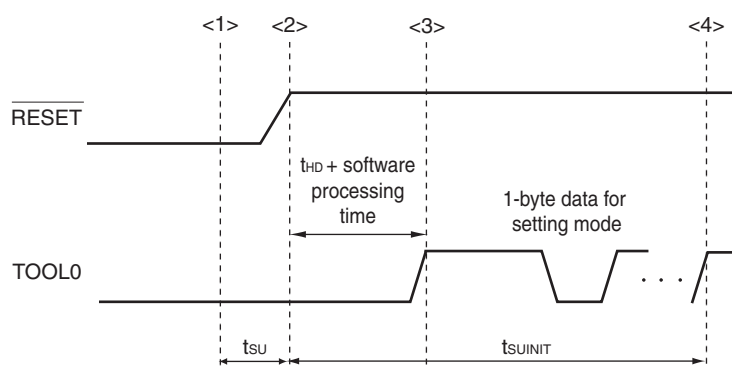
($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUNIT}	POR and LVD reset are released before external reset release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset are released before external reset release	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset are released before external reset release	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUNIT} : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

3.2 Oscillator Characteristics

3.2.1 X1 oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_x) ^{Note}	Ceramic resonator / crystal oscillator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		8.0	

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **5.4 System Clock Oscillator**.

3.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

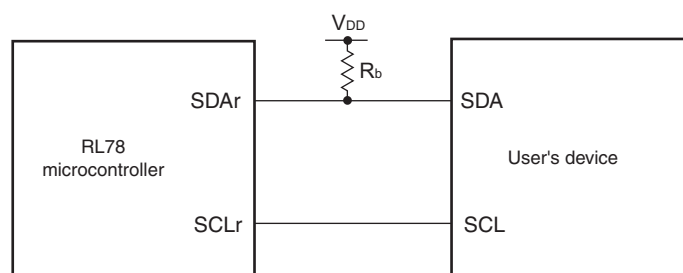
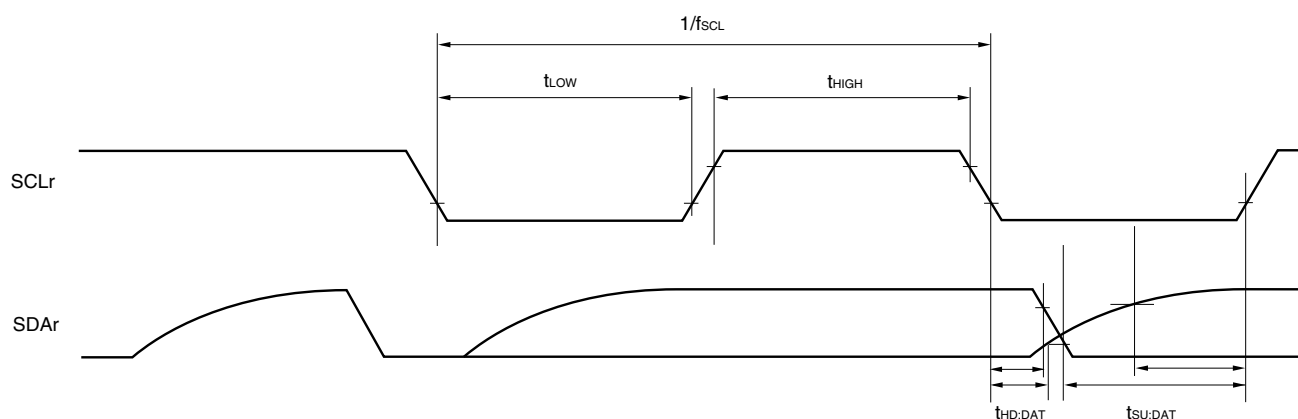
Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		R5F102 products	$T_A = -20$ to $+85^\circ\text{C}$	-1.0		+1.0	%
			$T_A = -40$ to -20°C	-1.5		+1.5	%
			$T_A = +85$ to $+105^\circ\text{C}$	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

(4) During communication at same potential (simplified I²C mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	$C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$		100 ^{Note 1}	kHz
Hold time when SCLr = "L"	t_{LOW}	$C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	$C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Data setup time (reception)	$t_{\text{SU:DAT}}$	$C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 580$ ^{Note 2}		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	0	1420	ns

Notes 1. The value must also be equal to or less than $f_{\text{MCK}}/4$.**2.** Set $t_{\text{SU:DAT}}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".**Caution** Select the N-ch open drain output (V_{DD} tolerance) mode for SDAr by using port output mode register h (POMh).**Simplified I²C mode connection diagram (during communication at same potential)****Simplified I²C mode serial transfer timing (during communication at same potential)****Remarks 1.** R_b [Ω]: Communication line (SDAr) pull-up resistance C_b [F]: Communication line (SCLr, SDAr) load capacitance**2.** r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1, 4, 5)**3.** f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number (m = 0, 1), n: Channel number (0, 1, 3))

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.
5. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.
7. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

8. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 7** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). **For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp \uparrow) <small>Note</small>	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	162		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	354		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	958		ns
Slp hold time (from SCKp \uparrow) <small>Note</small>	t_{KSI1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp \downarrow to SOp output <small>Note</small>	t_{KSO1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		200	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		390	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		966	ns

Note When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$.

(Cautions and Remarks are listed on the next page.)

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM} (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{BGR} ^{Note 3}, Reference voltage (–) = AV_{REFM}
^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8			bit
Conversion time	t_{CONV}	8-bit resolution	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	8-bit resolution			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution			± 2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution			± 1.0	LSB
Analog input voltage	V_{AIN}		0		V_{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (–) = AV_{REFM} .

Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

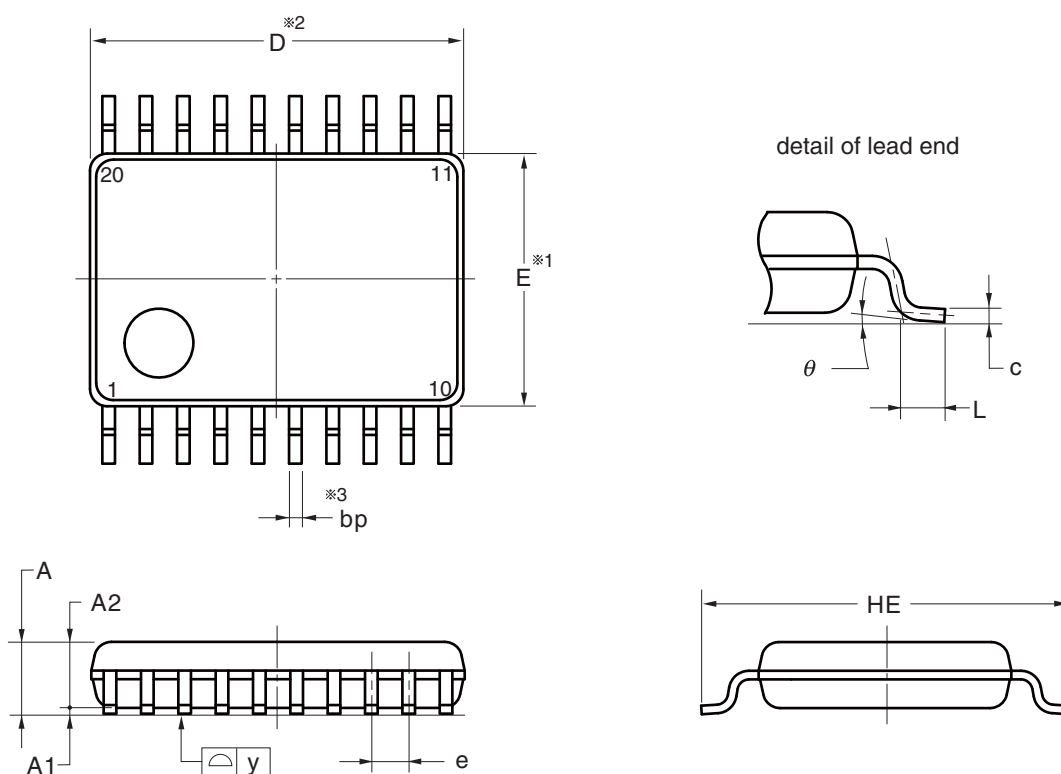
4. PACKAGE DRAWINGS

4.1 20-pin products

R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP
 R5F1036AASP, R5F10369ASP, R5F10368ASP, R5F10367ASP, R5F10366ASP
 R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP
 R5F1036ADSP, R5F10369DSP, R5F10368DSP, R5F10367DSP, R5F10366DSP
 R5F1026AGSP, R5F10269GSP, R5F10268GSP, R5F10267GSP, R5F10266GSP

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1



NOTE

1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include trim offset.

(UNIT:mm)

ITEM	DIMENSIONS
D	6.50±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.45 MAX.
A1	0.10±0.10
A2	1.15
e	0.65±0.12
bp	0.22 ^{+0.10} _{-0.05}
c	0.15 ^{+0.05} _{-0.02}
L	0.50±0.20
y	0.10
θ	0° to 10°

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Revision History	RL78/G12 Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Dec 10, 2012	-	First Edition issued
2.00	Sep 06, 2013	1	Modification of 1.1 Features
		3	Modification of 1.2 List of Part Numbers
		4	Modification of Table 1-1. List of Ordering Part Numbers, Note, and Caution
		7 to 9	Modification of package name in 1.4.1 to 1.4.3
		14	Modification of tables in 1.7 Outline of Functions
		17	Modification of description of table in 2.1 Absolute Maximum Ratings (TA = 25°C)
		18	Modification of table, Note, and Caution in 2.2.1 X1 oscillator characteristics
		18	Modification of table in 2.2.2 On-chip oscillator characteristics
		19	Modification of Note 3 in 2.3.1 Pin characteristics (1/4)
		20	Modification of Note 3 in 2.3.1 Pin characteristics (2/4)
		23	Modification of Notes 1 and 2 in (1) 20-, 24-pin products (1/2)
		24	Modification of Notes 1 and 3 in (1) 20-, 24-pin products (2/2)
		25	Modification of Notes 1 and 2 in (2) 30-pin products (1/2)
		26	Modification of Notes 1 and 3 in (2) 30-pin products (2/2)
		27	Modification of (3) Peripheral functions (Common to all products)
		28	Modification of table in 2.4 AC Characteristics
		29	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		30	Modification of figures of AC Timing Test Point and External Main System Clock Timing
		31	Modification of figure of AC Timing Test Point
		31	Modification of description and Note 2 in (1) During communication at same potential (UART mode)
		32	Modification of description in (2) During communication at same potential (CSI mode)
		33	Modification of description in (3) During communication at same potential (CSI mode)
		34	Modification of description in (4) During communication at same potential (CSI mode)
		36	Modification of table and Note 2 in (5) During communication at same potential (simplified I ² C mode)
		38, 39	Modification of table and Notes 1 to 9 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)
		40	Modification of Remarks 1 to 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)
		41	Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode)
		42	Modification of Caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode)
		43	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		44	Modification of table and Notes 1 and 2 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		45	Modification of table, Note 1, and Caution 1 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		47	Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode)
		50	Modification of table, Note 1, and Caution 1 in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode)
		52	Modification of Remark in 2.5.2 Serial interface IICA
		53	Addition of table to 2.6.1 A/D converter characteristics
		53	Modification of description in 2.6.1 (1)
		54	Modification of Notes 3 to 5 in 2.6.1 (1)
		54	Modification of description and Notes 2 to 4 in 2.6.1 (2)