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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10268gsp-v5

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 1-1.	List of	Ordering	Part	Numbers
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	Pin count	Package	Data flash	Fields of Application	Part Number
<r></r>	20 pins	20-pin plastic LSSOP $(4.4 \times 6.5 \text{ mm}, 0.65 \text{ mm pitch})$	Mounted	A	R5F1026AASP#V5, R5F10269ASP#V5, R5F10268ASP#V5, R5F10267ASP#V5, R5F10266ASP#V5 R5F1026AASP#X5, R5F10269ASP#X5, R5F10268ASP#X5, R5F10267ASP#X5, R5F10266ASP#X5
				D	R5F1026ADSP#V5, R5F10269DSP#V5, R5F10268DSP#V5, R5F10267DSP#V5, R5F10266DSP#V5 R5F1026ADSP#X5, R5F10269DSP#X5, R5F10268DSP#X5, R5F10267DSP#X5, R5F10266DSP#X5
				G	R5F1026AGSP#V5, R5F10269GSP#V5, R5F10268GSP#V5, R5F10267GSP#V5, R5F10266GSP#V5 R5F1026AGSP#X5, R5F10269GSP#X5, R5F10268GSP#X5, R5F10267GSP#X5, R5F10266GSP#X5
			Not mounted	A	R5F1036AASP#V5, R5F10369ASP#V5, R5F10368ASP#V5, R5F10367ASP#V5, R5F10366ASP#V5 R5F1036AASP#X5, R5F10369ASP#X5, R5F10368ASP#X5, R5F10367ASP#X5, R5F10366ASP#X5
				D	R5F1036ADSP#V5, R5F10369DSP#V5, R5F10368DSP#V5, R5F10367DSP#V5, R5F10366DSP#V5 R5F1036ADSP#X5, R5F10369DSP#X5, R5F10368DSP#X5, R5F10367DSP#X5, R5F10366DSP#X5
<r></r>	24 pins	24-pin plastic HWQFN $(4 \times 4 \text{ mm}, 0.5)$	Mounted	A	R5F1027AANA#U5, R5F10279ANA#U5, R5F10278ANA#U5, R5F10277ANA#U5 R5F1027AANA#W5, R5F10279ANA#W5, R5F10278ANA#W5, R5F10277ANA#W5
		mm pitch)		D	R5F1027ADNA#U5, R5F10279DNA#U5, R5F10278DNA#U5, R5F10277DNA#U5 R5F1027ADNA#W5, R5F10279DNA#W5, R5F10278DNA#W5, R5F10277DNA#W5
				G	R5F1027AGNA#U5, R5F10279GNA#U5, R5F10278GNA#U5, R5F10277GNA#U5 R5F1027AGNA#W5, R5F10279GNA#W5, R5F10278GNA#W5, R5F10277GNA#W5
			Not mounted	А	R5F1037AANA#V5, R5F10379ANA#V5, R5F10378ANA#V5, R5F10377ANA#V5
					R5F1037AANA#X5, R5F10379ANA#X5, R5F10378ANA#X5, R5F10377ANA#X5
				D	R5F1037ADNA#V5, R5F10379DNA#V5, R5F10378DNA#V5, R5F10377DNA#V5 R5F1037ADNA#X5, R5F10379DNA#X5, R5F10378DNA#X5, R5F10377DNA#X5
	30 pins	30-pin plastic LSSOP	Mounted	A	R5F102AAASP#V0, R5F102A9ASP#V0, R5F102A8ASP#V0, R5F102A7ASP#V0 R5F102AAASP#X0, R5F102A9ASP#X0, R5F102A8ASP#X0, R5F102A7ASP#X0
		(7.62 mm (300), 0.65 mm		D	R5F102AADSP#V0, R5F102A9DSP#V0, R5F102A8DSP#V0, R5F102A7DSP#V0 R5F102AADSP#X0, R5F102A9DSP#X0, R5F102A8DSP#X0, R5F102A7DSP#X0
		pitch)		G	R5F102AAGSP#V0, R5F102A9GSP#V0, R5F102A8GSP#V0, R5F102A7GSP#V0 R5F102AAGSP#X0, R5F102A9GSP#X0, R5F102A8GSP#X0, R5F102A7GSP#X0
			Not mounted	A	R5F103AAASP#V0, R5F103A9ASP#V0, R5F103A8ASP#V0, R5F103A7ASP#V0 R5F103AAASP#X0, R5F103A9ASP#X0, R5F103A8ASP#X0, R5F103A7ASP#X0
				D	R5F103AADSP#V0, R5F103A9DSP#V0, R5F103A8DSP#V0, R5F103A7DSP#V0 R5F103AADSP#X0, R5F103A9DSP#X0, R5F103A8DSP#X0, R5F103A7DSP#X0

Note For fields of application, see Figure 1-1 Part Number, Memory Size, and Package of RL78/G12.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.



1.4.2 24-pin products

<R> • 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)



Note Provided only in the R5F102 products.

Remarks 1. For pin identification, see 1.5 Pin Identification.

- 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR).
- 3. It is recommended to connect an exposed die pad to Vss.



1.6.3 30-pin products





Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR).



2.2 Oscillator Characteristics

2.2.1 X1 oscillator characteristics

$(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{V}_{DD} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{ V}_{SS} = 0 \text{ V})$

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation	Ceramic resonator /	$2.7~V \leq V_{\text{DD}} \leq 5.5~V$	1.0		20.0	MHz
frequency (fx) ^{Note}	crystal oscillator	$1.8~V \leq V_{\text{DD}} < 2.7~V$	1.0		8.0	

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

- Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.
- **Remark** When using the X1 oscillator, refer to **5.4 System Clock Oscillator**.

2.2.2 On-chip oscillator characteristics

$(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{ V}_{SS} = 0 \text{ V})$

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	fін			1		24	MHz
High-speed on-chip oscillator		R5F102 products	$T_A = -20 \text{ to } +85^{\circ}\text{C}$	-1.0		+1.0	%
clock frequency accuracy			$T_A = -40$ to $-20^{\circ}C$	-1.5		+1.5	%
		R5F103 products		-5.0		+5.0	%
Low-speed on-chip oscillator clock frequency	fı∟				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.



(1/2)

2.3.2 Supply current characteristics

(1) 20-, 24-pin products

Parameter	Symbol			Conditions			MIN.	TYP.	MAX.	Unit
Supply		Operating	HS(High-speed	$f_{IH} = 24 \text{ MHz}^{Note 3}$	Basic	$V_{DD} = 5.0 V$		1.5		mA
current ^{Note 1}		mode	main) mode ^{™e₄}		operation	$V_{DD} = 3.0 V$		1.5		
					Normal	$V_{DD} = 5.0 \text{ V}$		3.3	5.0	mA
					operation	$V_{DD} = 3.0 V$		3.3	5.0	
				f⊩ = 16 MHz ^{Note 3}		$V_{DD} = 5.0 V$		2.5	3.7	mA
						$V_{DD} = 3.0 V$		2.5	3.7	
			LS(Low-speed	$f_{IH}=8\ MHz^{Note3}$		$V_{DD} = 3.0 V$		1.2	1.8	mA
			main) mode ^{™e₄}			$V_{DD} = 2.0 V$		1.2	1.8	
			HS(High-speed	$f_{MX} = 20 \text{ MHz}^{Note 2},$		Square wave input		2.8	4.4	mA
			main) mode ^{№te4}	$V_{DD} = 5.0 \text{ V}$		Resonator connection		3.0	4.6	
				$f_{MX} = 20 \text{ MHz}^{Note 2},$		Square wave input		2.8	4.4	mA
				$V_{DD} = 3.0 \text{ V}$		Resonator connection		3.0	4.6	
				$f_{MX} = 10 \text{ MHz}^{Note 2},$		Square wave input		1.8	2.6	mA
				$V_{DD} = 5.0 \text{ V}$		Resonator connection		1.8	2.6	
				$f_{MX} = 10 \text{ MHz}^{Note 2}$,		Square wave input		1.8	2.6	mA
				$V_{DD} = 3.0 \text{ V}$		Resonator connection		1.8	2.6	
			LS(Low-speed	$f_{MX} = 8 \text{ MHz}^{Note 2},$		Square wave input		1.1	1.7	mA
			main) mode ^{№te4}	V _{DD} = 3.0 V		Resonator connection		1.1	1.7	
				$f_{MX} = 8 \text{ MHz}^{Note 2},$		Square wave input		1.1	1.7	mA
				VDD = 2.0 V		Resonator connection		1.1	1.7	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

- 2. When high-speed on-chip oscillator clock is stopped.
- **3.** When high-speed system clock is stopped
- **4.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: $V_{DD} = 2.7 \text{ V}$ to 5.5 V @1 MHz to 24 MHz $V_{DD} = 2.4 \text{ V}$ to 5.5 V @1 MHz to 16 MHz

- LS(Low speed main) mode: $V_{DD} = 1.8 V$ to 5.5 V @1 MHz to 8 MHz
- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 - 2. fil: high-speed on-chip oscillator clock frequency
 - **3.** Temperature condition of the TYP. value is $T_A = 25^{\circ}C$.



(2) During communication at same potential (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)

Parameter	Symbol	Conditions HS (high-speed main) LS (low-speed mode Mode		d main) LS (low-spee Mode		Unit	
			MIN.	MAX.	MIN.	MAX.	
SCK00 cycle time	tkCY1	tĸcyı ≥ 2/fclĸ	83.3		250		ns
SCK00 high-/low-	tкнı,	$4.0~V \leq V_{\text{DD}} \leq 5.5~V$	tксү1/2–7		tксү1/2–50		ns
level width	tĸ∟1	$2.7~V \leq V_{\text{DD}} \leq 5.5~V$	tксү1/2–10		tксү1/2–50		ns
SI00 setup time	tsik1	$4.0~V \leq V_{\text{DD}} \leq 5.5~V$	23		110		ns
(to SCK00↑) ^{Note 1}		$2.7~V \leq V_{\text{DD}} \leq 5.5~V$	33		110		ns
SI00 hold time (from SCK00↑) ^{Note2}	tksii		10		10		ns
Delay time from SCK00↓ to SO00 output ^{Note 3}	tkso1	$C = 20 \text{ pF}^{Note 4}$		10		10	ns

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 2.7 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{V}_{SS} = 0 \text{ V})$

- **Notes 1.** When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 setup time becomes "to $SCK00\downarrow$ " when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.
 - 2. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 hold time becomes "from SCK00↓" when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.
 - **3.** When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The delay time to SO00 output becomes "from SCK00∱" when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.
 - 4. C is the load capacitance of the SCK00 and SO00 output lines.
- **Caution** Select the normal input buffer for the SI00 pin and the normal output mode for the SO00 and SCK00 pins by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).
- Remarks 1. This specification is valid only when CSI00's peripheral I/O redirect function is not used.
 - 2. fMCK: Serial array unit operation clock frequency
 - (Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS00 bit of serial mode register 00 (SMR00).)





CSI mode connection diagram (during communication at same potential)





CSI mode serial transfer timing (during communication at same potential) (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



(Remarks are listed on the next page.)



- 5. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.
- 6. The smaller maximum transfer rate derived by using fMCK/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V \leq V_DD < 4.0 V and 2.3 V \leq V_b \leq 2.7 V

Maximum transfer rate =
$$\frac{1}{\{-Cb \times Rb \times ln (1 - \frac{2.0}{Vb})\} \times 3}$$
 [bps]

Baud rate error (theoretical value) =

 $\begin{array}{c} \displaystyle \frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{2.0}{V_b})\} \\ \hline \\ \displaystyle (\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits} \end{array} \times 100 \ [\%]$ * This value is the theoretical value of the relative difference between the transmission and reception sides.

- 7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.
- 8. The smaller maximum transfer rate derived by using fMCK/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V \leq V_DD < 3.3 V, 1.6 V \leq V_b \leq 2.0 V

Maximum transfer rate =
$$\frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\} \times 3}$$
 [bps]

Baud rate error (theoretical value) =

$$\frac{1}{\text{ransfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\}$$

$$\frac{1}{(1 - \frac{1.5}{V_b})} \times 100 \,[\%]$$
Transfer rate

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- 9. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 8 above to calculate the maximum transfer rate under conditions of the customer.
- Caution Select the TTL input buffer for the RxDg pin and the N-ch open drain output (VDD tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and V_{IL}, see the DC characteristics with TTL input buffer selected.



(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

Parameter	Symbol		Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t ксү1	$t_{KCY1} \geq 4/f_{CLK}$	$4.0~V \leq V_{\text{DD}} \leq 5.5~V,$	300		1150		ns
			$2.7~V \leq V_b \leq 4.0~V,$					
			C_b = 30 pF, R_b = 1.4 k Ω					
			$2.7~V \leq V_{\text{DD}} < 4.0~V,$	500		1150		ns
			$2.3~V \leq V_b \leq 2.7~V,$					
			C_b = 30 pF, R_b = 2.7 k Ω					
			$1.8~V \leq V_{\text{DD}} < 3.3~V,$	1150		1150		ns
			$1.6~V \leq V_{b} \leq 2.0~V^{\text{ Note}},$					
			C_b = 30 pF, R_b = 5.5 k Ω					
SCKp high-level width	tкнı	$4.0~V \leq V_{\text{DD}} \leq$	5.5 V, 2.7 V \leq V _b \leq 4.0 V,	tксү1/2-75		tксү1/2-75		ns
		$C_b = 30 \text{ pF}, \text{ F}$	lb = 1.4 kΩ					
		$2.7 \text{ V} \leq \text{V}_{\text{DD}}$ <	$4.0~V,~2.3~V \le V_b \le 2.7~V,~$	tксү1/2 –170		tксү1/2–170		ns
		$C_b = 30 \text{ pF}, \text{ R}$	$h_b = 2.7 \text{ k}\Omega$					
		$1.8 \text{ V} \leq \text{V}_{\text{DD}} <$	3.3 V, 1.6 V \leq V $_{b}$ \leq 2.0 V $^{\text{Note}},$	tксү1/2 –458		tксү1/2-458		ns
		$C_b = 30 \text{ pF}, \text{ F}$	$h_b = 5.5 \text{ k}\Omega$					
SCKp low-level width	tĸ∟1	$4.0~V \leq V_{\text{DD}} \leq$	$5.5~V,~2.7~V \le V_b \le 4.0~V,$	tксү1/2-12		tксү1/2–50		ns
		$C_{b} = 30 \text{ pF}, \text{ R}$	lb = 1.4 kΩ					
		$2.7 \text{ V} \leq \text{V}_{\text{DD}}$ <	$4.0~V,~2.3~V \le V_b \le 2.7~V,~$	tксү1/2 –18		tксү1/2–50		ns
		C _b = 30 pF, R	$h_b = 2.7 \text{ k}\Omega$					
		$1.8 \text{ V} \leq \text{V}_{\text{DD}} <$	$3.3 \text{ V}, \ 1.6 \text{ V} \le \text{V}_{b} \le 2.0 \text{ V}^{\text{Note}},$	tксү1/2 –50		tксү1/2–50		ns
		C _b = 30 pF, R	$h_b = 5.5 \text{ k}\Omega$					

 $(T_A = -40 \text{ to } +85^{\circ}C, 1.8 \text{ V} \le \text{V}_{DD} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{ V}_{SS} = 0 \text{ V})$

 $\label{eq:Note} \textbf{Note} \quad \textbf{Use it with } V_{\text{DD}} \geq V_{\text{b}}.$

- Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.
 - 2. CSI01 and CSI11 cannot communicate at different potential.
- **Remarks 1.** R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage
 - **2.** p: CSI number (p = 00, 20)





CSI mode serial transfer timing (master mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)







2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode (TA = -40 to $+85^{\circ}$ C, VPDR \leq VDD \leq 5.5 V, Vss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	VLVD0	Power supply rise time	3.98	4.06	4.14	V
		Power supply fall time	3.90	3.98	4.06	V
	VLVD1	Power supply rise time	3.68	3.75	3.82	V
		Power supply fall time	3.60	3.67	3.74	V
	VLVD2	Power supply rise time	3.07	3.13	3.19	V
		Power supply fall time	3.00	3.06	3.12	V
	VLVD3	Power supply rise time	2.96	3.02	3.08	V
		Power supply fall time	2.90	2.96	3.02	V
	VLVD4	Power supply rise time	2.86	2.92	2.97	V
		Power supply fall time	2.80	2.86	2.91	V
	VLVD5	Power supply rise time	2.76	2.81	2.87	V
		Power supply fall time	2.70	2.75	2.81	V
	VLVD6	Power supply rise time	2.66	2.71	2.76	V
		Power supply fall time	2.60	2.65	2.70	V
	VLVD7	Power supply rise time	2.56	2.61	2.66	V
		Power supply fall time	2.50	2.55	2.60	V
	VLVD8	Power supply rise time	2.45	2.50	2.55	V
		Power supply fall time	2.40	2.45	2.50	V
	VLVD9	Power supply rise time	2.05	2.09	2.13	V
		Power supply fall time	2.00	2.04	2.08	V
	VLVD10	Power supply rise time	1.94	1.98	2.02	v
		Power supply fall time	1.90	1.94	1.98	V
	VLVD11	Power supply rise time	1.84	1.88	1.91	v
		Power supply fall time	1.80	1.84	1.87	V
Minimum pulse width	t∟w		300			μS
Detection delay time					300	μs



<R> 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

$(T_A = -40 \text{ to } +85^{\circ}\text{C}, \text{Vss} = 0 \text{ V})$						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 Note		5.5	V

<R> Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



2.8 Flash Memory Programming Characteristics

$(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{DD}$
--

<r></r>	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	System clock frequency	fclk		1		24	MHz
Coo Notes Dat	Code flash memory rewritable times	Cerwr	Retained for 20 years	1,000			Times
	Notes 1, 2, 3		$T_A = 85^{\circ}C$				
	Data flash memory rewritable times Notes 1, 2, 3		Retained for 1 year		1,000,000		
			T _A = 25°C				
			Retained for 5 years	100,000			
			T _A = 85°C				
			Retained for 20 years	10,000			
			T _A = 85°C				

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

- 2. When using flash memory programmer and Renesas Electronics self programming library
- 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.



3.2 Oscillator Characteristics

3.2.1 X1 oscillator characteristics

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{V}_{DD} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{V}_{SS} = 0 \text{ V})$

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation	Ceramic resonator / 2	$2.7~V \leq V_{\text{DD}} \leq 5.5~V$	1.0		20.0	MHz
frequency (fx) ^{Note}	crystal oscillator	$2.4~V \leq V_{\text{DD}} < 2.7~V$	1.0		8.0	

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

- **Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.
- Remark When using the X1 oscillator, refer to 5.4 System Clock Oscillator.

3.2.2 On-chip oscillator characteristics

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{V}_{SS} = 0 \text{ V})$

Oscillators	Parameters	Cond	litions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	fiн			1		24	MHz
High-speed on-chip oscillator		R5F102 products	T _A = -20 to +85°C	-1.0		+1.0	%
clock frequency accuracy			$T_A = -40$ to $-20^{\circ}C$	-1.5		+1.5	%
			T _A = +85 to +105°C	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	fı∟				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.



Parameter	Symbol	Condition	s	MIN.	TYP.	MAX.	Unit
Input voltage, high	VIH1	Normal input buffer		0.8Vdd		Vdd	V
		20-, 24-pin products: P00 to P0 P40 to P42	03 ^{Note 2} , P10 to P14,				
		30-pin products: P00, P01, P1 P40, P50, P51, P120, P147	0 to P17, P30, P31,				
	VIH2	TTL input buffer	$4.0~V \leq V_{\text{DD}} \leq 5.5~V$	2.2		VDD	v
		20-, 24-pin products: P10, P11	$3.3~V \leq V_{\text{DD}} < 4.0~V$	2.0		VDD	V
		30-pin products: P01, P10, P11, P13 to P17	$2.4~V \leq V_{\text{DD}} < 3.3~V$	1.5		Vdd	V
	VIH3	Normal input buffer		0.7Vdd		Vdd	V
	Villa	P60 P61		0.71/00		6.0	V
	VINE	P121 P122 P125 ^{Note 1} P137 F	0.81/pp		Voo	V	
Input voltage low	Vii 1	Normal input buffer		0.0100		0 2Vpp	v
		20-, 24-pin products: P00 to P03 ^{Note 2} , P10 to P14, P40 to P42					
		30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147					
	VIL2	TTL input buffer	$4.0~V \leq V_{\text{DD}} \leq 5.5~V$	0		0.8	V
		20-, 24-pin products: P10, P11	$3.3~V \leq V_{\text{DD}} < 4.0~V$	0		0.5	V
		30-pin products: P01, P10, P11, P13 to P17	$2.4~V \leq V_{\text{DD}} < 3.3~V$	0		0.32	V
	VIL3	P20 to P23	-	0		0.3VDD	V
	VIL4	P60, P61		0		0.3VDD	V
	VIL5	P121, P122, P125 ^{Note 1} , P137, I	EXCLK, RESET	0		0.2VDD	V
Output voltage, high	Vон1	20-, 24-pin products: P00 to P03 ^{Note 2} , P10 to P14,	$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OH1}} = -3.0 \ mA \end{array} \end{array} \label{eq:VDD}$	VDD-0.7			V
		P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	$2.7 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V},$ Ioh1 = -2.0 mA	VDD-0.6			V
			$\begin{array}{l} 2.4 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OH1}} = -1.5 \ mA \end{array}$	V _{DD} -0.5			V
	Vон2	P20 to P23	Іон2 = -100 <i>µ</i> А	VDD-0.5			V

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{V}_{SS} = 0 \text{ V})$

(3/4)

Notes 1. 20, 24-pin products only.

- **2.** 24-pin products only.
- CautionThe maximum value of VIH of pins P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-
pin products, and P00, P10 to P15, P17, and P50 for 30-pin products is VDD even in N-ch open-drain mode.High level is not output in the N-ch open-drain mode.
- Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



(2) 30-pin products

$(T_A = -40 \text{ to } +105^{\circ}\text{C}.$	$2.4 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}$. $\text{V}_{\text{SS}} = 0 \text{ V}$
(17 - 40.0 + 100 0)	, 2.4 • 3 • 66 3 6.6 • , • 66 = 6 • 7

(T _A = -40 to	+105°C,	2.4 V ≤ V	DD \leq 5.5 V, Vss =	= 0 V)					(2/2)
Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply current ^{Note 1}	DD2 Note 2	HALT	HS (High-speed	$f_{IH} = 24 \text{ MHz}^{Note 4}$	V _{DD} = 5.0 V		440	2300	μA
		mode	main) mode ^{Note 6}		V _{DD} = 3.0 V		440	2300	
				fін = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		400	1700	μA
					V _{DD} = 3.0 V		400	1700	
				f _{MX} = 20 MHz ^{Note 3} ,	Square wave input		280	1900	μA
				$V_{DD} = 5.0 V$	Resonator connection		450	2000	
				$f_{MX} = 20 \text{ MHz}^{\text{Note 3}},$ $V_{\text{DD}} = 3.0 \text{ V}$	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				$f_{MX} = 10 \text{ MHz}^{\text{Note 3}},$ $V_{\text{DD}} = 5.0 \text{ V}$	Square wave input		190	1020	μA
					Resonator connection		260	1100	
				$f_{MX} = 10 \text{ MHz}^{\text{Note 3}},$ $V_{\text{DD}} = 3.0 \text{ V}$	Square wave input		190	1020	μA
					Resonator connection		260	1100	
	DD3 Note 5	⁵ STOP T mode T	$T_A = -40^{\circ}C$				0.18	0.50	μA
			T _A = +25°C				0.23	0.50	
			$T_A = +50^{\circ}C$				0.30	1.10	
			$T_A = +70^{\circ}C$	$T_{A} = +70^{\circ}C$ $T_{A} = +85^{\circ}C$			0.46	1.90	
			$T_A = +85^{\circ}C$ $T_A = +105^{\circ}C$				0.75	3.30	
							2.94	15.30	

Notes 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or Vss. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

- 2. During HALT instruction execution by flash memory.
- 3. When high-speed on-chip oscillator clock is stopped.
- 4. When high-speed system clock is stopped.
- Not including the current flowing into the 12-bit interval timer and watchdog timer. 5.
- 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: VDD = 2.7 V to 5.5 V @1 MHz to 24 MHz VDD = 2.4 V to 5.5 V @1 MHz to 16 MHz

- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 - 2. fin: high-speed on-chip oscillator clock frequency
 - 3. Except STOP mode, temperature condition of the TYP. value is TA = 25°C.



3.4 AC Characteristics

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{ V}_{SS} = 0 \text{ V})$

Items	Symbol		Condition	S	MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum	Тсч	Main system	HS (High-	$2.7~V \leq V_{\text{DD}} \leq 5.5~V$	0.04167		1	μS
instruction execution time)		clock (fMAIN) operation	speed main) mode	$2.4~V \leq V_{\text{DD}} < 2.7~V$	0.0625		1	μS
		During self	HS (High-	$2.7~V \leq V_{\text{DD}} \leq 5.5~V$	0.04167		1	μS
		programming	speed main) mode	$2.4~V \leq V_{\text{DD}} < 2.7~V$	0.0625		1	μS
External main system clock	fex	$2.7~V \leq V_{\text{DD}} \leq 5.4$	5 V		1.0		20.0	MHz
frequency		$2.4~V \leq V_{\text{DD}} < 2$.7 V		1.0		16.0	MHz
External main system clock	texн, texL	$2.7~V \leq V_{\text{DD}} \leq 5$.5 V		24			ns
input high-level width, low- level width		$2.4~V \leq V_{\text{DD}} < 2.7~V$			30			ns
TI00 to TI07 input high-level width, low-level width	t⊓∺, t⊤∟		1/fмск + 10			ns		
TO00 to TO07 output	fто	$4.0~V \leq V_{\text{DD}} \leq 5.5~V$					12	MHz
frequency		$2.7~V \leq V_{\text{DD}} < 4.0~V$					8	MHz
		$2.4~V \leq V_{\text{DD}} < 2.7~V$					4	MHz
PCLBUZ0, or PCLBUZ1	f PCL	$4.0~V \leq V_{\text{DD}} \leq 5$.5 V				16	MHz
output frequency		$2.7~V \leq V_{\text{DD}} < 4.0~V$					8	MHz
		$2.4~V \leq V_{\text{DD}} < 2$			4	MHz		
INTP0 to INTP5 input high- level width, low-level width	tinth, tintl				1			μS
KR0 to KR9 input available width	t KR				250			ns
RESET low-level width	trsL				10			μS

Remark fmck: Timer array unit operation clock frequency

(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))



3.5 Peripheral Functions Characteristics

AC Timing Test Point



3.5.1 Serial array unit

(1) During communication at same potential (UART mode) (T_A = -40 to +105°C, 2.4 V \leq V_{DD} \leq 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-spee	Unit	
			MIN.	MAX.	
Transfer rate				fмск/12	bps
Note 1		Theoretical value of the maximum transfer rate $f_{CLK} = f_{MCK}^{Note2}$		2.0	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

- 2. The maximum operating frequencies of the CPU/peripheral hardware clock (fcLk) are: HS (high-speed main) mode: 24 MHz (2.7 V \leq V_{DD} \leq 5.5 V) 16 MHz (2.4 V \leq V_{DD} \leq 5.5 V)
- **Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

- 2. fMCK: Serial array unit operation clock frequency
 - (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
 - m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))





CSI mode serial transfer timing (during communication at same potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)





- Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)
 2. fMCK: Serial array unit operation clock frequency
 - (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3))



UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)





- **Remarks 1.** R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage
 - **2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)
 - fmck: Serial array unit operation clock frequency (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

4. UART0 of the 20- and 24-pin products supports communication at different potential only when the peripheral I/O redirection function is not used.



- **Notes 1.** Excludes quantization error ($\pm 1/2$ LSB).
 - **2.** This value is indicated as a ratio (%FSR) to the full-scale value.
 - 3. When AV_{REFP} < V_{DD}, the MAX. values are as follows. Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}. Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}. Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.
 - 4. Refer to 29.6.2 Temperature sensor/internal reference voltage characteristics.
- (2) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22

(TA = -40 to +105°C, 2.4 V \leq AV _{REFP} \leq V _{DD} \leq 5.5 V, V _{SS} = 0 V, Reference voltation	age (+) = AVREFP, Reference voltage (-) =
AVREFM = 0 V)	

Parameter	Symbol	Conditio	ns	MIN.	TYP.	MAX.	Unit
Resolution	Res			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}			1.2	±5.0	LSB
Conversion time	tCONV	10-bit resolution	$3.6~V \leq V \text{DD} \leq 5.5~V$	2.125		39	μs
		Target ANI pin: ANI16 to ANI22	$2.7~V \leq V \text{DD} \leq 5.5~V$	3.1875		39	μs
			$2.4~V \leq V \text{DD} \leq 5.5~V$	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}				±0.35	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}				±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}				±3.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}				±2.0	LSB
Analog input voltage	VAIN	ANI16 to ANI22		0		AVREFP and VDD	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

