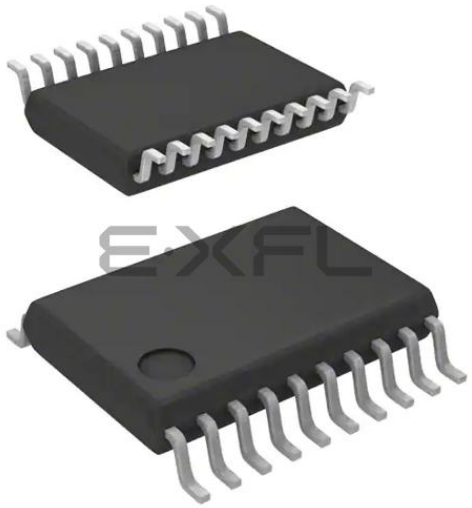
# Renesas Electronics America Inc - R5F10268GSP#X5 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CSI, I²C, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 14 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 768 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 11x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-LSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10268gsp-x5 |

○ ROM, RAM capacities

| Code flash | Data flash | RAM | 20 pins | 24 pins | 30 pins |
|---|---|---|---|---|---|
| 16 KB | 2 KB | 2 KB | — | — | R5F102AA |
| | — | | — | — | R5F103AA |
| | 2 KB | 1.5 KB | R5F1026A Note 1 | R5F1027A Note 1 | — |
| | — | | R5F1036A Note 1 | R5F1037A Note 1 | — |
| 12 KB | 2KB | 1 KB | R5F10269 Note 1 | R5F10279 Note 1 | R5F102A9 |
| | — | | R5F10369 Note 1 | R5F10379 Note 1 | R5F103A9 |
| 8 KB | 2 KB | 768 B | R5F10268 Note 1 | R5F10278 Note 1 | R5F102A8 |
| | — | | R5F10368 Note 1 | R5F10378 Note 1 | R5F103A8 |
| 4 KB | 2KB | 512 B | R5F10267 | R5F10277 | R5F102A7 |
| | — | | R5F10367 | R5F10377 | R5F103A7 |
| 2 KB | 2 KB | 256 B | R5F10266 Note 2 | — | — |
| | — | | R5F10366 Note 2 | — | — |

**Notes 1.** This is 640 bytes when the self-programming function or data flash function is used. (For details, see **CHAPTER 3 CPU ARCHITECTURE**.)

**2.** The self-programming function cannot be used for R5F10266 and R5F10366.

**Caution** When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

### 1.3.2 On-chip oscillator characteristics

(1) High-speed on-chip oscillator oscillation frequency of the R5F102 products

| Oscillator | Condition | MIN | MAX | Unit |
|---|---|---|---|---|
| High-speed on-chip oscillator oscillation frequency accuracy | $T_A$ = -20 to +85 °C | -1.0 | +1.0 | % |
| | $T_A$ = -40 to -20 °C | -1.5 | +1.5 | |
| | $T_A$ = +85 to +105 °C | -2.0 | +2.0 | |

(2) High-speed on-chip oscillator oscillation frequency of the R5F103 products

| Oscillator | Condition | MIN | MAX | Unit |
|---|---|---|---|---|
| High-speed on-chip oscillator oscillation frequency accuracy | $T_A$ = -40 to + 85 °C | -5.0 | +5.0 | % |

### 1.3.3 Peripheral Functions

The following are differences in peripheral functions between the R5F102 products and the R5F103 products.

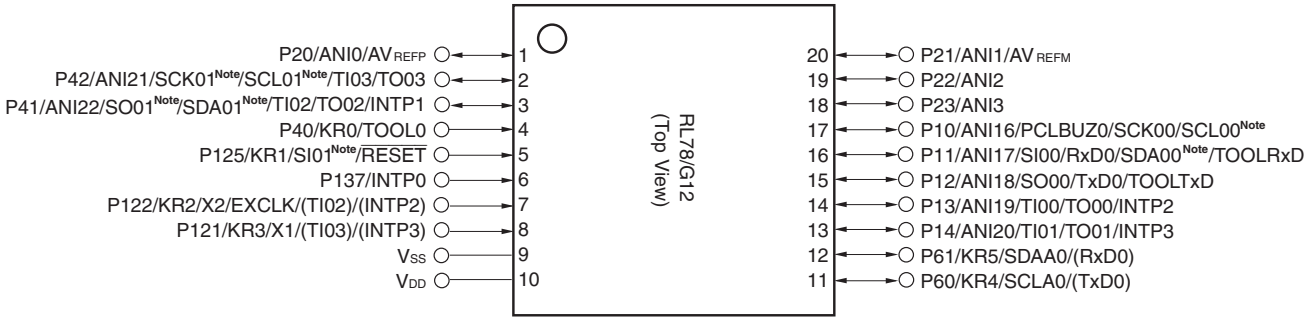
| RL78/G12 | | R5F102 product | | R5F103 product | |
|---|---|---|---|---|---|
| | | 20, 24 pin product | 30 pin product | 20, 24 pin product | 30 pin product |
| Serial interface | UART | 1 channel | 3 channels | 1 channel | |
| | CSI | 2 channels | 3 channels | 1 channel | |
| | Simplified $I^2C$ | 2 channels | 3 channels | None | |
| DMA function | | 2 channels | | None | |
| Safety function | CRC operation | Yes | | None | |
| | RAM guard | Yes | | None | |
| | SFR guard | Yes | | None | |

## 1.4 Pin Configuration (Top View)

### 1.4.1 20-pin products

- 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)

<R>




**Note** Provided only in the R5F102 products.

**Remarks 1.** For pin identification, see **1.5 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

## 1.5 Pin Identification

| | |
|---|---|
| ANI0 to ANI3, ANI16 to ANI22: | Analog input |
| AVREFM: | Analog Reference Voltage Minus |
| AVREFP: | Analog reference voltage plus |
| EXCLK: | External Clock Input (Main System Clock) |
| INTP0 to INTP5 | Interrupt Request From Peripheral |
| KR0 to KR9: | Key Return |
| P00 to P03: | Port 0 |
| P10 to P17: | Port 1 |
| P20 to P23: | Port 2 |
| P30 to P31: | Port 3 |
| P40 to P42: | Port 4 |
| P50, P51: | Port 5 |
| P60, P61: | Port 6 |
| P120 to P122, P125: | Port 12 |
| P137: | Port 13 |
| P147: | Port 14 |
| PCLBUZ0, PCLBUZ1: | Programmable Clock Output/ Buzzer Output |
| REGC: | Regulator Capacitance |
| $\overline{\text{RESET}}$: | Reset |
| RxD0 to RxD2: | Receive Data |
| SCK00, SCK01, SCK11, SCK20: | Serial Clock Input/Output |
| SCL00, SCL01, SCL11, SCL20, SCLA0: | Serial Clock Input/Output |
| SDA00, SDA01, SDA11, SDA20, SDAA0: | Serial Data Input/Output |
| SI00, SI01, SI11, SI20: | Serial Data Input |
| SO00, SO01, SO11, SO20: | Serial Data Output |
| TI00 to TI07: | Timer Input |
| TO00 to TO07: | Timer Output |
| TOOL0: | Data Input/Output for Tool |
| TOOLRxD, TOOLTxD: | Data Input/Output for External Device |
| TxD0 to TxD2: | Transmit Data |
| VDD: | Power supply |
| VSS: | Ground |
| X1, X2: | Crystal Oscillator (Main System Clock) |

## 2.2 Oscillator Characteristics

### 2.2.1 X1 oscillator characteristics

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$)[Note] | Ceramic resonator / crystal oscillator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 8.0 | |

**Note** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

**Remark** When using the X1 oscillator, refer to **5.4 System Clock Oscillator**.

### 2.2.2 On-chip oscillator characteristics

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency [Notes 1, 2] | $f_{IH}$ | | | 1 | | 24 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | R5F102 products | $T_A$ = −20 to +85°C | -1.0 | | +1.0 | % |
| | | | $T_A$ = −40 to −20°C | -1.5 | | +1.5 | % |
| | | R5F103 products | | -5.0 | | +5.0 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | -15 | | +15 | % |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

**2.** This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (4/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, low | $V_{OL1}$ | 20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 20.0 mA | | | 1.3 | V |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P23 | $I_{OL2}$ = 400 μA | | | 0.4 | V |
| | $V_{OL3}$ | P60, P61 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 2.0 mA | | | 0.4 | V |
| Input leakage current, high | $I_{LIH1}$ | Other than P121, P122 | $V_I$ = $V_{DD}$ | | | 1 | μA |
| | $I_{LIH2}$ | P121, P122 (X1, X2/EXCLK) | $V_I$ = $V_{DD}$ Input port or external clock input | | | 1 | μA |
| | | | $V_I$ = $V_{DD}$ When resonator connected | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | Other than P121, P122 | $V_I$ = $V_{SS}$ | | | −1 | μA |
| | $I_{LIL2}$ | P121, P122 (X1, X2/EXCLK) | $V_I$ = $V_{SS}$ Input port or external clock input | | | −1 | μA |
| | | | $V_I$ = $V_{SS}$ When resonator connected | | | −10 | μA |
| On-chip pull-up resistance | $R_U$ | 20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42, P125, $\overline{\text{RESET}}$<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | $V_I$ = $V_{SS}$, input port | 10 | 20 | 100 | kΩ |

**Note** 24-pin products only.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.3.2 Supply current characteristics

**(1) 20-, 24-pin products**

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD1}$ | Operating mode | HS(High-speed main) mode[Note 4] | $f_{IH}$ = 24 MHz[Note 3] | Basic operation | $V_{DD}$ = 5.0 V | | 1.5 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.5 | | |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.3 | 5.0 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.3 | 5.0 | |
| | | | | $f_{IH}$ = 16 MHz[Note 3] | | $V_{DD}$ = 5.0 V | | 2.5 | 3.7 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.5 | 3.7 | |
| | | | LS(Low-speed main) mode[Note 4] | $f_{IH}$ = 8 MHz[Note 3] | | $V_{DD}$ = 3.0 V | | 1.2 | 1.8 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.2 | 1.8 | |
| | | | HS(High-speed main) mode[Note4] | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 2.8 | 4.4 | mA |
| | | | | | | Resonator connection | | 3.0 | 4.6 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 2.8 | 4.4 | mA |
| | | | | | | Resonator connection | | 3.0 | 4.6 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 1.8 | 2.6 | mA |
| | | | | | | Resonator connection | | 1.8 | 2.6 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 1.8 | 2.6 | mA |
| | | | | | | Resonator connection | | 1.8 | 2.6 | |
| | | | LS(Low-speed main) mode[Note 4] | $f_{MX}$ = 8 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 1.1 | 1.7 | mA |
| | | | | | | Resonator connection | | 1.1 | 1.7 | |
| | | | | $f_{MX}$ = 8 MHz[Note 2], $V_{DD}$ = 2.0 V | | Square wave input | | 1.1 | 1.7 | mA |
| | | | | | | Resonator connection | | 1.1 | 1.7 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator clock is stopped.

**3.** When high-speed system clock is stopped

**4.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS(Low speed main) mode: $V_{DD}$ = 1.8 V to 5.5 V @1 MHz to 8 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Temperature condition of the TYP. value is $T_A$ = 25°C.

**(2) 30-pin products**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (High-speed main) mode Note 4 | $f_{IH}$ = 24 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 1.5 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.5 | | |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.7 | 5.5 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.7 | 5.5 | |
| | | | | $f_{IH}$ = 16 MHz Note 3 | | $V_{DD}$ = 5.0 V | | 2.7 | 4.0 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.7 | 4.0 | |
| | | | LS (Low-speed main) mode Note 4 | $f_{IH}$ = 8 MHz Note 3 | | $V_{DD}$ = 3.0 V | | 1.2 | 1.8 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.2 | 1.8 | |
| | | | HS (High-speed main) mode Note 4 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | | Square wave input | | 3.0 | 4.6 | mA |
| | | | | | | Resonator connection | | 3.2 | 4.8 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | | Square wave input | | 3.0 | 4.6 | mA |
| | | | | | | Resonator connection | | 3.2 | 4.8 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | | Square wave input | | 1.9 | 2.7 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.7 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | | Square wave input | | 1.9 | 2.7 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.7 | |
| | | | LS (Low-speed main) mode Note 4 | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.0 V | | Square wave input | | 1.1 | 1.7 | mA |
| | | | | | | Resonator connection | | 1.1 | 1.7 | |
| | | | | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 2.0 V | | Square wave input | | 1.1 | 1.7 | mA |
| | | | | | | Resonator connection | | 1.1 | 1.7 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator clock is stopped.

**3.** When high-speed system clock is stopped

**4.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS(Low speed main) mode: $V_{DD}$ = 1.8 V to 5.5 V @1 MHz to 8 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Temperature condition of the TYP. value is $T_A$ = 25°C.

**(2) 30-pin products**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 6 | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 440 | 1280 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 1280 | |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 400 | 1000 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 1000 | |
| | | | LS (Low-speed main) mode Note 6 | $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 260 | 530 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 260 | 530 | |
| | | | HS (High-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1000 | μA |
| | | | | | Resonator connection | | 450 | 1170 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1000 | μA |
| | | | | | Resonator connection | | 450 | 1170 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 190 | 600 | μA |
| | | | | | Resonator connection | | 260 | 670 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 190 | 600 | μA |
| | | | | | Resonator connection | | 260 | 670 | |
| | | | LS (Low-speed main) mode Note 6 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | |
| | | | | $f_{MX}$ = 8 MHz Note 3 $V_{DD}$ = 2.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | |
| | $I_{DD3}$ Note 5 | STOP mode | $T_A$ = –40°C | | | | 0.18 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.30 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.46 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.75 | 3.30 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS (Low speed main) mode: $V_{DD}$ = 1.8 V to 5.5 V @1 MHz to 8 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C.

### (3) Peripheral functions (Common to all products)

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed onchip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | μA |
| 12-bit interval timer operating current | $I_{TMKA}$ Notes 1, 2, 3 | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 4 | $f_{IL}$ = 15 kHz | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 5 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | 1.30 | 1.70 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.50 | 0.70 | mA |
| A/D converter reference voltage operating current | $I_{ADREF}$ Note 1 | | | | 75.0 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | 75.0 | | μA |
| LVD operating current | $I_{LVD}$ Notes 1, 6 | | | | 0.08 | | μA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 8 | | | | 2.00 | 12.20 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 7 | | | | 2.00 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 9 | | 0.50 | 0.60 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 1.44 | mA |
| | | CSI/UART operation | | | 0.70 | 0.84 | mA |

**Notes 1.** Current flowing to the $V_{DD}$.

**2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**3.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$, and $I_{FIL}$ and $I_{TMKA}$ when the 12-bit interval timer operates.

**4.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer operates.

**5.** Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**6.** Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit operates.

**7.** Current flowing only during data flash rewrite.

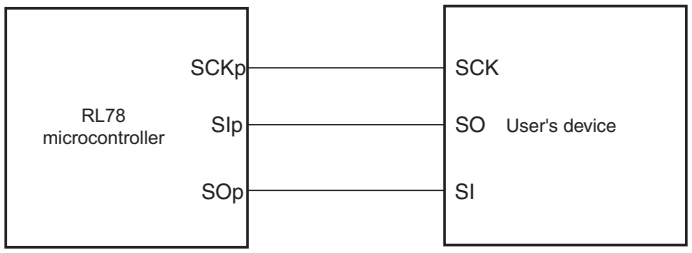
**8.** Current flowing only during self programming.

**9.** For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.

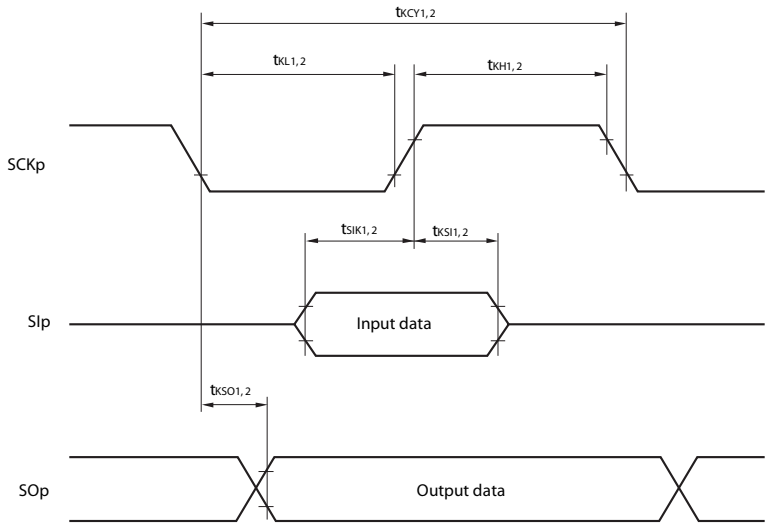
**Remarks 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**2.** Temperature condition of the TYP. value is $T_A$ = 25°C

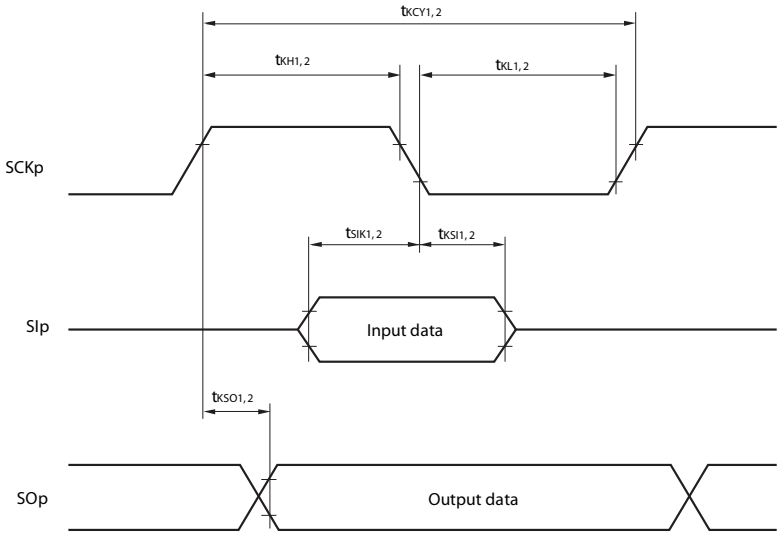
**CSI mode connection diagram (during communication at same potential)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




(**Remarks** are listed on the next page.)

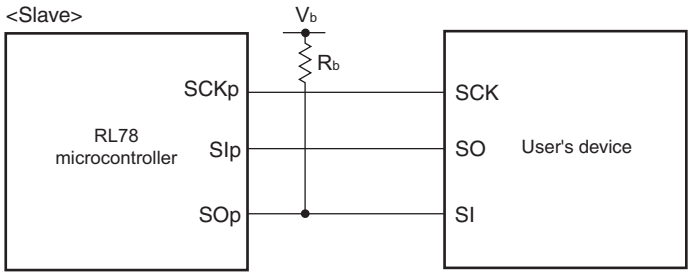
**(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCK00 cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 2/f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 200 | | 1150 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 300 | | 1150 | | ns |
| SCK00 high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2– 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 120 | | $t_{KCY1}$/2 – 120 | | ns |
| SCK00 low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 7 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 10 | | $t_{KCY1}$/2 – 50 | | ns |
| SI00 setup time (to SCK00↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 58 | | 479 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 121 | | 479 | | ns |
| SI00 hold time (from SCK00↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | ns |
| Delay time from SCK00↓ to SO00 output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 60 | | 60 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 130 | | 130 | ns |
| SI00 setup time (to SCK00↓) Note 2 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 23 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 33 | | 110 | | ns |
| SI00 hold time (from SCK00↓) Note 2 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | ns |
| Delay time from SCK00↑ to SO00 output Note 2 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 10 | | 10 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 10 | | 10 | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**

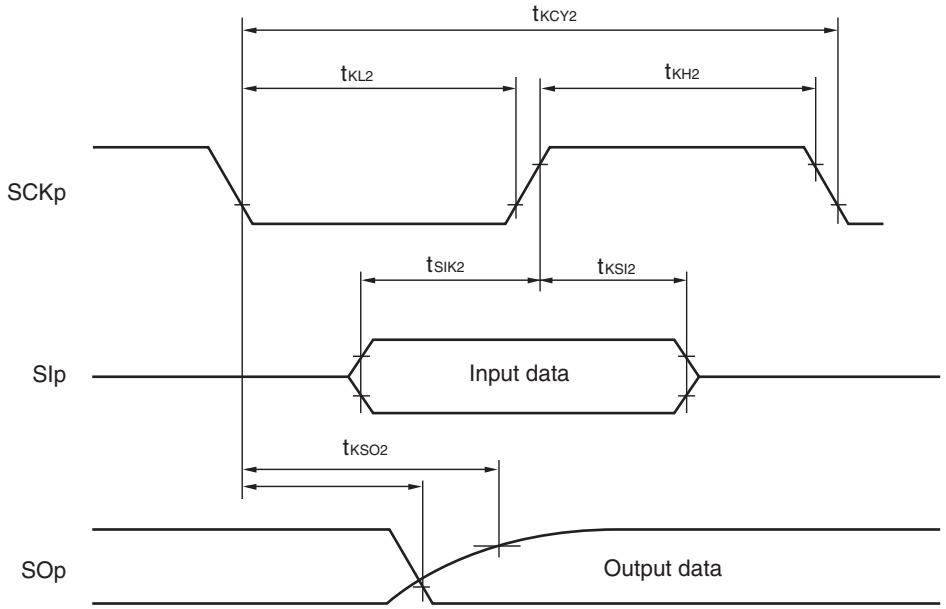



**Remarks 1.** $R_b$ [Ω]: Communication line (SOp) pull-up resistance, $C_b$ [F]: Communication line (SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 10))

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

**4.** Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

**5.** Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | 1.2 | ±5.0 | LSB |
| | | | | | 1.2 | ±8.5 Note 4 | LSB |
| Conversion time | tCONV | 10-bit resolution<br>Target ANI pin: ANI16 to ANI22 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | | | 57 | | 95 | μs |
| Zero-scale error Notes 1, 2 | EZS | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±0.35 | %FSR |
| | | | | | | ±0.60 Note 4 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±0.35 | %FSR |
| | | | | | | ±0.60 Note 4 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±3.5 | LSB |
| | | | | | | ±6.0 Note 4 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±2.0 | LSB |
| | | | | | | ±2.5 Note 4 | LSB |
| Analog input voltage | VAIN | ANI16 to ANI22 | | 0 | | $AV_{REFP}$ and $V_{DD}$ | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

**4.** When the conversion time is set to 57 μs (min.) and 95 μs (max.).

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (2/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low[Note 1] | $I_{OL1}$ | 20-, 24-pin products:<br>Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42<br>30-pin products:<br>Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | | | 8.5 [Note 2] | mA |
| | | Per pin for P60, P61 | | | | 15.0 [Note 2] | mA |
| | | 20-, 24-pin products:<br>Total of P40 to P42<br>30-pin products:<br>Total of P00, P01, P40, P120<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 25.5 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 9.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 1.8 | mA |
| | | 20-, 24-pin products:<br>Total of P00 to P03[Note 4], P10 to P14, P60, P61<br>30-pin products:<br>Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 27.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 5.4 | mA |
| | | Total of all pins (When duty ≤ 70% [Note 3]) | | | | 65.5 | mA |
| | $I_{OL2}$ | Per pin for P20 to P23 | | | | 0.4 | mA |
| | | Total of all pins | | | | 1.6 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $V_{SS}$ pin.

**2.** However, do not exceed the total current value.

**3.** The output current value under conditions where the duty factor ≤ 70%.
If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**4.** 24-pin products only.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (3/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | Normal input buffer<br>20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | TTL input buffer<br>20-, 24-pin products: P10, P11<br>30-pin products: P01, P10, P11, P13 to P17 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 2.2 | | $V_{DD}$ | V |
| | | | 3.3 V ≤ $V_{DD}$ < 4.0 V | 2.0 | | $V_{DD}$ | V |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V | 1.5 | | $V_{DD}$ | V |
| | $V_{IH3}$ | Normal input buffer<br>P20 to P23 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60, P61 | | 0.7$V_{DD}$ | | 6.0 | V |
| | $V_{IH5}$ | P121, P122, P125[Note 1], P137, EXCLK, $\overline{\text{RESET}}$ | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | Normal input buffer<br>20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | 0 | | 0.2$V_{DD}$ | V |
| | $V_{IL2}$ | TTL input buffer<br>20-, 24-pin products: P10, P11<br>30-pin products: P01, P10, P11, P13 to P17 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | 3.3 V ≤ $V_{DD}$ < 4.0 V | 0 | | 0.5 | V |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P23 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL4}$ | P60, P61 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL5}$ | P121, P122, P125[Note 1], P137, EXCLK, $\overline{\text{RESET}}$ | | 0 | | 0.2$V_{DD}$ | V |
| Output voltage, high | $V_{OH1}$ | 20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –3.0 mA | $V_{DD}$–0.7 | | | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –2.0 mA | $V_{DD}$–0.6 | | | V |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –1.5 mA | $V_{DD}$–0.5 | | | V |
| | $V_{OH2}$ | P20 to P23 | $I_{OH2}$ = –100 μA | $V_{DD}$–0.5 | | | V |

**Notes 1.** 20, 24-pin products only.

**2.** 24-pin products only.

**Caution** The maximum value of $V_{IH}$ of pins P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products is $V_{DD}$ even in N-ch open-drain mode. High level is not output in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| Transfer rate Note4 | | Reception | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |
| | | Transmission | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | **Note 3** | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.0 Note 4 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, | | **Note 5** | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 6 | Mbps |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | **Notes 2, 7** | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 8 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**3.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ $V_{DD}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 600 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 1000 | | ns |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 2300 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 –150 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 –340 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 –916 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 –24 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 –36 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 –100 | | ns |

**Cautions 1.** Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.

**2.** CSI01 and CSI11 cannot communicate at different potential.

**Remarks 1.** $R_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$ [F]: Communication line (SCKp, SOp) load capacitance, $V_b$ [V]: Communication line voltage

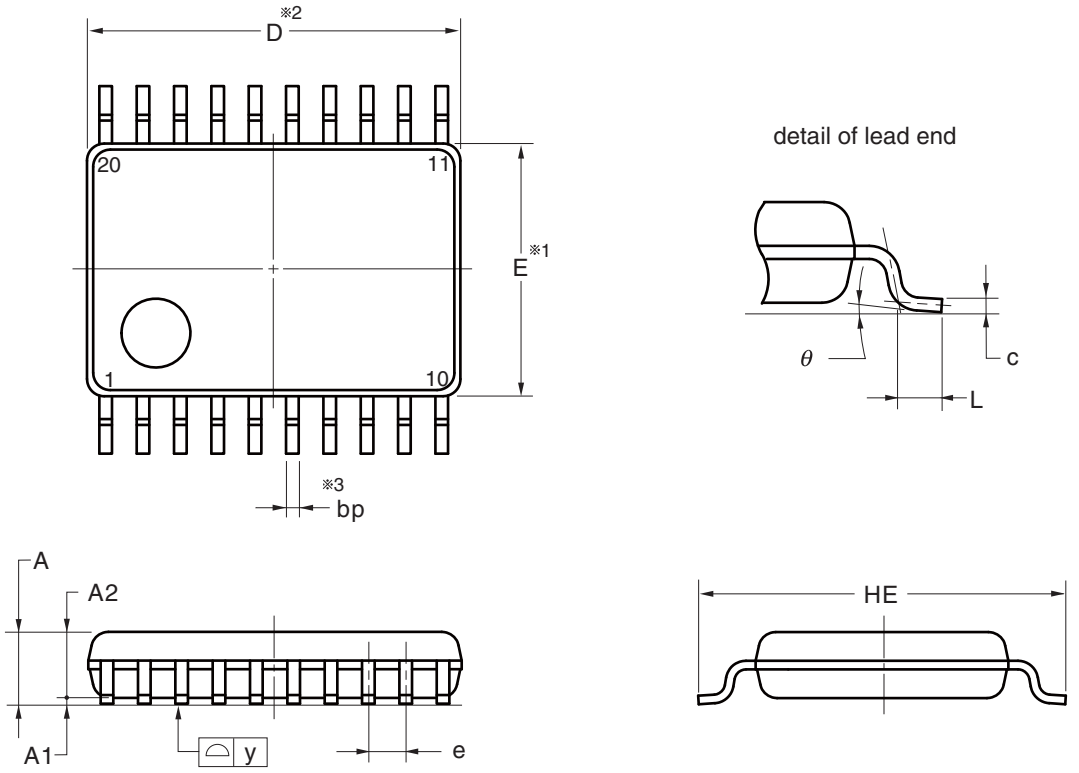
**2.** p: CSI number (p = 00, 20)

# 4. PACKAGE DRAWINGS

## 4.1 20-pin products

R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP
R5F1036AASP, R5F10369ASP, R5F10368ASP, R5F10367ASP, R5F10366ASP
R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP
R5F1036ADSP, R5F10369DSP, R5F10368DSP, R5F10367DSP, R5F10366DSP
<R> R5F1026AGSP, R5F10269GSP, R5F10268GSP, R5F10267GSP, R5F10266GSP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LSSOP20-4.4x6.5-0.65 | PLSP0020JB-A | P20MA-65-NAA-1 | 0.1 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 6.50±0.10 |
| E | 4.40±0.10 |
| HE | 6.40±0.20 |
| A | 1.45 MAX. |
| A1 | 0.10±0.10 |
| A2 | 1.15 |
| e | 0.65±0.12 |
| bp | $0.22^{+0.10}_{-0.05}$ |
| c | $0.15^{+0.05}_{-0.02}$ |
| L | 0.50±0.20 |
| y | 0.10 |
| θ | 0° to 10° |

**NOTE**

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

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