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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

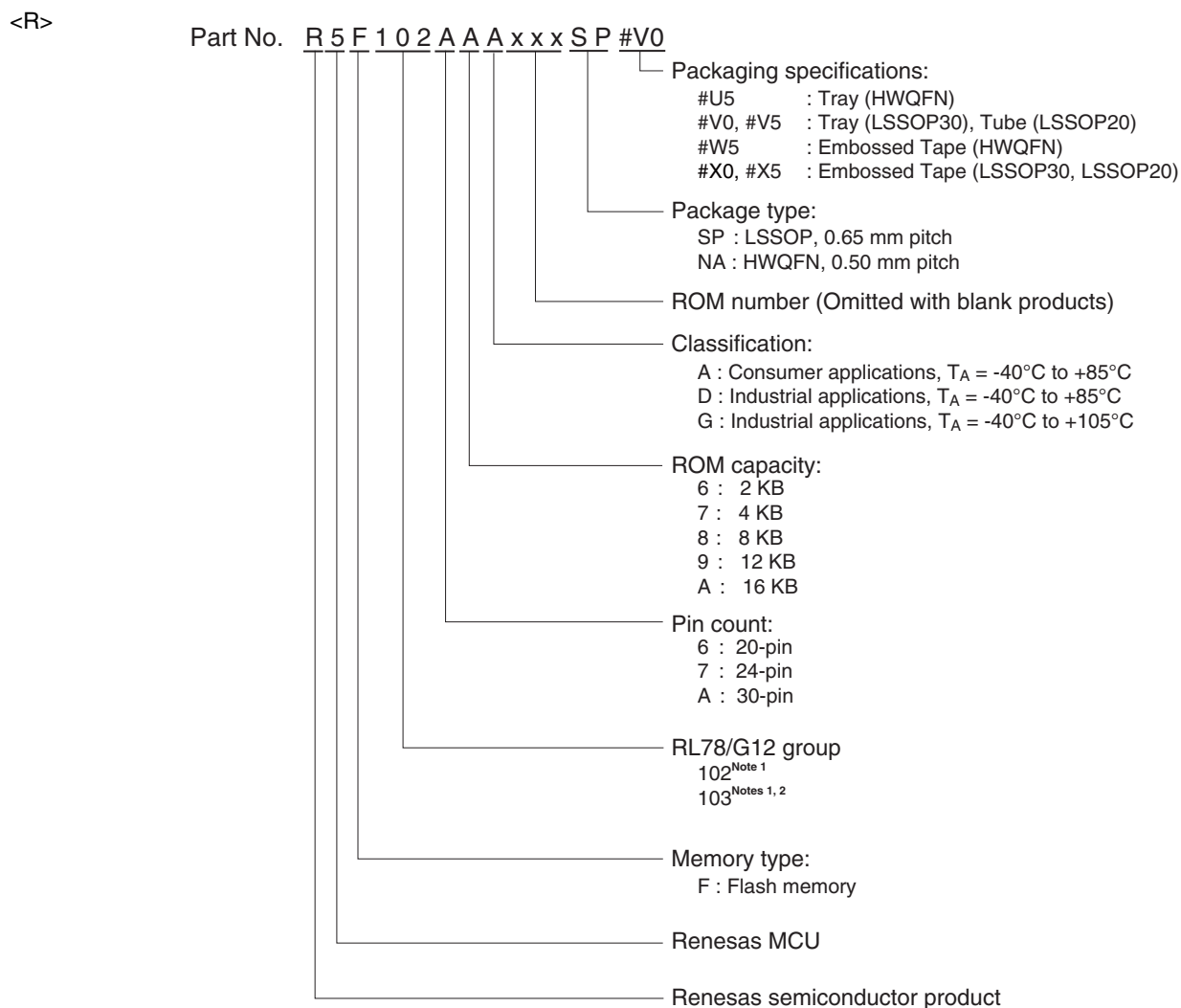
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10269asp-x0

1.2 List of Part Numbers

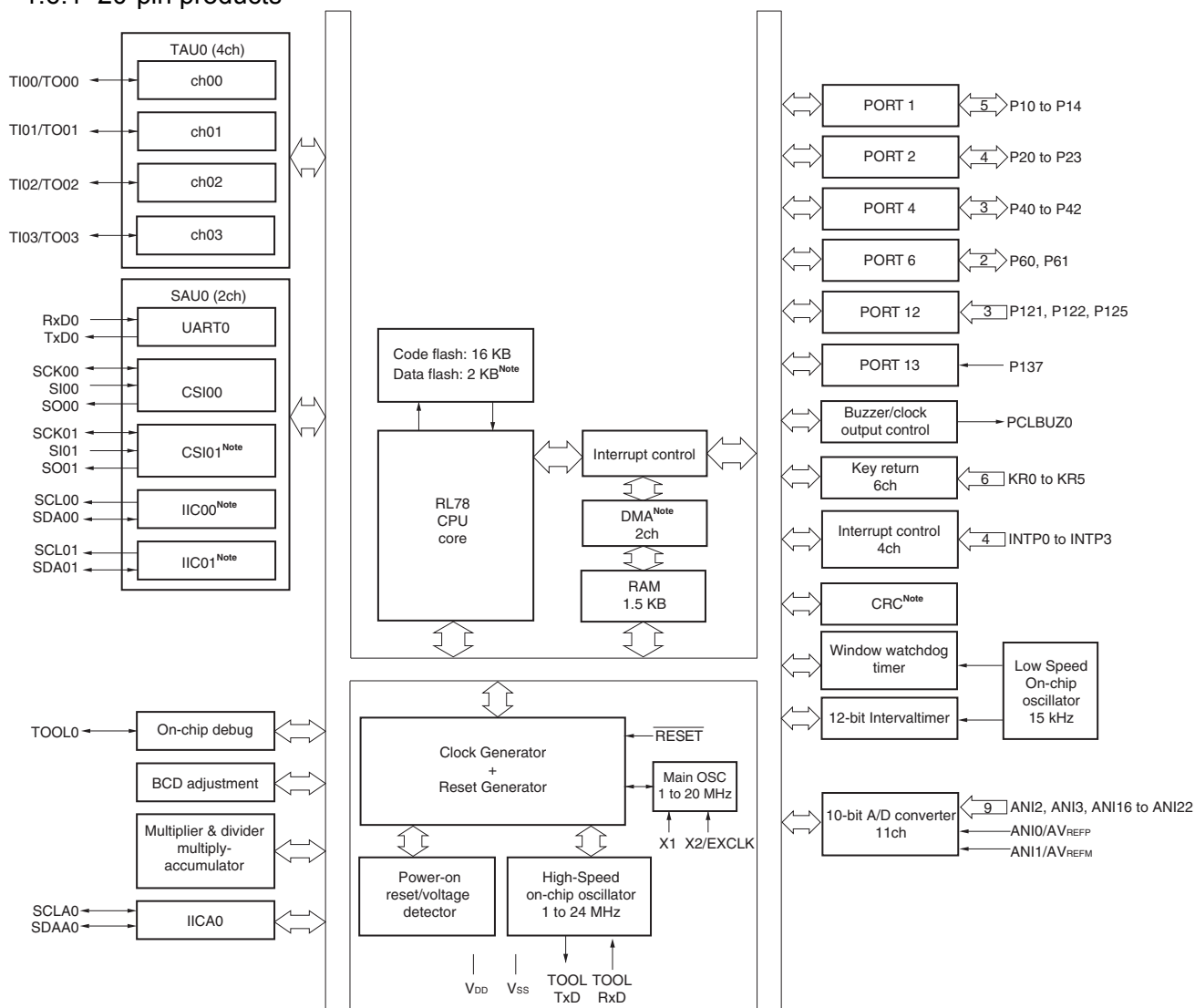
Figure 1-1. Part Number, Memory Size, and Package of RL78/G12



- Notes**
1. For details about the differences between the R5F102 products and the R5F103 products of RL78/G12, see **1.1 Differences between the R5F102 Products and the R5F103 Products**.
 2. Products only for "A: Consumer applications ($T_A = -40$ to $+85^{\circ}\text{C}$)" and "D: Industrial applications ($T_A = -40$ to $+85^{\circ}\text{C}$)"

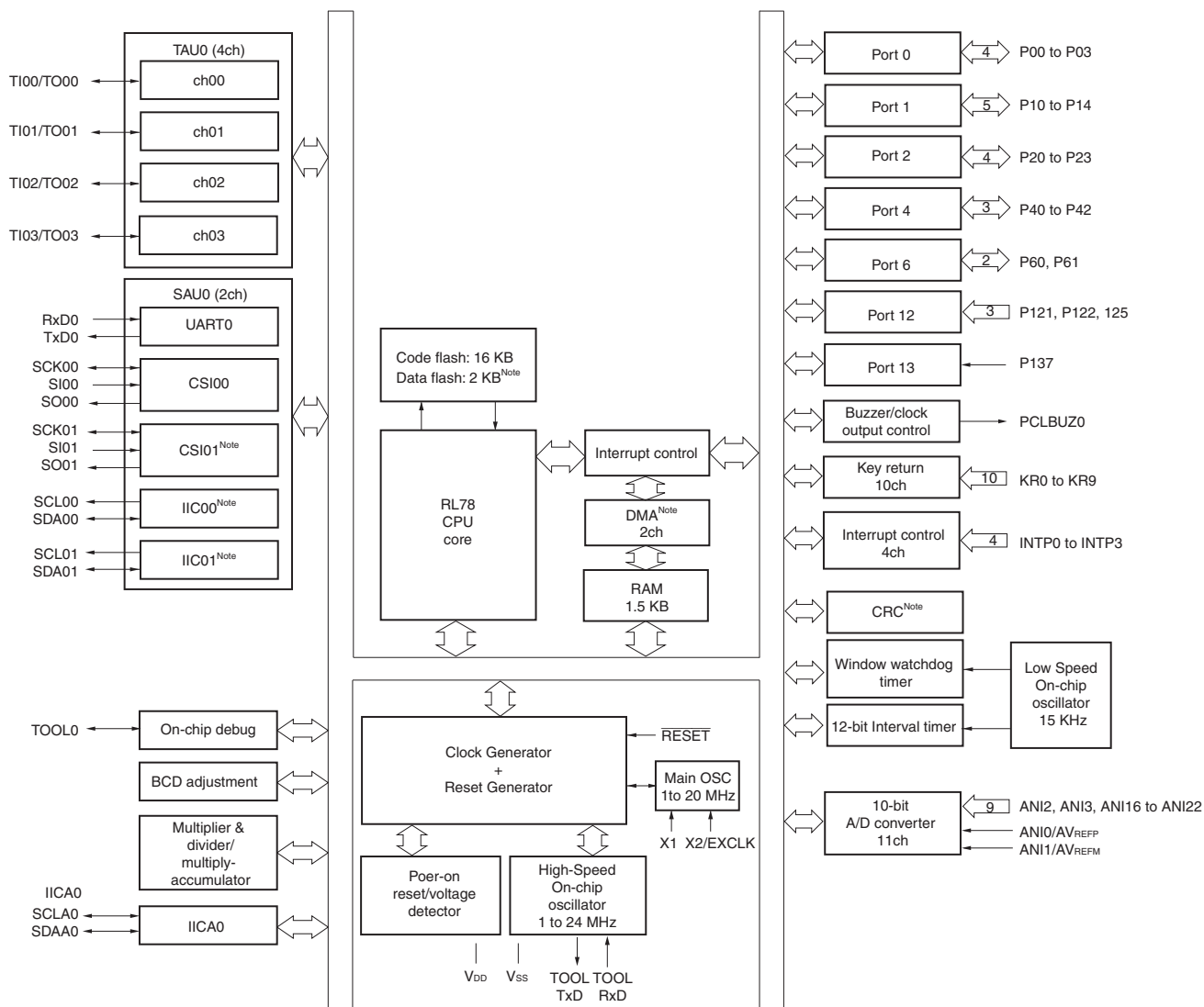
1.6 Block Diagram

1.6.1 20-pin products



Note Provided only in the R5F102 products.

1.6.2 24-pin products



Note Provided only in the R5F102 products.

<R> 2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$)

<R> This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A = -40$ to $+85^\circ\text{C}$

<R> R5F102xxAxx, R5F103xxAxx

D: Industrial applications $T_A = -40$ to $+85^\circ\text{C}$

<R> R5F102xxDxx, R5F103xxDxx

G: Industrial applications when $T_A = -40$ to $+105^\circ\text{C}$ products is used in the range of $T_A = -40$ to $+85^\circ\text{C}$

<R> R5F102xxGxx

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product.

2.2 Oscillator Characteristics

2.2.1 X1 oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_x) ^{Note}	Ceramic resonator / crystal oscillator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		8.0	

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **5.4 System Clock Oscillator**.

2.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		R5F102 products	$T_A = -20$ to $+85^\circ\text{C}$	-1.0		+1.0	%
			$T_A = -40$ to -20°C	-1.5		+1.5	%
		R5F103 products		-5.0		+5.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

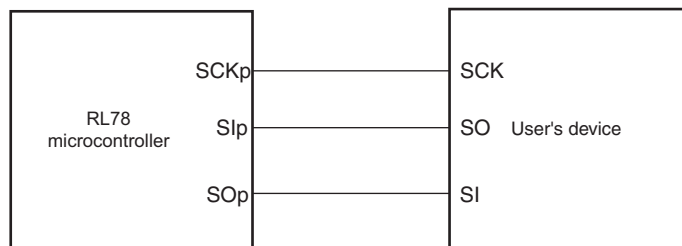
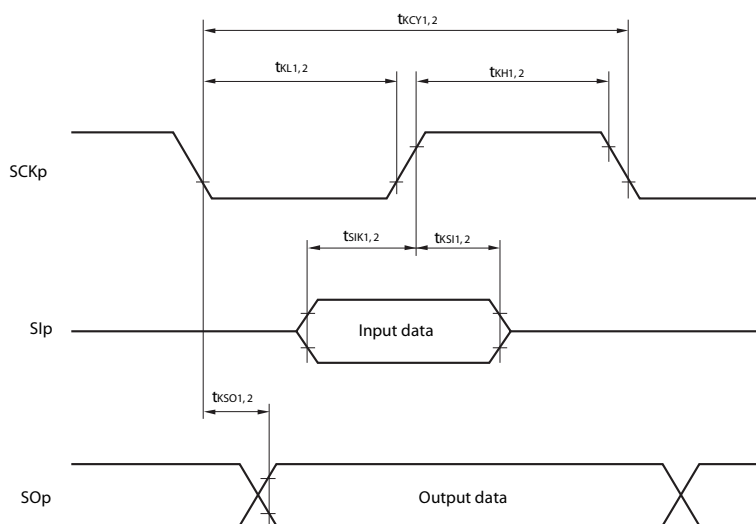
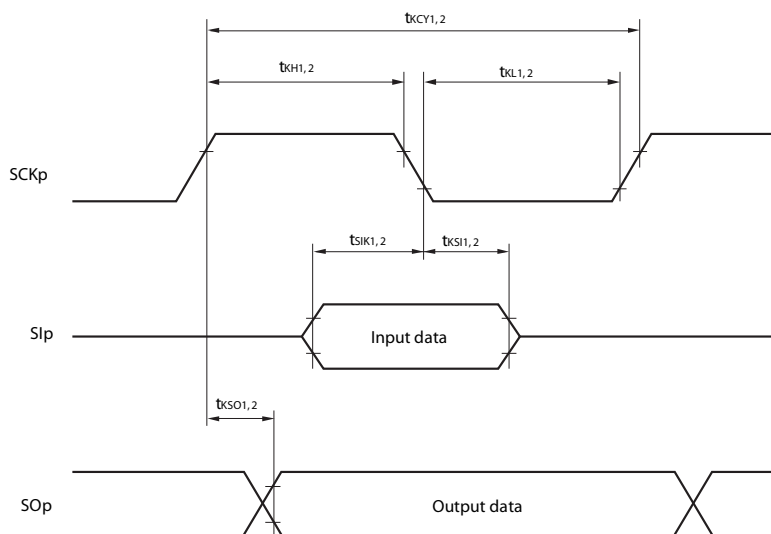
2.4 AC Characteristics

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (High-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			During self programming	HS (High-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1
		2.7 V ≤ V _{DD} ≤ 5.5 V			0.04167		1	μs
		LS (Low-speed main) mode		2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
External main system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V _{DD} < 2.4 V			1.0		8.0	MHz
External main system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V _{DD} < 2.7 V			30			ns
		1.8 V ≤ V _{DD} < 2.4 V			60			ns
TI00 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}				1/f _{MCK} + 10			ns
TO00 to TO07 output frequency	f _{TO}	4.0 V ≤ V _{DD} ≤ 5.5 V					12	MHz
		2.7 V ≤ V _{DD} < 4.0 V					8	MHz
		1.8 V ≤ V _{DD} < 2.7 V					4	MHz
PCLBUZ0, or PCLBUZ1 output frequency	f _{PCL}	4.0 V ≤ V _{DD} ≤ 5.5 V					16	MHz
		2.7 V ≤ V _{DD} < 4.0 V					8	MHz
		1.8 V ≤ V _{DD} < 2.7 V					4	MHz
INTP0 to INTP5 input high-level width, low-level width	t _{INTH} , t _{INTL}				1			μs
KR0 to KR9 input available width	t _{KR}				250			ns
RESET low-level width	t _{RSL}				10			μs

Remark fMCK: Timer array unit operation clock frequency

(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

CSI mode connection diagram (during communication at same potential)**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)****CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**

(Remarks are listed on the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate <small>Note4</small>		Reception	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			f _{MCK} /6 <small>Note1</small>	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} <small>Note3</small>			4.0	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			f _{MCK} /6 <small>Note1</small>	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} <small>Note3</small>			4.0	Mbps
			1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			f _{MCK} /6 <small>Notes1, 2</small>	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} <small>Note3</small>			4.0	Mbps
		Transmission	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			Note4	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V			2.8 <small>Note5</small>	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V,			Note6	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V			1.2 <small>Note7</small>	Mbps
			1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			Notes 2, 8	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V			0.43 <small>Note9</small>	Mbps

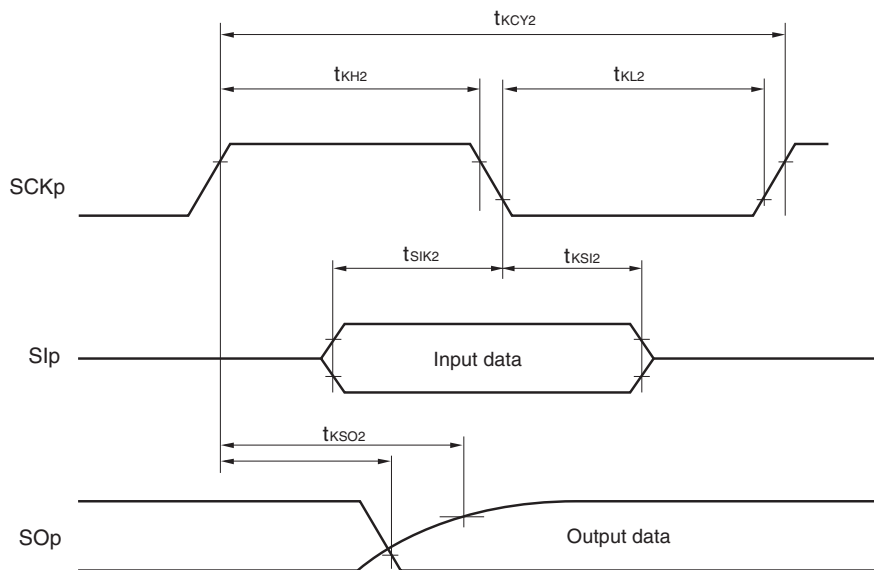
Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.2. Use it with V_{DD} ≥ V_b.3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)4. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-) = AV_{REFM}
ANI0 to ANI3	Refer to 28.6.1 (1) .	Refer to 28.6.1 (3) .	Refer to 28.6.1 (4) .
ANI16 to ANI22	Refer to 28.6.1 (2) .		
Internal reference voltage Temperature sensor output voltage	Refer to 28.6.1 (1) .		—

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}			1.2	± 3.5	LSB
					1.2	± 7.0 ^{Note 4}	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2, ANI3	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
				57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 0.25	%FSR
						± 0.50 ^{Note 4}	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 0.25	%FSR
						± 0.50 ^{Note 4}	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 2.5	LSB
						± 5.0 ^{Note 4}	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 1.5	LSB
						± 2.0 ^{Note 4}	LSB
Analog input voltage	V_{AIN}	ANI2, ANI3		0		AV_{REFP}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} ^{Note 5}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TMPS25} ^{Note 5}			V

(Notes are listed on the next page.)

- Notes**
1. Excludes quantization error ($\pm 1/2$ LSB).
 2. This value is indicated as a ratio (%FSR) to the full-scale value.
 3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
 Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
 Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 4. Values when the conversion time is set to $57\ \mu\text{s}$ (min.) and $95\ \mu\text{s}$ (max.).
 5. Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (–) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI16 to ANI22

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\ \text{V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\ \text{V}$, $V_{SS} = 0\ \text{V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (–) = $AV_{REFM} = 0\ \text{V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error ^{Note 1}	$AINL$	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}			1.2	± 5.0	LSB
					1.2	± 8.5 ^{Note 4}	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI22	$3.6\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$	2.125		39	μs
			$2.7\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$	3.1875		39	μs
			$1.8\ \text{V} \leq V_{DD} \leq 5.5\ \text{V}$	17		39	μs
				57		95	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 0.35	%FSR
						± 0.60 ^{Note 4}	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 0.35	%FSR
						± 0.60 ^{Note 4}	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 3.5	LSB
						± 6.0 ^{Note 4}	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 2.0	LSB
						± 2.5 ^{Note 4}	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI22		0		AV_{REFP} and V_{DD}	V

- Notes**
1. Excludes quantization error ($\pm 1/2$ LSB).
 2. This value is indicated as a ratio (%FSR) to the full-scale value.
 3. When $AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.
 Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
 Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 4. When the conversion time is set to $57\ \mu\text{s}$ (min.) and $95\ \mu\text{s}$ (max.).

LVD detection voltage of interrupt & reset mode**($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVD0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V _{LVD1}	LVIS1, LVIS0 = 1, 0	Rising reset release voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V _{LVD2}	LVIS1, LVIS0 = 0, 1	Rising reset release voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V _{LVD3}	LVIS1, LVIS0 = 0, 0	Rising reset release voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V _{LVD0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V _{LVD1}	LVIS1, LVIS0 = 1, 0	Rising reset release voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V _{LVD2}	LVIS1, LVIS0 = 0, 1	Rising reset release voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V _{LVD3}	LVIS1, LVIS0 = 0, 0	Rising reset release voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V _{LVD0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V _{LVD1}	LVIS1, LVIS0 = 1, 0	Rising reset release voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVD2}	LVIS1, LVIS0 = 0, 1	Rising reset release voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V _{LVD3}	LVIS1, LVIS0 = 0, 0	Rising reset release voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

2.6.5 Power supply voltage rising slope characteristics**($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S _{VDD}				54	V/ms

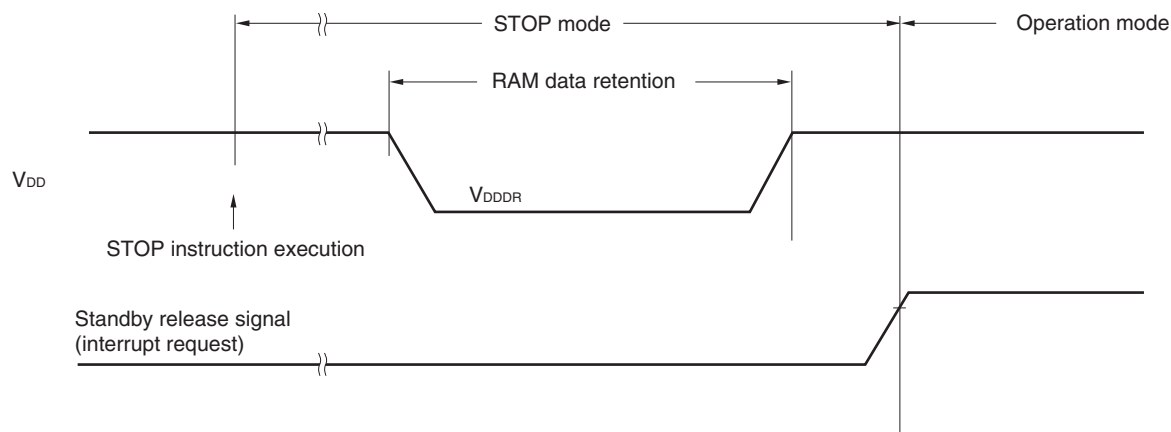
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 28.4 AC Characteristics.

<R> 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 ^{Note}		5.5	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



2.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

<R>	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	System clock frequency	f _{CLK}		1		24	MHz
	Code flash memory rewritable times <small>Notes 1, 2, 3</small>	C _{erwr}	Retained for 20 years T _A = 85°C	1,000			Times
	Data flash memory rewritable times <small>Notes 1, 2, 3</small>		Retained for 1 year T _A = 25°C		1,000,000		
			Retained for 5 years T _A = 85°C	100,000			
			Retained for 20 years T _A = 85°C	10,000			

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library
 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**(2/4)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	20-, 24-pin products: Per pin for P00 to P03 ^{Note 4} , P10 to P14, P40 to P42			8.5 ^{Note 2}	mA
		30-pin products: Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147				
		Per pin for P60, P61			15.0 ^{Note 2}	mA
		20-, 24-pin products: Total of P40 to P42	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		25.5	mA
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		9.0	mA
		30-pin products: Total of P00, P01, P40, P120 (When duty $\leq 70\%$ ^{Note 3})	$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$		1.8	mA
		20-, 24-pin products: Total of P00 to P03 ^{Note 4} , P10 to P14, P60, P61	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		40.0	mA
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		27.0	mA
		30-pin products: Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147 (When duty $\leq 70\%$ ^{Note 3})	$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$		5.4	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})			65.5	mA
	I _{OL2}	Per pin for P20 to P23			0.4	mA
		Total of all pins			1.6	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. The output current value under conditions where the duty factor $\leq 70\%$.

If duty factor $> 70\%$: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{OL} = 10.0\text{ mA}$

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. 24-pin products only.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) 30-pin products

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

(1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current ^{Note 1}	I_{DD1}	Operating mode	HS (High-speed main) mode ^{Note 4}	$f_{IH} = 24\text{ MHz}$ ^{Note 3}	Basic operation	$V_{DD} = 5.0\text{ V}$		1.5		mA
						$V_{DD} = 3.0\text{ V}$		1.5		
					Normal operation	$V_{DD} = 5.0\text{ V}$		3.7	5.8	mA
						$V_{DD} = 3.0\text{ V}$		3.7	5.8	
				$f_{IH} = 16\text{ MHz}$ ^{Note 3}		$V_{DD} = 5.0\text{ V}$		2.7	4.2	mA
						$V_{DD} = 3.0\text{ V}$		2.7	4.2	
				$f_{MX} = 20\text{ MHz}$ ^{Note 2} , $V_{DD} = 5.0\text{ V}$		Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	
				$f_{MX} = 20\text{ MHz}$ ^{Note 2} , $V_{DD} = 3.0\text{ V}$		Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	
				$f_{MX} = 10\text{ MHz}$ ^{Note 2} , $V_{DD} = 5.0\text{ V}$		Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	
				$f_{MX} = 10\text{ MHz}$ ^{Note 2} , $V_{DD} = 3.0\text{ V}$		Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	

Notes 1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.

3. When high-speed system clock is stopped

4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: $V_{DD} = 2.7\text{ V}$ to 5.5 V @ 1 MHz to 24 MHz

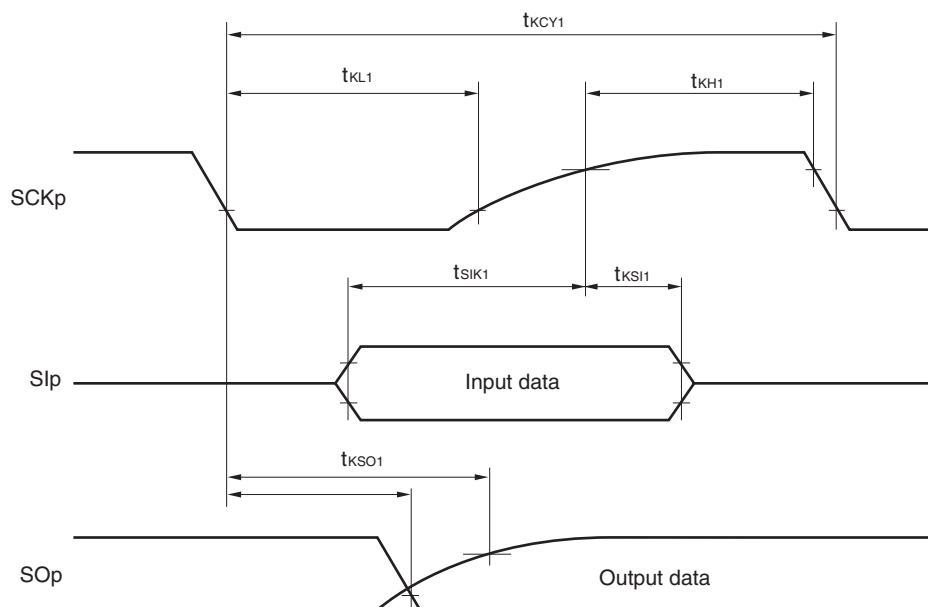
$V_{DD} = 2.4\text{ V}$ to 5.5 V @ 1 MHz to 16 MHz

Remarks 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

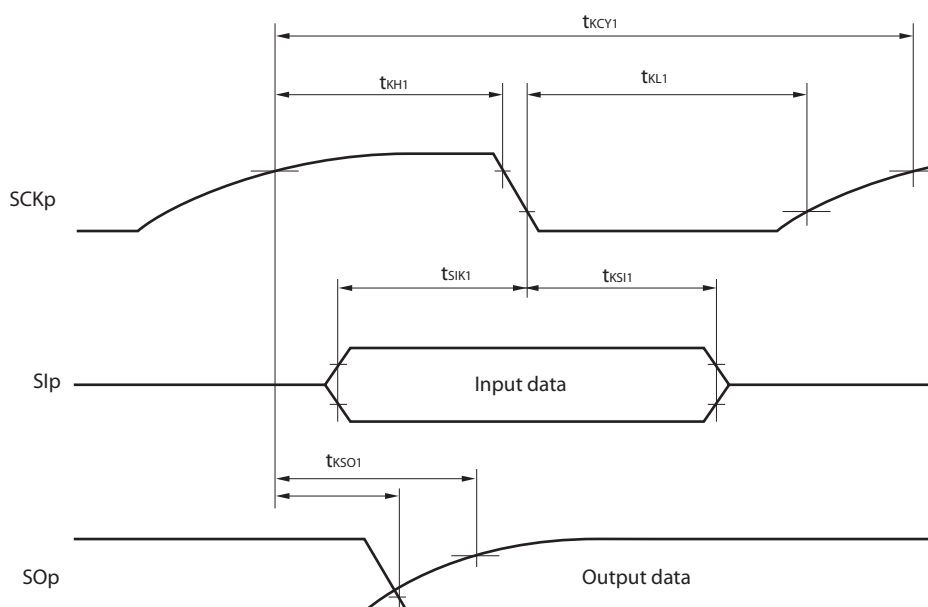
2. f_{IH} : high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (–) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI16 to ANI22

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (–) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}		1.2	± 5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI22	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}			± 0.35	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}			± 0.35	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}			± 3.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}			± 2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI22	0		AV_{REFP} and V_{DD}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

3.6.2 Temperature sensor/internal reference voltage characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

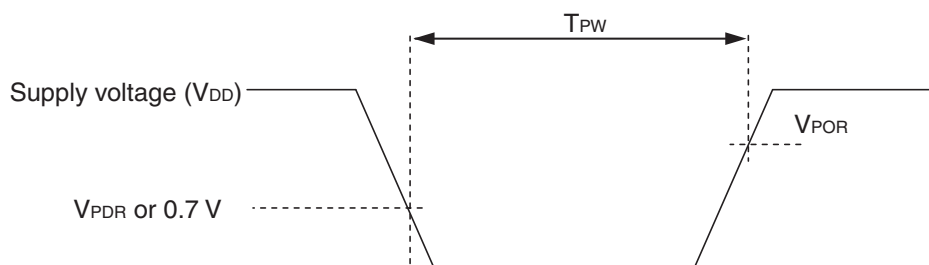
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F_{VTMS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/ $^\circ\text{C}$
Operation stabilization wait time	t_{AMP}		5			μs

3.6.3 POR circuit characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width ^{Note}	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).

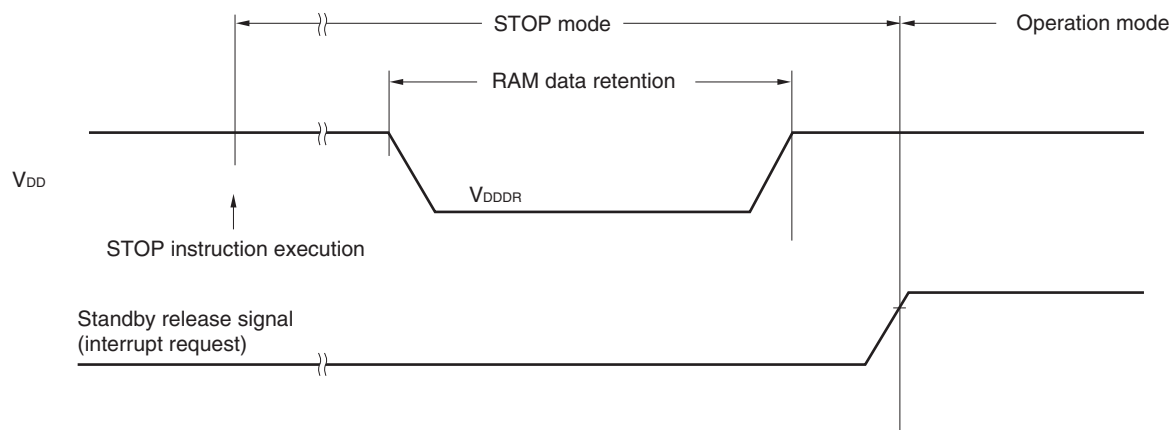


<R> 3.7 RAM Data Retention Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 ^{Note}		5.5	V

<R> Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		1		24	MHz
Code flash memory rewritable times <small>Notes 1, 2, 3</small>	C_{erwr}	Retained for 20 years $T_A = 85^\circ\text{C}$ <small>Notes 4</small>	1,000			Times
Data flash memory rewritable times <small>Notes 1, 2, 3</small>		Retained for 1 year $T_A = 25^\circ\text{C}$ <small>Notes 4</small>		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$ <small>Notes 4</small>	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$ <small>Notes 4</small>	10,000			

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library
 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
 4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

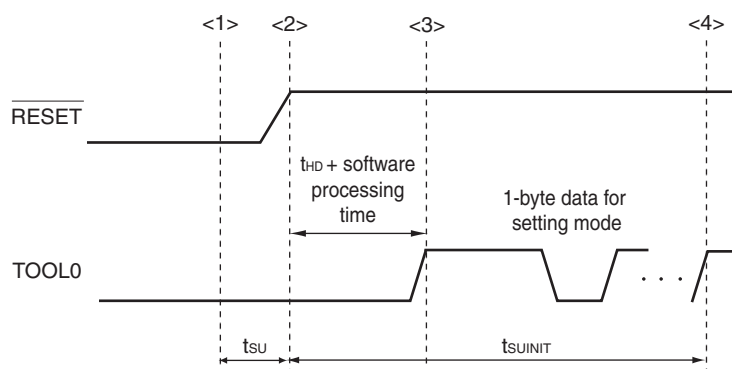
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUNIT}	POR and LVD reset are released before external release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset are released before external release	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset are released before external release	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUNIT} : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)