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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I <sup>2</sup> C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10269gsp-x5">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10269gsp-x5</a>

## <R> 2. ELECTRICAL SPECIFICATIONS ( $T_A = -40$ to $+85^\circ\text{C}$ )

<R> This chapter describes the following electrical specifications.

Target products A: Consumer applications  $T_A = -40$  to  $+85^\circ\text{C}$

<R> R5F102xxAxx, R5F103xxAxx

D: Industrial applications  $T_A = -40$  to  $+85^\circ\text{C}$

<R> R5F102xxDxx, R5F103xxDxx

G: Industrial applications when  $T_A = -40$  to  $+105^\circ\text{C}$  products is used in the range of  $T_A = -40$  to  $+85^\circ\text{C}$

<R> R5F102xxGxx

**Cautions** 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product.

## 2.2 Oscillator Characteristics

### 2.2.1 X1 oscillator characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency ( $f_x$ ) <sup>Note</sup>	Ceramic resonator / crystal oscillator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		8.0	

**Note** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

**Remark** When using the X1 oscillator, refer to **5.4 System Clock Oscillator**.

### 2.2.2 On-chip oscillator characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency <sup>Notes 1, 2</sup>	$f_{IH}$			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		R5F102 products	$T_A = -20$ to $+85^\circ\text{C}$	-1.0		+1.0	%
			$T_A = -40$ to $-20^\circ\text{C}$	-1.5		+1.5	%
		R5F103 products		-5.0		+5.0	%
Low-speed on-chip oscillator clock frequency	$f_{IL}$				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

**2.** This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

## (2) 30-pin products

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

(1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current <small>Note 1</small>	I <sub>DD1</sub>	Operating mode	HS (High-speed main) mode <small>Note 4</small>	f <sub>IH</sub> = 24 MHz <small>Note 3</small>	Basic operation	V <sub>DD</sub> = 5.0 V		1.5		mA
						V <sub>DD</sub> = 3.0 V		1.5		
					Normal operation	V <sub>DD</sub> = 5.0 V		3.7	5.5	mA
						V <sub>DD</sub> = 3.0 V		3.7	5.5	
				f <sub>IH</sub> = 16 MHz <small>Note 3</small>		V <sub>DD</sub> = 5.0 V		2.7	4.0	mA
						V <sub>DD</sub> = 3.0 V		2.7	4.0	
						V <sub>DD</sub> = 3.0 V		1.2	1.8	mA
						V <sub>DD</sub> = 2.0 V		1.2	1.8	
			HS (High-speed main) mode <small>Note 4</small>	f <sub>MX</sub> = 20 MHz <small>Note 2</small> , V <sub>DD</sub> = 5.0 V		Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
						Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f <sub>MX</sub> = 10 MHz <small>Note 2</small> , V <sub>DD</sub> = 5.0 V		Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
						Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
			LS (Low-speed main) mode <small>Note 4</small>	f <sub>MX</sub> = 8 MHz <small>Note 2</small> , V <sub>DD</sub> = 3.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f <sub>MX</sub> = 8 MHz <small>Note 2</small> , V <sub>DD</sub> = 2.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	

**Notes** 1. Total current flowing into V<sub>DD</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub> or V<sub>SS</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.

3. When high-speed system clock is stopped

4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V<sub>DD</sub> = 2.7 V to 5.5 V @ 1 MHz to 24 MHz

V<sub>DD</sub> = 2.4 V to 5.5 V @ 1 MHz to 16 MHz

LS(Low speed main) mode: V<sub>DD</sub> = 1.8 V to 5.5 V @ 1 MHz to 8 MHz

**Remarks** 1. f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f<sub>IH</sub>: high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T<sub>A</sub> = 25°C.

## (2) 30-pin products

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note 1</sup>	I <sub>DD2</sub> <sup>Note 2</sup>	HALT mode	HS (High-speed main) mode <sup>Note 6</sup>	f <sub>IH</sub> = 24 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		440	1280	μA	
					V <sub>DD</sub> = 3.0 V		440	1280		
				f <sub>IH</sub> = 16 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		400	1000	μA	
					V <sub>DD</sub> = 3.0 V		400	1000		
			LS (Low-speed main) mode <sup>Note 6</sup>	f <sub>IH</sub> = 8 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 3.0 V		260	530	μA	
					V <sub>DD</sub> = 2.0 V		260	530		
			HS (High-speed main) mode <sup>Note 6</sup>	f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		280	1000	μA	
					Resonator connection		450	1170		
				f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		280	1000	μA	
					Resonator connection		450	1170		
				f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		190	600	μA	
					Resonator connection		260	670		
				f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		190	600	μA	
					Resonator connection		260	670		
			LS (Low-speed main) mode <sup>Note 6</sup>	f <sub>MX</sub> = 8 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380		
				f <sub>MX</sub> = 8 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 2.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380		
	I <sub>DD3</sub> <sup>Note 5</sup>	STOP mode	T <sub>A</sub> = −40°C					0.18	0.50	μA
			T <sub>A</sub> = +25°C					0.23	0.50	
			T <sub>A</sub> = +50°C					0.30	1.10	
			T <sub>A</sub> = +70°C					0.46	1.90	
			T <sub>A</sub> = +85°C					0.75	3.30	

**Notes** 1. Total current flowing into V<sub>DD</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub> or V<sub>SS</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator clock is stopped.

4. When high-speed system clock is stopped.

5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: V<sub>DD</sub> = 2.7 V to 5.5 V @ 1 MHz to 24 MHz

V<sub>DD</sub> = 2.4 V to 5.5 V @ 1 MHz to 16 MHz

LS (Low speed main) mode: V<sub>DD</sub> = 1.8 V to 5.5 V @ 1 MHz to 8 MHz

**Remarks** 1. f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f<sub>IH</sub>: high-speed on-chip oscillator clock frequency

3. Except STOP mode, temperature condition of the TYP. value is T<sub>A</sub> = 25°C.

**(3) Peripheral functions (Common to all products)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed onchip oscillator operating current	I <sub>FIL</sub> <sup>Note 1</sup>				0.20		μA
12-bit interval timer operating current	I <sub>TMKA</sub> <sup>Notes 1, 2, 3</sup>				0.02		μA
Watchdog timer operating current	I <sub>WDT</sub> <sup>Notes 1, 2, 4</sup>	f <sub>IL</sub> = 15 kHz			0.22		μA
A/D converter operating current	I <sub>ADC</sub> <sup>Notes 1, 5</sup>	When conversion at maximum speed	Normal mode, AV <sub>REFP</sub> = V <sub>DD</sub> = 5.0 V		1.30	1.70	mA
			Low voltage mode, AV <sub>REFP</sub> = V <sub>DD</sub> = 3.0 V		0.50	0.70	mA
A/D converter reference voltage operating current	I <sub>ADREF</sub> <sup>Note 1</sup>				75.0		μA
Temperature sensor operating current	I <sub>TMPS</sub> <sup>Note 1</sup>				75.0		μA
LVD operating current	I <sub>LVD</sub> <sup>Notes 1, 6</sup>				0.08		μA
Self-programming operating current	I <sub>FSP</sub> <sup>Notes 1, 8</sup>				2.00	12.20	mA
BGO operating current	I <sub>BGO</sub> <sup>Notes 1, 7</sup>				2.00	12.20	mA
SNOOZE operating current	I <sub>SNOZ</sub> <sup>Note 1</sup>	ADC operation	The mode is performed <sup>Note 9</sup>		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV <sub>REFP</sub> = V <sub>DD</sub> = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

**Notes** 1. Current flowing to the V<sub>DD</sub>.

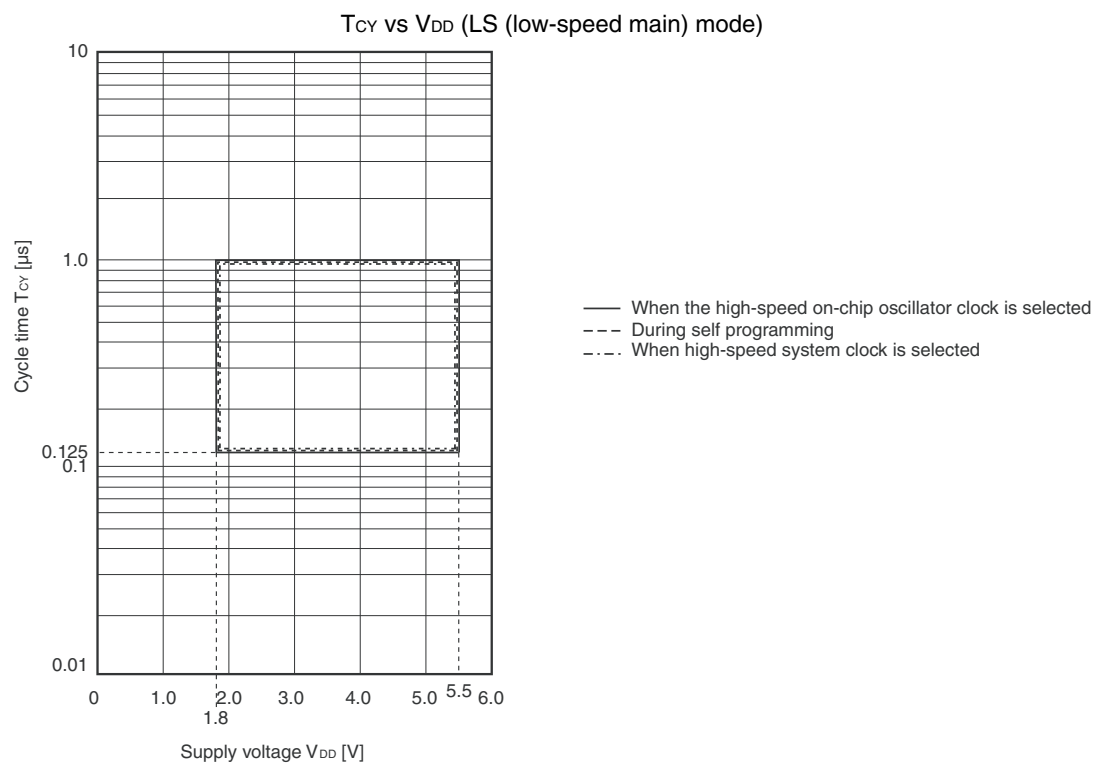
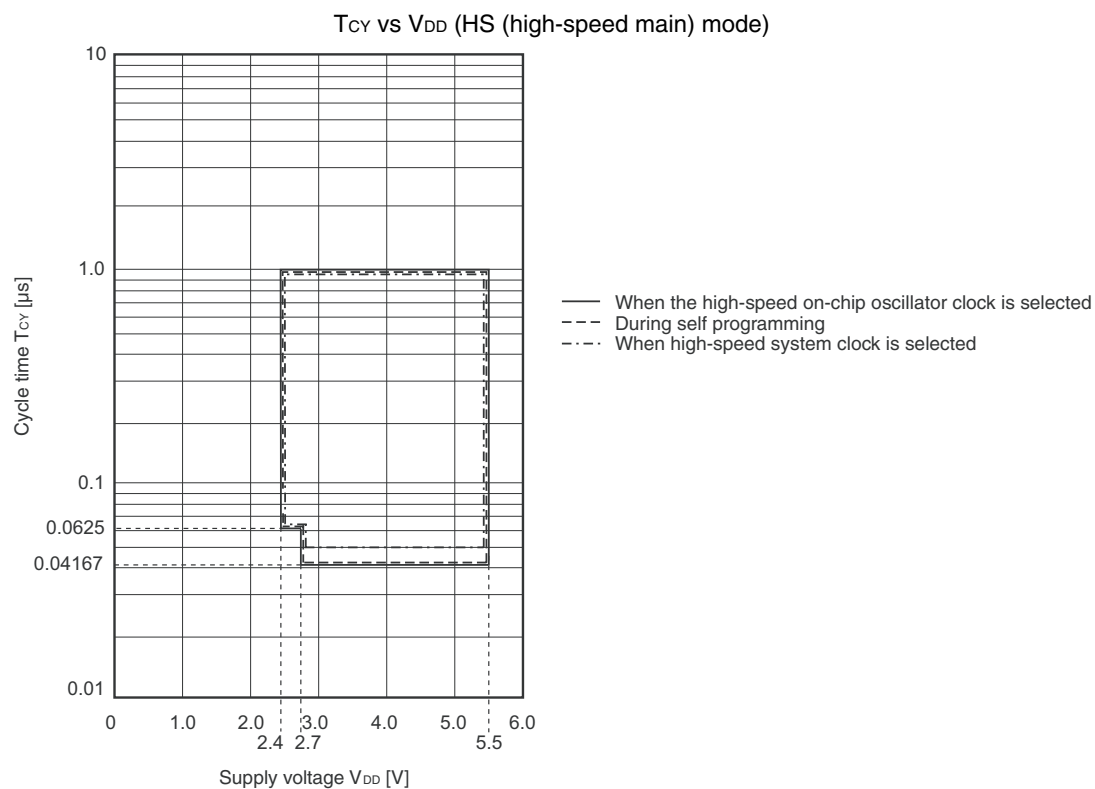
2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I<sub>DD1</sub>, I<sub>DD2</sub> or I<sub>DD3</sub>, and I<sub>FIL</sub> and I<sub>TMKA</sub> when the 12-bit interval timer operates.4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I<sub>DD1</sub>, I<sub>DD2</sub> or I<sub>DD3</sub> and I<sub>WDT</sub> when the watchdog timer operates.5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I<sub>DD1</sub> or I<sub>DD2</sub> and I<sub>ADC</sub> when the A/D converter operates in an operation mode or the HALT mode.6. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I<sub>DD1</sub>, I<sub>DD2</sub> or I<sub>DD3</sub> and I<sub>LVD</sub> when the LVD circuit operates.

7. Current flowing only during data flash rewrite.

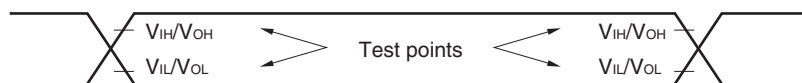
8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.**Remarks** 1. f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency2. Temperature condition of the TYP. value is T<sub>A</sub> = 25°C

**Minimum Instruction Execution Time during Main System Clock Operation**

## 2.5 Peripheral Functions Characteristics

### AC Timing Test Point



### 2.5.1 Serial array unit

#### (1) During communication at same potential (UART mode)

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate				$f_{MCK}/6$		$f_{MCK}/6$	bps
Note 1		Theoretical value of the maximum transfer rate $f_{CLK} = f_{MCK}$ <sup>Note2</sup>		4.0		1.3	Mbps

**Notes** 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock ( $f_{CLK}$ ) are:

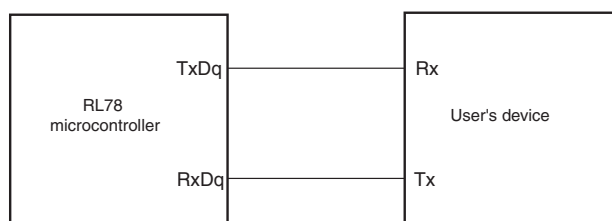
HS (high-speed main) mode: 24 MHz ( $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

16 MHz ( $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

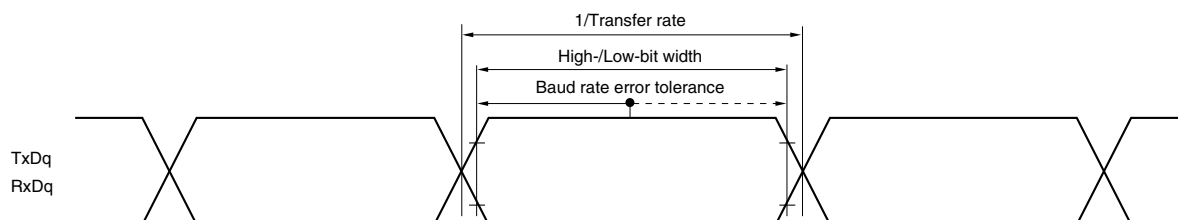
LS (low-speed main) mode: 8 MHz ( $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

#### UART mode connection diagram (during communication at same potential)



#### UART mode bit width (during communication at same potential) (reference)



**Remarks** 1. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

2.  $f_{MCK}$ : Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

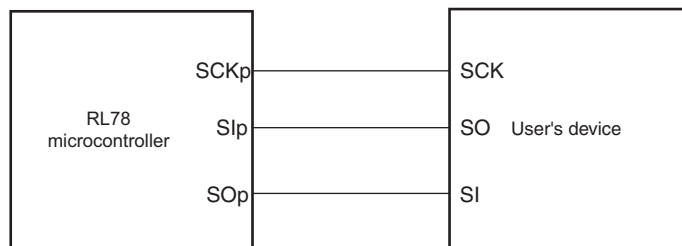
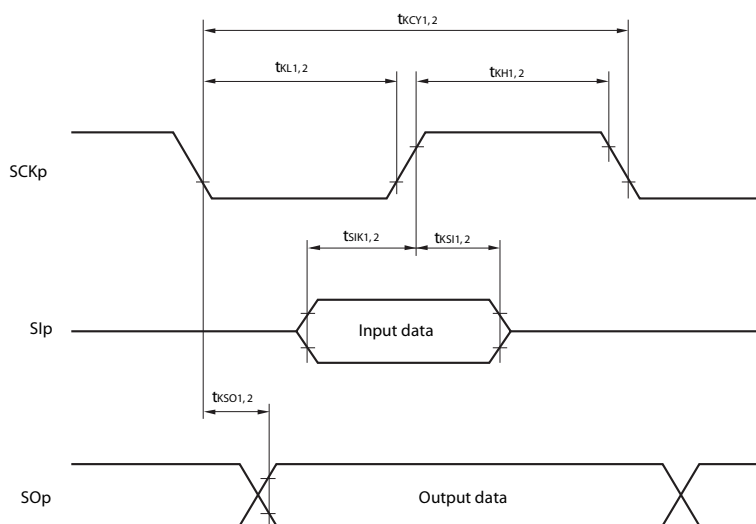
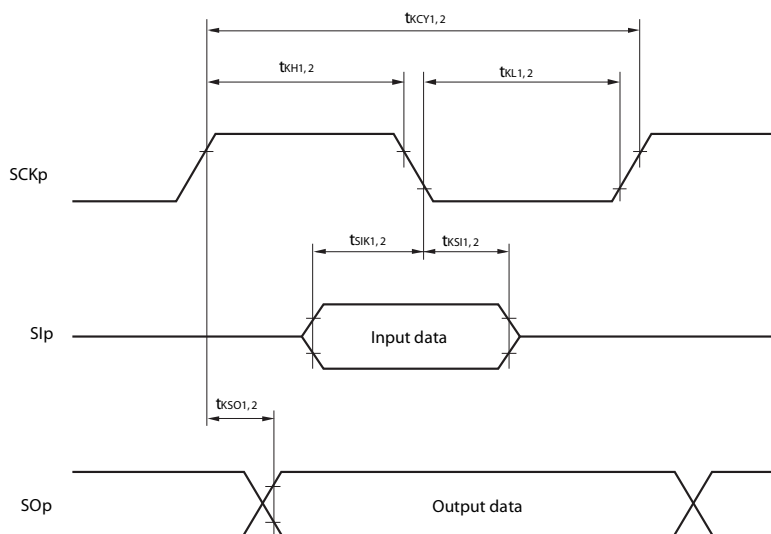


**(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)****( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time <sup>Note 4</sup>	$t_{KCY2}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$20\text{ MHz} < f_{MCK}$	$8/f_{MCK}$		—		ns
			$f_{MCK} \leq 20\text{ MHz}$	$6/f_{MCK}$		$6/f_{MCK}$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$16\text{ MHz} < f_{MCK}$	$8/f_{MCK}$		—		ns
			$f_{MCK} \leq 16\text{ MHz}$	$6/f_{MCK}$		$6/f_{MCK}$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$6/f_{MCK}$ and 500		$6/f_{MCK}$ and 500		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		$6/f_{MCK}$ and 750		ns
SCKp high-/low-level width	$t_{KH2}$ , $t_{KL2}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-7$		$t_{KCY2}/2-7$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-8$		$t_{KCY2}/2-8$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-18$		$t_{KCY2}/2-18$		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		$t_{KCY2}/2-18$		ns
Slp setup time (to SCKp $\uparrow$ ) <sup>Note 1</sup>	$t_{SIK2}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 20$		$1/f_{MCK} + 30$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 30$		$1/f_{MCK} + 30$		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		$1/f_{MCK} + 30$		ns
Slp hold time (from SCKp $\uparrow$ ) <sup>Note 2</sup>	$t_{KSI2}$			$1/f_{MCK} + 31$		$1/f_{MCK} + 31$		ns
Delay time from SCKp $\downarrow$ to SOp output <sup>Note 3</sup>	$t_{KSO2}$	$C = 30\text{ pF}$ <sup>Note 4</sup>	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$2/f_{MCK} + 44$		$2/f_{MCK} + 110$	ns
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$2/f_{MCK} + 75$		$2/f_{MCK} + 110$	ns
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		$2/f_{MCK} + 110$	ns

- Notes**
1. When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The Slp setup time becomes “to SCKp $\downarrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
  2. When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The Slp hold time becomes “from SCKp $\downarrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
  3. When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The delay time to SOp output becomes “from SCKp $\uparrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
  4. C is the load capacitance of the SOp output lines.
  5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Caution** Select the normal input buffer for the Slp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

**CSI mode connection diagram (during communication at same potential)**
**CSI mode serial transfer timing (during communication at same potential)**  
 (When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ .)

**CSI mode serial transfer timing (during communication at same potential)**  
 (When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .)


(Remarks are listed on the next page.)

**(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)****( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCK00 cycle time	$t_{KCY1}$	$t_{KCY1} \geq 2/f_{CLK}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	200		1150		ns
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	300		1150		ns
SCK00 high-level width	$t_{KH1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		ns
SCK00 low-level width	$t_{KL1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$		$t_{KCY1}/2 - 7$		$t_{KCY1}/2 - 50$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		$t_{KCY1}/2 - 10$		$t_{KCY1}/2 - 50$		ns
SI00 setup time (to SCK00 $\uparrow$ ) <sup>Note 1</sup>	$t_{SIK1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$		58		479		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		121		479		ns
SI00 hold time (from SCK00 $\uparrow$ ) <sup>Note 1</sup>	$t_{KSI1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$		10		10		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		10		10		ns
Delay time from SCK00 $\downarrow$ to SO00 output <sup>Note 1</sup>	$t_{KSO1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$			60		60	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$			130		130	ns
SI00 setup time (to SCK00 $\downarrow$ ) <sup>Note 2</sup>	$t_{SIK1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$		23		110		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		33		110		ns
SI00 hold time (from SCK00 $\downarrow$ ) <sup>Note 2</sup>	$t_{KSI1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$		10		10		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		10		10		ns
Delay time from SCK00 $\uparrow$ to SO00 output <sup>Note 2</sup>	$t_{KSO1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$			10		10	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$			10		10	ns

(Notes, Caution, and Remarks are listed on the next page.)

## 2.6.4 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode**(T<sub>A</sub> = -40 to +85°C, V<sub>PDR</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	V <sub>LVD0</sub>	Power supply rise time	3.98	4.06	4.14	V
		Power supply fall time	3.90	3.98	4.06	V
	V <sub>LVD1</sub>	Power supply rise time	3.68	3.75	3.82	V
		Power supply fall time	3.60	3.67	3.74	V
	V <sub>LVD2</sub>	Power supply rise time	3.07	3.13	3.19	V
		Power supply fall time	3.00	3.06	3.12	V
	V <sub>LVD3</sub>	Power supply rise time	2.96	3.02	3.08	V
		Power supply fall time	2.90	2.96	3.02	V
	V <sub>LVD4</sub>	Power supply rise time	2.86	2.92	2.97	V
		Power supply fall time	2.80	2.86	2.91	V
	V <sub>LVD5</sub>	Power supply rise time	2.76	2.81	2.87	V
		Power supply fall time	2.70	2.75	2.81	V
	V <sub>LVD6</sub>	Power supply rise time	2.66	2.71	2.76	V
		Power supply fall time	2.60	2.65	2.70	V
	V <sub>LVD7</sub>	Power supply rise time	2.56	2.61	2.66	V
		Power supply fall time	2.50	2.55	2.60	V
	V <sub>LVD8</sub>	Power supply rise time	2.45	2.50	2.55	V
		Power supply fall time	2.40	2.45	2.50	V
	V <sub>LVD9</sub>	Power supply rise time	2.05	2.09	2.13	V
		Power supply fall time	2.00	2.04	2.08	V
	V <sub>LVD10</sub>	Power supply rise time	1.94	1.98	2.02	V
		Power supply fall time	1.90	1.94	1.98	V
	V <sub>LVD11</sub>	Power supply rise time	1.84	1.88	1.91	V
		Power supply fall time	1.80	1.84	1.87	V
Minimum pulse width	t <sub>LW</sub>		300			μs
Detection delay time					300	μs

## 3.1 Absolute Maximum Ratings

Absolute Maximum Ratings ( $T_A = 25^{\circ}\text{C}$ )

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	$V_{DD}$			$-0.5$ to $+6.5$	V
REGC terminal input voltage <sup>Note 1</sup>	$V_{IREGC}$	REGC		$-0.3$ to $+2.8$ and $-0.3$ to $V_{DD} + 0.3$ <sup>Note 2</sup>	V
Input Voltage	$V_{I1}$	Other than P60, P61		$-0.3$ to $V_{DD} + 0.3$ <sup>Note 3</sup>	V
	$V_{I2}$	P60, P61 (N-ch open drain)		$-0.3$ to $6.5$	V
Output Voltage	$V_O$			$-0.3$ to $V_{DD} + 0.3$ <sup>Note 3</sup>	V
Analog input voltage	$V_{AI}$	20, 24-pin products: ANI0 to ANI3, ANI16 to ANI22 30-pin products: ANI0 to ANI3, ANI16 to ANI19		$-0.3$ to $V_{DD} + 0.3$ and $-0.3$ to $AVREF(+)+0.3$ <sup>Notes 3, 4</sup>	V
Output current, high	$I_{OH1}$	Per pin	Other than P20 to P23	$-40$	mA
		Total of all pins	All the terminals other than P20 to P23	$-170$	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	$-70$	mA
			20-, 24-pin products: P00 to P03 <sup>Note 5</sup> , P10 to P14 30-pin products: P10 to P17, P30, P31, P50, P51, P147	$-100$	mA
	$I_{OH2}$	Per pin	P20 to P23	$-0.5$	mA
		Total of all pins		$-2$	mA
Output current, low	$I_{OL1}$	Per pin	Other than P20 to P23	$40$	mA
		Total of all pins	All the terminals other than P20 to P23	$170$	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	$70$	mA
			20-, 24-pin products: P00 to P03 <sup>Note 5</sup> , P10 to P14, P60, P61 30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147	$100$	mA
	$I_{OL2}$	Per pin	P20 to P23	$1$	mA
		Total of all pins		$5$	mA
Operating ambient temperature	$T_A$			$-40$ to $+105$	$^{\circ}\text{C}$
Storage temperature	$T_{stg}$			$-65$ to $+150$	$^{\circ}\text{C}$

**Notes** 1. 30-pin product only.

2. Connect the REGC pin to  $V_{SS}$  via a capacitor (0.47 to 1  $\mu\text{F}$ ). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.

3. Must be 6.5 V or lower.

4. Do not exceed  $AVREF(+) + 0.3$  V in case of A/D conversion target pin.

5. 24-pin products only.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks** 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.  $AVREF(+)$  : + side reference voltage of the A/D converter.

3.  $V_{SS}$  : Reference voltage

## 3.3 DC Characteristics

## 3.3.1 Pin characteristics

(T<sub>A</sub> = -40 to +105°C, 2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

(1/4)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high <sup>Note 1</sup>	I <sub>OH1</sub>	20-, 24-pin products: Per pin for P00 to P03 <sup>Note 4</sup> , P10 to P14, P40 to P42  30-pin products: Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147			-3.0 <sup>Note 2</sup>	mA
		20-, 24-pin products: Total of P40 to P42	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V		-9.0	mA
			2.7 V ≤ V <sub>DD</sub> < 4.0 V		-6.0	mA
		30-pin products: Total of P00, P01, P40, P120 (When duty ≤ 70% <sup>Note 3</sup> )	2.4 V ≤ V <sub>DD</sub> < 2.7 V		-4.5	mA
		20-, 24-pin products: Total of P00 to P03 <sup>Note 4</sup> , P10 to P14	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V		-27.0	mA
			2.7 V ≤ V <sub>DD</sub> < 4.0 V		-18.0	mA
		30-pin products: Total of P10 to P17, P30, P31, P50, P51, P147 (When duty ≤ 70% <sup>Note 3</sup> )	2.4 V ≤ V <sub>DD</sub> < 2.7 V		-10.0	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )			-36.0	mA
	I <sub>OH2</sub>	Per pin for P20 to P23			-0.1	mA
		Total of all pins			-0.4	mA

**Notes** 1. value of current at which the device operation is guaranteed even if the current flows from the V<sub>DD</sub> pin to an output pin.

2. However, do not exceed the total current value.

3. The output current value under conditions where the duty factor ≤ 70%.

If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = (I<sub>OH</sub> × 0.7)/(n × 0.01)

<Example> Where n = 80% and I<sub>OH</sub> = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. 24-pin products only.

**Caution** P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## (1) 20-, 24-pin products

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V})$ 

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current <sup>Note 1</sup>	I <sub>DD2</sub> <sup>Note 2</sup>	HALT mode	HS (High-speed main) mode <sup>Note 6</sup>	f <sub>IH</sub> = 24 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		440	2230	μA
					V <sub>DD</sub> = 3.0 V		440	2230	
				f <sub>IH</sub> = 16 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		400	1650	μA
					V <sub>DD</sub> = 3.0 V		400	1650	
				f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		190	1010	μA
					Resonator connection		260	1090	
				f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		190	1010	μA
					Resonator connection		260	1090	
I <sub>DD3</sub> <sup>Note 5</sup>	STOP mode	T <sub>A</sub> = −40°C					0.19	0.50	μA
		T <sub>A</sub> = +25°C					0.24	0.50	
		T <sub>A</sub> = +50°C					0.32	0.80	
		T <sub>A</sub> = +70°C					0.48	1.20	
		T <sub>A</sub> = +85°C					0.74	2.20	
		T <sub>A</sub> = +105°C					1.50	10.20	

- Notes**
1. Total current flowing into  $V_{DD}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$  or  $V_{SS}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator clock is stopped.
  4. When high-speed system clock is stopped.
  5. Not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode:  $V_{DD} = 2.7\text{ V}$  to  $5.5\text{ V}$  @  $1\text{ MHz}$  to  $24\text{ MHz}$

$V_{DD} = 2.4\text{ V}$  to  $5.5\text{ V}$  @  $1\text{ MHz}$  to  $16\text{ MHz}$

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : high-speed on-chip oscillator clock frequency
  3. Except temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$ , other than STOP mode

**(3) Peripheral functions (Common to all products)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed onchip oscillator operating current	$I_{FIL}$ <sup>Note 1</sup>				0.20		$\mu\text{A}$
12-bit interval timer operating current	$I_{TMKA}$ <sup>Notes 1, 2, 3</sup>				0.02		$\mu\text{A}$
Watchdog timer operating current	$I_{WDT}$ <sup>Notes 1, 2, 4</sup>	$f_{IL} = 15\text{ kHz}$			0.22		$\mu\text{A}$
A/D converter operating current	$I_{ADC}$ <sup>Notes 1, 5</sup>	When conversion at maximum speed	Normal mode, $AV_{REFP} = V_{DD} = 5.0\text{ V}$		1.30	1.70	mA
			Low voltage mode, $AV_{REFP} = V_{DD} = 3.0\text{ V}$		0.50	0.70	mA
A/D converter reference voltage operating current	$I_{ADREF}$ <sup>Note 1</sup>				75.0		$\mu\text{A}$
Temperature sensor operating current	$I_{TMPS}$ <sup>Note 1</sup>				75.0		$\mu\text{A}$
LVD operating current	$I_{LVD}$ <sup>Notes 1, 6</sup>				0.08		$\mu\text{A}$
Self-programming operating current	$I_{FSP}$ <sup>Notes 1, 8</sup>				2.00	12.20	mA
BGO operating current	$I_{BGO}$ <sup>Notes 1, 7</sup>				2.00	12.20	mA
SNOOZE operating current	$I_{SNOZ}$ <sup>Note 1</sup>	ADC operation	The mode is performed <sup>Note 9</sup>		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, $AV_{REFP} = V_{DD} = 3.0\text{ V}$		1.20	2.04	mA
		CSI/UART operation			0.70	1.54	mA

**Notes** 1. Current flowing to the  $V_{DD}$ .

2. When high speed on-chip oscillator and high-speed system clock are stopped.

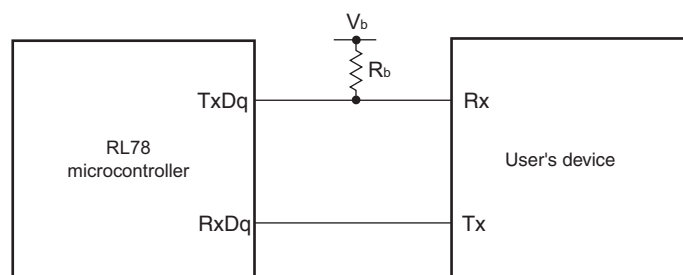
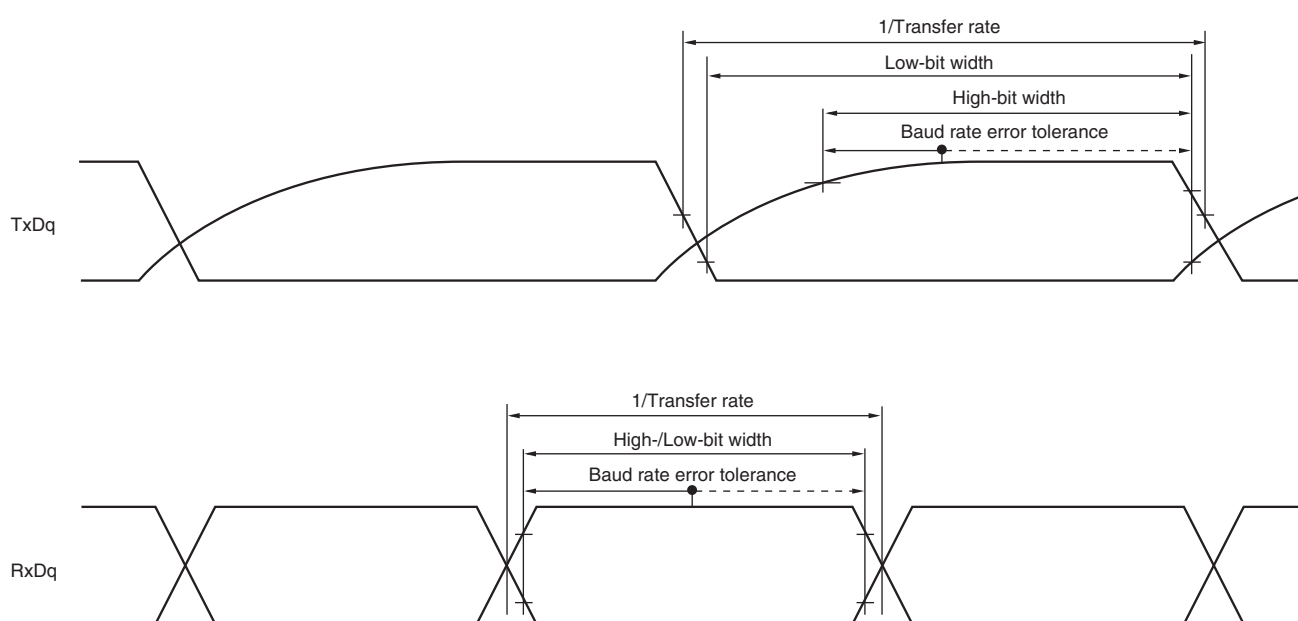
3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$ , and  $I_{FIL}$  and  $I_{TMKA}$  when the 12-bit interval timer operates.4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$  and  $I_{WDT}$  when the watchdog timer operates.5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of  $I_{DD1}$  or  $I_{DD2}$  and  $I_{ADC}$  when the A/D converter operates in an operation mode or the HALT mode.6. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$  and  $I_{LVD}$  when the LVD circuit operates.

7. Current flowing only during data flash rewrite.

8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.**Remarks** 1.  $f_{IL}$ : Low-speed on-chip oscillator clock frequency2. Temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$



**UART mode connection diagram (during communication at different potential)****UART mode bit width (during communication at different potential) (reference)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  $C_b[\text{F}]$ : Communication line (TxDq) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)
  3.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))
  4. UART0 of the 20- and 24-pin products supports communication at different potential only when the peripheral I/O redirection function is not used.

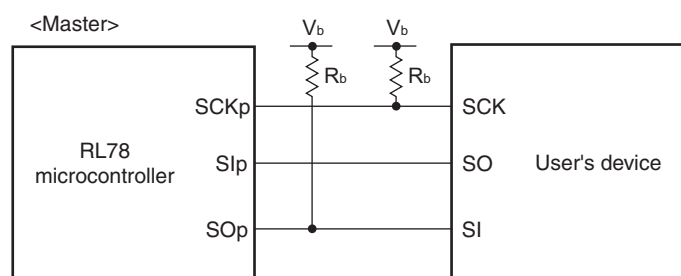
**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↓) <small>Note</small>	$t_{SIK1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	88		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	88		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	220		ns
Slp hold time (from SCKp↓) <small>Note</small>	$t_{KSI1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp↑ to SO <sub>p</sub> output <small>Note</small>	$t_{KSO1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$		50	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		50	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$		50	ns

**Note** When  $DAP_{mn} = 0$  and  $CKP_{mn} = 1$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 0$ .

- Cautions 1.** Select the TTL input buffer for the Slp pin and the N-ch open drain output ( $V_{DD}$  tolerance) mode for the SO<sub>p</sub> pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.
- 2.** CSI01 and CSI11 cannot communicate at different potential.

- Remarks 1.**  $R_b$  [ $\Omega$ ]: Communication line (SCKp, SO<sub>p</sub>) pull-up resistance,  $C_b$  [F]: Communication line (SCKp, SO<sub>p</sub>) load capacitance,  $V_b$  [V]: Communication line voltage
- 2.** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

**CSI mode connection diagram (during communication at different potential)**

## 3.6.4 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{PDR} \leq V_{DD} \leq 5.5$  V,  $V_{SS} = 0$  V)**

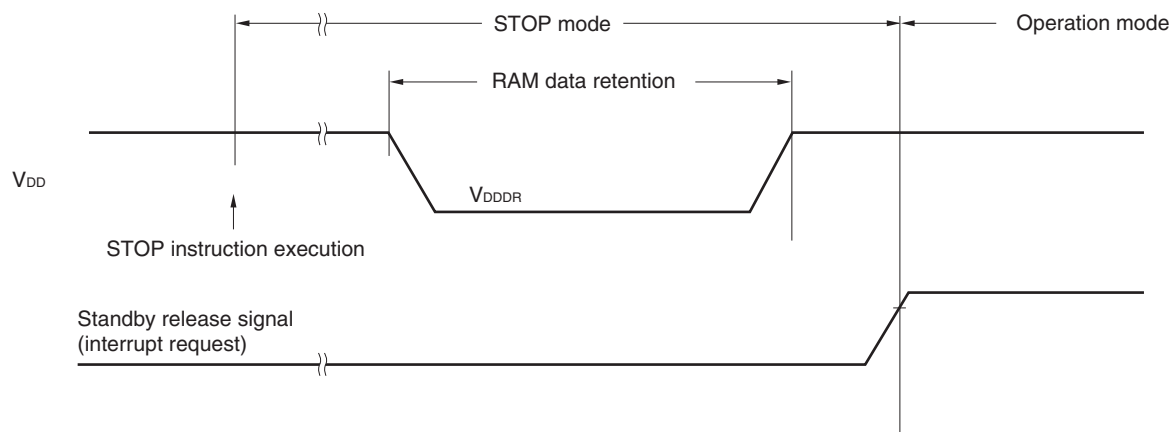
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	$V_{LVD0}$	Power supply rise time	3.90	4.06	4.22	V
		Power supply fall time	3.83	3.98	4.13	V
	$V_{LVD1}$	Power supply rise time	3.60	3.75	3.90	V
		Power supply fall time	3.53	3.67	3.81	V
	$V_{LVD2}$	Power supply rise time	3.01	3.13	3.25	V
		Power supply fall time	2.94	3.06	3.18	V
	$V_{LVD3}$	Power supply rise time	2.90	3.02	3.14	V
		Power supply fall time	2.85	2.96	3.07	V
	$V_{LVD4}$	Power supply rise time	2.81	2.92	3.03	V
		Power supply fall time	2.75	2.86	2.97	V
	$V_{LVD5}$	Power supply rise time	2.70	2.81	2.92	V
		Power supply fall time	2.64	2.75	2.86	V
	$V_{LVD6}$	Power supply rise time	2.61	2.71	2.81	V
		Power supply fall time	2.55	2.65	2.75	V
	$V_{LVD7}$	Power supply rise time	2.51	2.61	2.71	V
		Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width	$t_{LW}$		300			$\mu\text{s}$
Detection delay time					300	$\mu\text{s}$

## &lt;R&gt; 3.7 RAM Data Retention Characteristics

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	$V_{DDDR}$		1.44 <sup>Note</sup>		5.5	V

<R> Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



## 3.8 Flash Memory Programming Characteristics

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	$f_{CLK}$		1		24	MHz
Code flash memory rewritable times <small>Notes 1, 2, 3</small>	$C_{erwr}$	Retained for 20 years $T_A = 85^\circ\text{C}$ <sup>Notes 4</sup>	1,000			Times
Data flash memory rewritable times <small>Notes 1, 2, 3</small>		Retained for 1 year $T_A = 25^\circ\text{C}$ <sup>Notes 4</sup>		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$ <sup>Notes 4</sup>	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$ <sup>Notes 4</sup>	10,000			

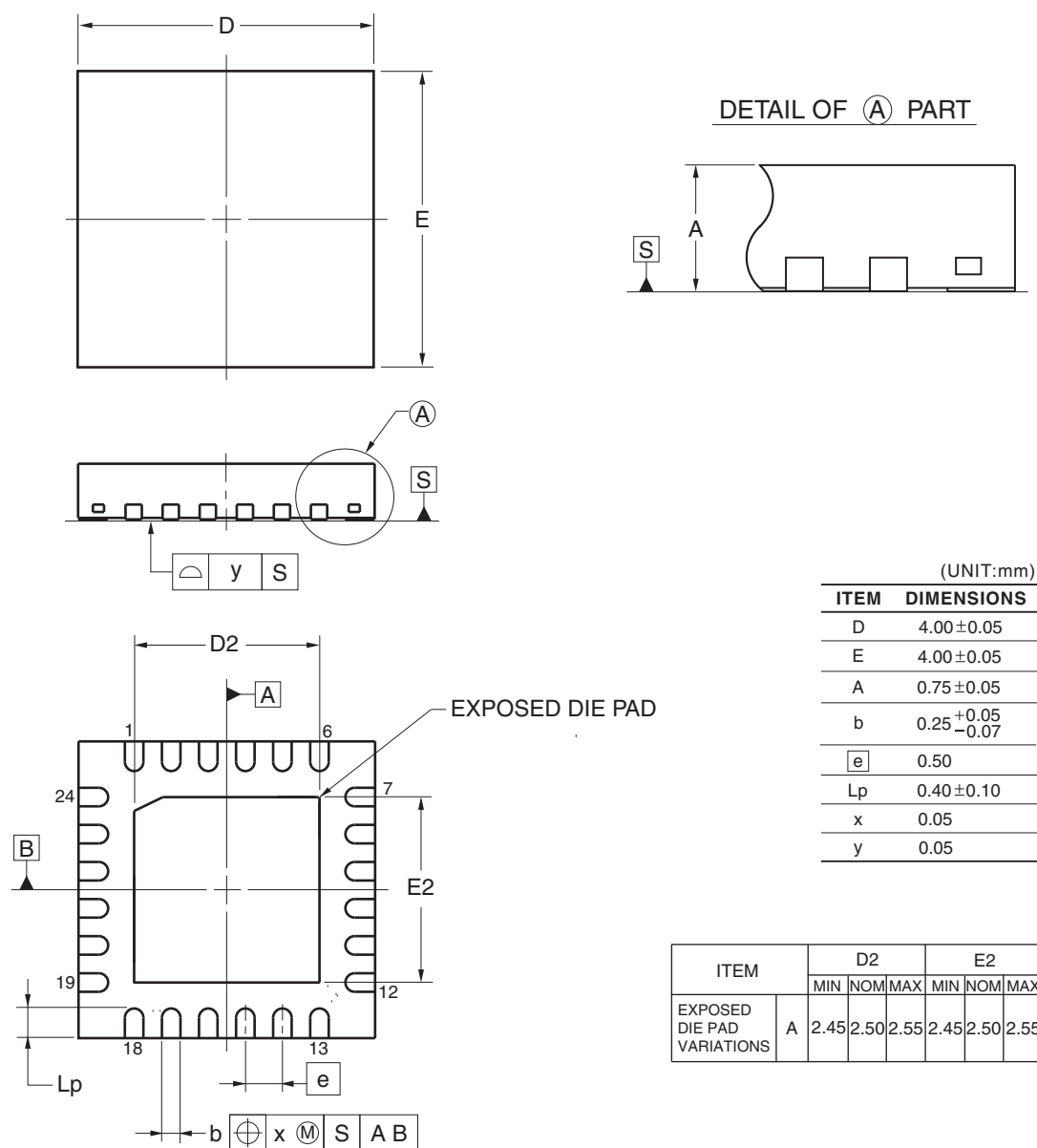
- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
  2. When using flash memory programmer and Renesas Electronics self programming library
  3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
  4. This temperature is the average value at which data are retained.

## 4.2 24-pin products

R5F1027AANA, R5F10279ANA, R5F10278ANA, R5F10277ANA  
 R5F1037AANA, R5F10379ANA, R5F10378ANA, R5F10377ANA  
 R5F1027ADNA, R5F10279DNA, R5F10278DNA, R5F10277DNA  
 R5F1037ADNA, R5F10379DNA, R5F10378DNA, R5F10377DNA  
 R5F1027AGNA, R5F10279GNA, R5F10278GNA, R5F10277GNA

&lt;R&gt;

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN24-4x4-0.50	PWQN0024KE-A	P24K8-50-CAB-1	0.04



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