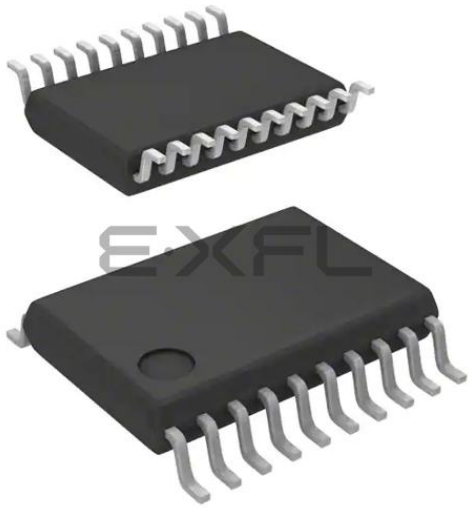

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1026agsp-v0

1.3.2 On-chip oscillator characteristics

(1) High-speed on-chip oscillator oscillation frequency of the R5F102 products

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = -20 to +85 °C	-1.0	+1.0	%
	T_A = -40 to -20 °C	-1.5	+1.5	
	T_A = +85 to +105 °C	-2.0	+2.0	

(2) High-speed on-chip oscillator oscillation frequency of the R5F103 products

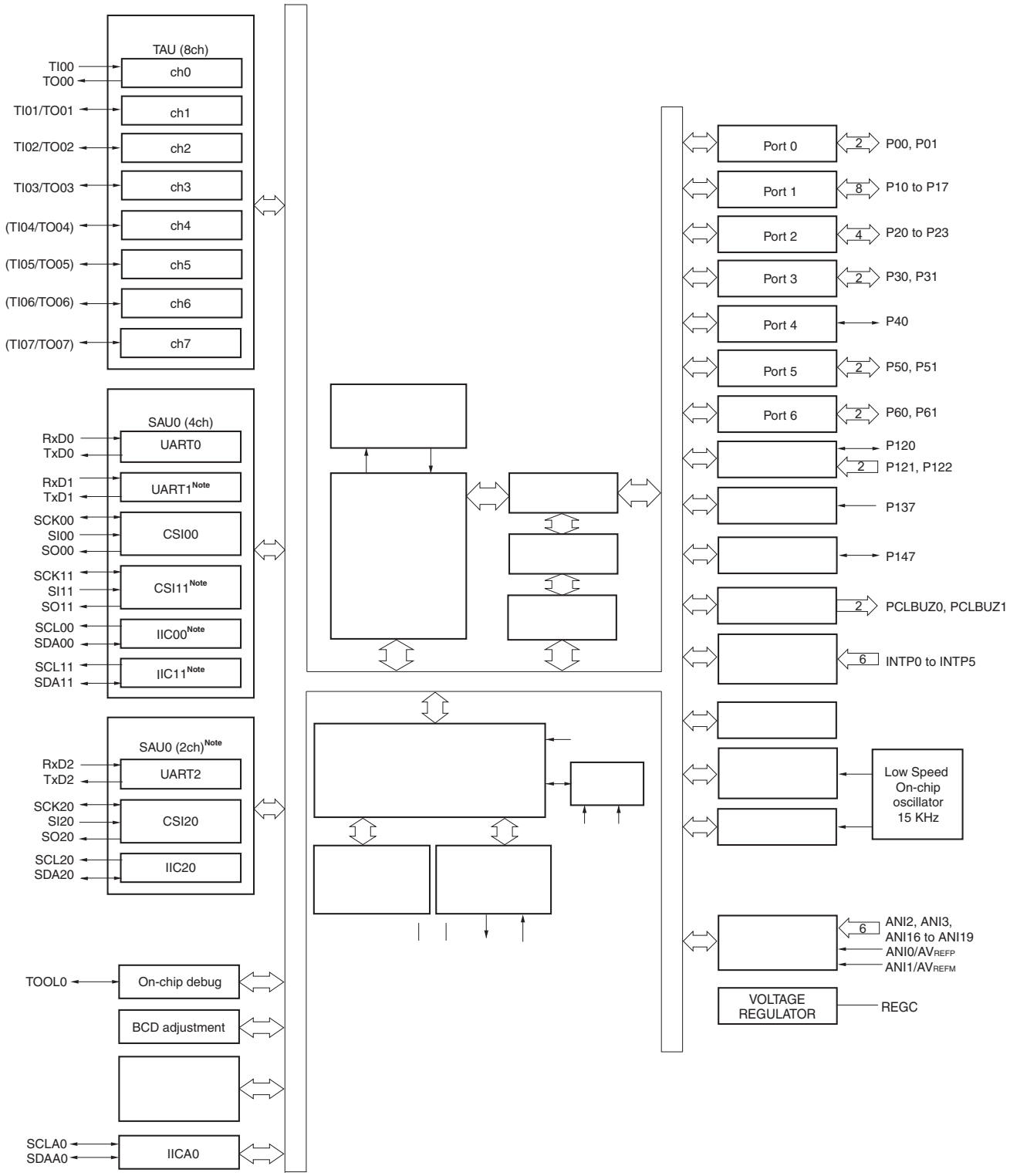
Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = -40 to + 85 °C	-5.0	+5.0	%

1.3.3 Peripheral Functions

The following are differences in peripheral functions between the R5F102 products and the R5F103 products.

RL78/G12		R5F102 product		R5F103 product	
		20, 24 pin product	30 pin product	20, 24 pin product	30 pin product
Serial interface	UART	1 channel	3 channels	1 channel	
	CSI	2 channels	3 channels	1 channel	
	Simplified I^2C	2 channels	3 channels	None	
DMA function		2 channels		None	
Safety function	CRC operation	Yes		None	
	RAM guard	Yes		None	
	SFR guard	Yes		None	

1.6.3 30-pin products



(2/2)

Item		20-pin		24-pin		30-pin	
		R5F1026x	R5F1036x	R5F1027x	R5F1037x	R5F102Ax	R5F103Ax
Clock output/buzzer output		1				2	
		2.44 kHz to 10 MHz: (Peripheral hardware clock: f_{MAIN} = 20 MHz operation)					
8/10-bit resolution A/D converter		11 channels				8 channels	
Serial interface		[R5F1026x (20-pin), R5F1027x (24-pin)] ・ CSI: 2 channels/Simplified I^2C: 2 channels/UART: 1 channel [R5F102Ax (30-pin)] ・ CSI: 1 channel/Simplified I^2C: 1 channel/UART: 1 channel ・ CSI: 1 channel/Simplified I^2C: 1 channel/UART: 1 channel ・ CSI: 1 channel/Simplified I^2C: 1 channel/UART: 1 channel [R5F1036x (20-pin), R5F1037x (24-pin)] ・ CSI: 1 channel/Simplified I^2C: 0 channel/UART: 1 channel [R5F103Ax (30-pin)] ・ CSI: 1 channel/Simplified I^2C: 0 channel/UART: 1 channel					
	I^2C bus	1 channel					
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (unsigned or signed) • 32 bits × 32 bits = 32 bits (unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (unsigned or signed)					
DMA controller		2 channels	—	2 channels	—	2 channels	—
Vectored interrupt sources	Internal	18	16	18	16	26	19
	External	5				6	
Key interrupt		6		10		—	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access					
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP) • Power-down-reset: 1.50 V (TYP)					
Voltage detector		• Rising edge : 1.88 to 4.06 V (12 stages) • Falling edge : 1.84 to 3.98 V (12 stages)					
On-chip debug function		Provided					
Power supply voltage		V_{DD} = 1.8 to 5.5 V					
Operating ambient temperature		T_A = −40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = −40 to +105°C (G: Industrial applications)					

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/4)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	20-, 24-pin products: Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42 30-pin products: Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147				−10.0 [Note 2]	mA
		20-, 24-pin products: Total of P40 to P42 30-pin products: Total of P00, P01, P40, P120 (When duty ≤ 70% [Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			−30.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−6.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			−4.5	mA
		20-, 24-pin products: Total of P00 to P03[Note 4], P10 to P14 30-pin products: Total of P10 to P17, P30, P31, P50, P51, P147 (When duty ≤ 70% [Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			−80.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−18.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			−10.0	mA
		Total of all pins (When duty ≤ 70% [Note 3])				−100	mA
	I_{OH2}	Per pin for P20 to P23				−0.1	mA
		Total of all pins				−0.4	mA

Notes 1. value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. The output current value under conditions where the duty factor ≤ 70%.
If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = −10.0 mA

Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ −8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. 24-pin products only.

Caution P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(1) 20-, 24-pin products

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS(High-speed main) mode[Note 4]	f_{IH} = 24 MHz[Note 3]	Basic operation	V_{DD} = 5.0 V		1.5		mA
						V_{DD} = 3.0 V		1.5		
					Normal operation	V_{DD} = 5.0 V		3.3	5.0	mA
						V_{DD} = 3.0 V		3.3	5.0	
				f_{IH} = 16 MHz[Note 3]		V_{DD} = 5.0 V		2.5	3.7	mA
						V_{DD} = 3.0 V		2.5	3.7	
			LS(Low-speed main) mode[Note 4]	f_{IH} = 8 MHz[Note 3]		V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	
			HS(High-speed main) mode[Note4]	f_{MX} = 20 MHz[Note 2], V_{DD} = 5.0 V		Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	
				f_{MX} = 20 MHz[Note 2], V_{DD} = 3.0 V		Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 5.0 V		Square wave input		1.8	2.6	mA
						Resonator connection		1.8	2.6	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 3.0 V		Square wave input		1.8	2.6	mA
						Resonator connection		1.8	2.6	
			LS(Low-speed main) mode[Note 4]	f_{MX} = 8 MHz[Note 2], V_{DD} = 3.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f_{MX} = 8 MHz[Note 2], V_{DD} = 2.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.

3. When high-speed system clock is stopped

4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS(Low speed main) mode: V_{DD} = 1.8 V to 5.5 V @1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C.

(2) 30-pin products

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (High-speed main) mode Note 6	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		440	1280	μA
					V_{DD} = 3.0 V		440	1280	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		400	1000	μA
					V_{DD} = 3.0 V		400	1000	
			LS (Low-speed main) mode Note 6	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		260	530	μA
					V_{DD} = 2.0 V		260	530	
			HS (High-speed main) mode Note 6	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		280	1000	μA
					Resonator connection		450	1170	
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		280	1000	μA
					Resonator connection		450	1170	
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		190	600	μA
					Resonator connection		260	670	
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		190	600	μA
					Resonator connection		260	670	
			LS (Low-speed main) mode Note 6	f_{MX} = 8 MHz Note 3, V_{DD} = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
				f_{MX} = 8 MHz Note 3 V_{DD} = 2.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
	I_{DD3} Note 5	STOP mode	T_A = −40°C				0.18	0.50	μA
			T_A = +25°C				0.23	0.50	
			T_A = +50°C				0.30	1.10	
			T_A = +70°C				0.46	1.90	
			T_A = +85°C				0.75	3.30	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator clock is stopped.

4. When high-speed system clock is stopped.

5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS (Low speed main) mode: V_{DD} = 1.8 V to 5.5 V @1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Except STOP mode, temperature condition of the TYP. value is T_A = 25°C.

(3) Peripheral functions (Common to all products)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed onchip oscillator operating current	I_{FIL} Note 1				0.20		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 2, 3				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 4	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 5	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.30	1.70	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.50	0.70	mA
A/D converter reference voltage operating current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVD} Notes 1, 6				0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 8				2.00	12.20	mA
BGO operating current	I_{BGO} Notes 1, 7				2.00	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 9		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to the V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{FIL} and I_{TMKA} when the 12-bit interval timer operates.

4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

6. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.

7. Current flowing only during data flash rewrite.

8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. Temperature condition of the TYP. value is T_A = 25°C

3.2 Oscillator Characteristics

3.2.1 1 oscillator characteristics

□ □ □–40 to 105 °□2.4 V ≤ V_{DD} ≤ 5.5 V□V □ □0 V□

Parameter	Resonator	Conditions	MIN.	TP.	MA.	Unit
1 clock oscillation frequency (f)ote	Ceramic resonator / crystal oscillator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} 2.7 V	1.0		8.0	

ote **Indicates only permissible oscillator frequency ranges. Refer AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.**

tion **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the 1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remr□ **When using the 1 oscillator, refer to 5.4 tem loc□illtor.**

3.2.2 On-chip oscillator characteristics

□ □ □–40 to 105 °□2.4 V ≤ V_{DD} ≤ 5.5 V□V □ □0 V□

Oscillators	Parameters	Conditions		MIN.	TP.	MA.	Unit
High-speed on-chip oscillator clock frequencyote1 2	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		R5F102 products	T_A = −20 to +85°C	-1.0		+1.0	
			T_A = −40 to −20°C	-1.5		+1.5	
			T_A = +85 to +105°C	-2.0		+2.0	
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	

ote□1. **High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.**

2. **This only indicates the oscillator characteristics. Refer AC Characteristics for instruction execution time.**

(1) 20-, 24-pin products

(T_A = □40 to +105□C, 2.4 V □□V_{DD} □5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (High-speed main) mode Note 6	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		440	2230	□A
					V_{DD} = 3.0 V		440	2230	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		400	1650	□A
					V_{DD} = 3.0 V		400	1650	
				f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		280	1900	□A
					Resonator connection		450	2000	
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		280	1900	□A
					Resonator connection		450	2000	
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		190	1010	□A
					Resonator connection		260	1090	
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		190	1010	□A
					Resonator connection		260	1090	
	I_{DD3} Note 5	STOP mode	T_A = □□40□C				0.19	0.50	□A
			T_A = +25□C				0.24	0.50	
			T_A = +50□C				0.32	0.80	
			T_A = +70□C				0.48	1.20	
			T_A = +85□C				0.74	2.20	
			T_A = +105□C				1.50	10.20	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.
3. When high-speed on-chip oscillator clock is stopped.
4. When high-speed system clock is stopped.
5. Not including the current flowing into the 12-bit interval timer and watchdog timer.
6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

   HS (High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
   V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency
3. Except temperature condition of the TYP. value is T_A = 25□□C, other than STOP mode

□

(2) 30-pin products

(T_A = □40 to +105□C, 2.4 V □□V_{DD} □5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (High-speed main) mode Note 6	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		440	2300	□A
					V_{DD} = 3.0 V		440	2300	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		400	1700	□A
					V_{DD} = 3.0 V		400	1700	
				f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		280	1900	□A
					Resonator connection		450	2000	
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		280	1900	□A
					Resonator connection		450	2000	
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		190	1020	□A
					Resonator connection		260	1100	
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		190	1020	□A
					Resonator connection		260	1100	
	I_{DD3} Note 5	STOP mode	T_A = □□40□C				0.18	0.50	□A
			T_A = +25□C				0.23	0.50	
			T_A = +50□C				0.30	1.10	
			T_A = +70□C				0.46	1.90	
			T_A = +85□C				0.75	3.30	
			T_A = +105□C				2.94	15.30	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.
3. When high-speed on-chip oscillator clock is stopped.
4. When high-speed system clock is stopped.
5. Not including the current flowing into the 12-bit interval timer and watchdog timer.
6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

   HS (High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
   V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency
3. Except STOP mode, temperature condition of the TYP. value is T_A = 25□□C.

□

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

(T_A = □40 to +105□□C, 2.4 V □□V_{DD} □□5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp□□) Note	t_{SIK1}	4.0 V □□ V_b □□ 5.5 V, 2.7 V □□ V_b □□ 4.0 V, C_b = 30 pF, R_b = 1.4 k□□	88		ns
		2.7 V □□ V_b < 4.0 V, 2.3 V □□ V_b □□ 2.7 V, C_b = 30 pF, R_b = 2.7 k□□	88		ns
		2.4 V □□ V_b < 3.3 V, 1.6 V □□ V_b □□ 2.0 V, C_b = 30 pF, R_b = 5.5 k□□	220		ns
SIp hold time (from SCKp□□) Note	t_{KSI1}	4.0 V □□ V_b □□ 5.5 V, 2.7 V □□ V_b □□ 4.0 V, C_b = 30 pF, R_b = 1.4 k□□	38		ns
		2.7 V □□ V_b < 4.0 V, 2.3 V □□ V_b □□ 2.7 V, C_b = 30 pF, R_b = 2.7 k□□	38		ns
		2.4 V □□ V_b < 3.3 V, 1.6 V □□ V_b □□ 2.0 V, C_b = 30 pF, R_b = 5.5 k□□	38		ns
Delay time from SCKp□□ to SOp output Note	t_{KSO1}	4.0 V □□ V_b □□ 5.5 V, 2.7 V □□ V_b □□ 4.0 V, C_b = 30 pF, R_b = 1.4 k□□		50	ns
		2.7 V □□ V_b < 4.0 V, 2.3 V □□ V_b □□ 2.7 V, C_b = 30 pF, R_b = 2.7 k□□		50	ns
		2.4 V □□ V_b < 3.3 V, 1.6 V □□ V_b □□ 2.0 V, C_b = 30 pF, R_b = 5.5 k□□		50	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

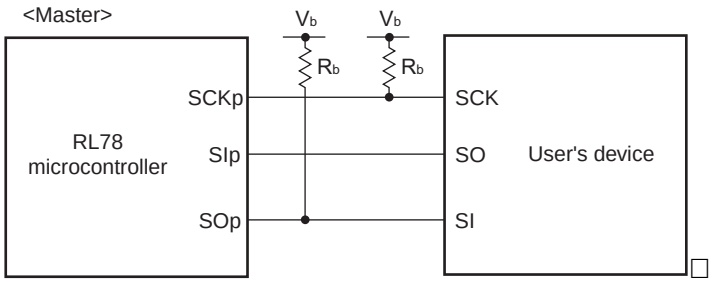
2. CSI01 and CSI11 cannot communicate at different potential.

Remarks 1. R_b [□]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

CSI mode connection diagram (during communication at different potential)

□



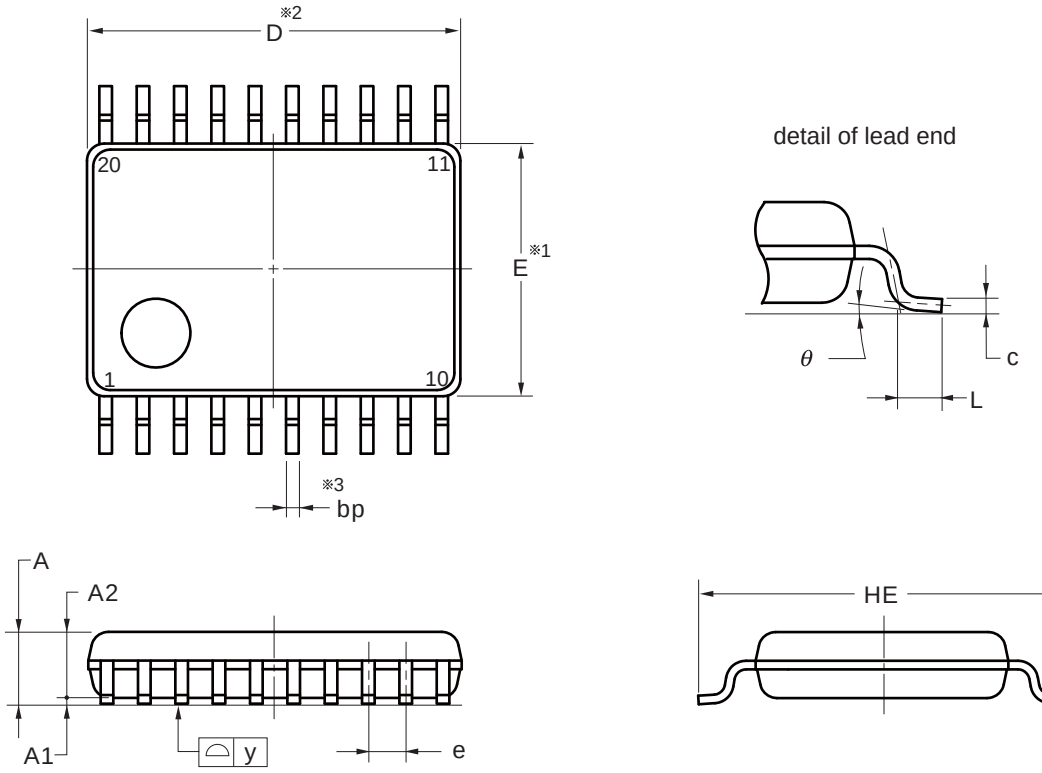
□

4. PACKAGE DRAWINGS

4.1 20-pin products

R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP
R5F1036AASP, R5F10369ASP, R5F10368ASP, R5F10367ASP, R5F10366ASP
R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP
R5F1036ADSP, R5F10369DSP, R5F10368DSP, R5F10367DSP, R5F10366DSP
<R> R5F1026AGSP, R5F10269GSP, R5F10268GSP, R5F10267GSP, R5F10266GSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1



(UNIT:mm)

ITEM	DIMENSIONS
D	6.50±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.45 MAX.
A1	0.10±0.10
A2	1.15
e	0.65±0.12
bp	$0.22^{+0.10}_{-0.05}$
c	$0.15^{+0.05}_{-0.02}$
L	0.50±0.20
y	0.10
θ	0° to 10°

NOTE

1.Dimensions ※1 and ※2 do not include mold flash.

2.Dimension ※3 does not include trim offset.

Rev.	Date	Description	
		Page	Summary
1.00	Dec 10, 2012	-	First Edition issued
2.00	Sep 06, 2013	1	Modification of 1.1 Features
		3	Modification of 1.2 List of Part Numbers
		4	Modification of Table 1-1. List of Ordering Part Numbers, Note, and Caution
		7 to 9	Modification of package name in 1.4.1 to 1.4.3
		14	Modification of tables in 1.7 Outline of Functions
		17	Modification of description of table in 2.1 Absolute Maximum Ratings (T_A = 25°C)
		18	Modification of table, Note, and Caution in 2.2.1 X1 oscillator characteristics
		18	Modification of table in 2.2.2 On-chip oscillator characteristics
		19	Modification of Note 3 in 2.3.1 Pin characteristics (1/4)
		20	Modification of Note 3 in 2.3.1 Pin characteristics (2/4)
		23	Modification of Notes 1 and 2 in (1) 20-, 24-pin products (1/2)
		24	Modification of Notes 1 and 3 in (1) 20-, 24-pin products (2/2)
		25	Modification of Notes 1 and 2 in (2) 30-pin products (1/2)
		26	Modification of Notes 1 and 3 in (2) 30-pin products (2/2)
		27	Modification of (3) Peripheral functions (Common to all products)
		28	Modification of table in 2.4 AC Characteristics
		29	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		30	Modification of figures of AC Timing Test Point and External Main System Clock Timing
		31	Modification of figure of AC Timing Test Point
		31	Modification of description and Note 2 in (1) During communication at same potential (UART mode)
		32	Modification of description in (2) During communication at same potential (CSI mode)
		33	Modification of description in (3) During communication at same potential (CSI mode)
		34	Modification of description in (4) During communication at same potential (CSI mode)
		36	Modification of table and Note 2 in (5) During communication at same potential (simplified I^2C mode)
		38, 39	Modification of table and Notes 1 to 9 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)
		40	Modification of Remarks 1 to 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)
		41	Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode)
		42	Modification of Caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode)
		43	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		44	Modification of table and Notes 1 and 2 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		45	Modification of table, Note 1, and Caution 1 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		47	Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode)
		50	Modification of table, Note 1, and Caution 1 in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode)
		52	Modification of Remark in 2.5.2 Serial interface IICA
		53	Addition of table to 2.6.1 A/D converter characteristics
		53	Modification of description in 2.6.1 (1)
		54	Modification of Notes 3 to 5 in 2.6.1 (1)
		54	Modification of description and Notes 2 to 4 in 2.6.1 (2)

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.