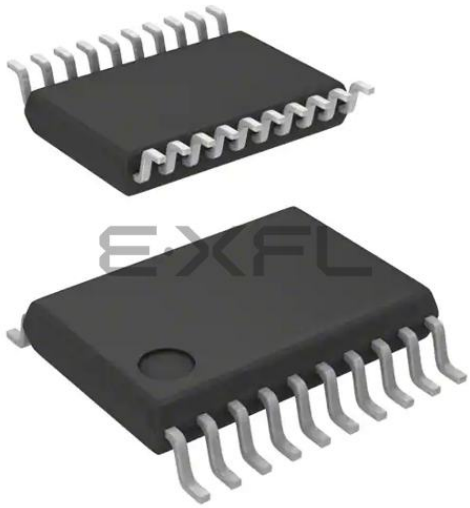

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

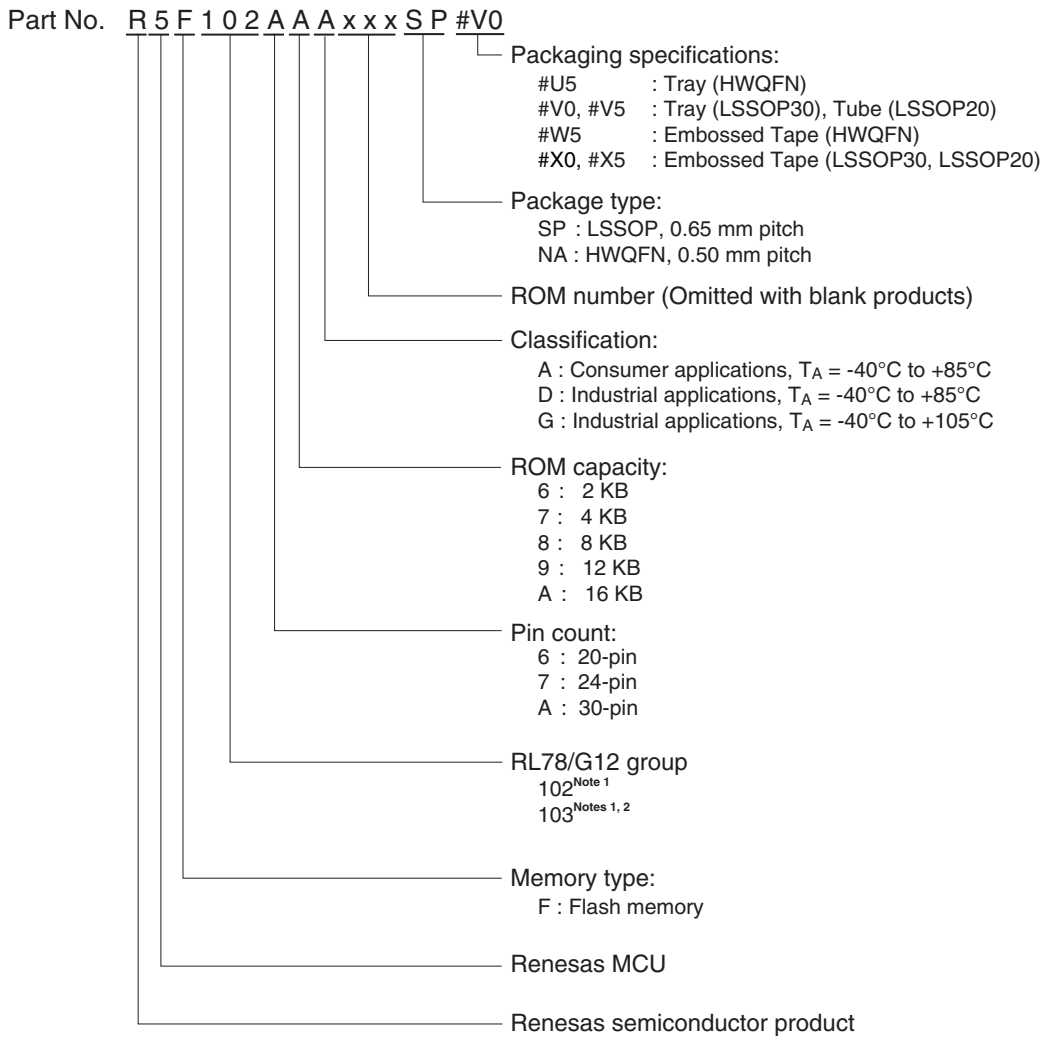
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CSI, I²C, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 14 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 1.5K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 11x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-LSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1026agsp-v5 |

## 1.2 List of Part Numbers

**Figure 1-1. Part Number, Memory Size, and Package of RL78/G12**

<R>




**Notes 1.** For details about the differences between the R5F102 products and the R5F103 products of RL78/G12, see **1.1 Differences between the R5F102 Products and the R5F103 Products**.

**2.** Products only for "A: Consumer applications ($T_A$ = -40 to +85°C)" and "D: Industrial applications ($T_A$ = -40 to +85°C)"

## 1.3 Differences between the R5F102 Products and the R5F103 Products

The following are differences between the R5F102 products and the R5F103 products.

- Whether the data flash memory is mounted or not
- High-speed on-chip oscillator oscillation frequency accuracy
- Number of channels in serial interface
- Whether the DMA function is mounted or not
- Whether a part of the safety functions are mounted or not

### 1.3.1 Data Flash

The data flash memory of 2 KB is mounted on the R5F102 products, but not on the R5F103 products.

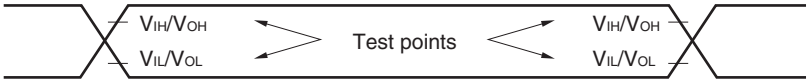
| Product | Data Flash |
|---|---|
| **R5F102 products**<br>R5F1026A, R5F1027A, R5F102AA,<br>R5F10269, R5F10279, R5F102A9,<br>R5F10268, R5F10278, R5F102A8,<br>R5F10267, R5F10277, R5F102A7,<br>R5F10266 Note | 2KB |
| **R5F103 products**<br>R5F1036A, R5F1037A, R5F103AA,<br>R5F10369, R5F10379, R5F103A9,<br>R5F10368, R5F10378 R5F103A8,<br>R5F10367, R5F10377, R5F103A7,<br>R5F10366 | Not mounted |

**Note** The RAM in the R5F10266 has capacity as small as 256 bytes. Depending on the customer's program specification, the stack area to execute the data flash library may not be kept and data may not be written to or erased from the data flash memory.

**Caution** When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

## 2.5 Peripheral Functions Characteristics

**AC Timing Test Point**




### 2.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

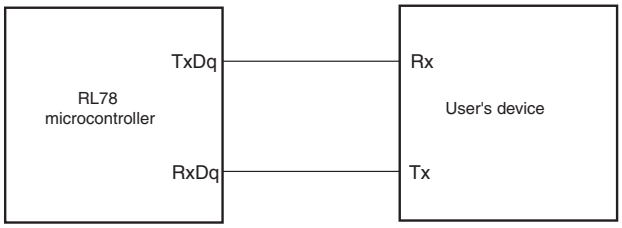
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 1 | | | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{CLK} = f_{MCK}$ Note2 | | 4.0 | | 1.3 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

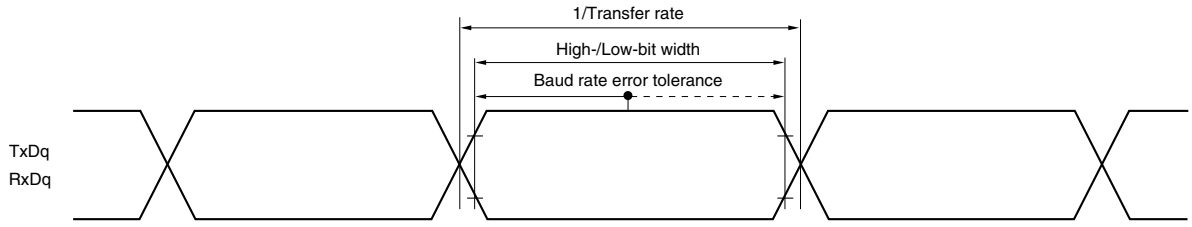
**2.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**UART mode connection diagram (during communication at same potential)**



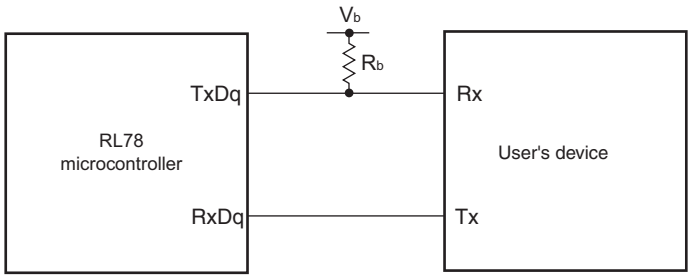

**UART mode bit width (during communication at same potential) (reference)**



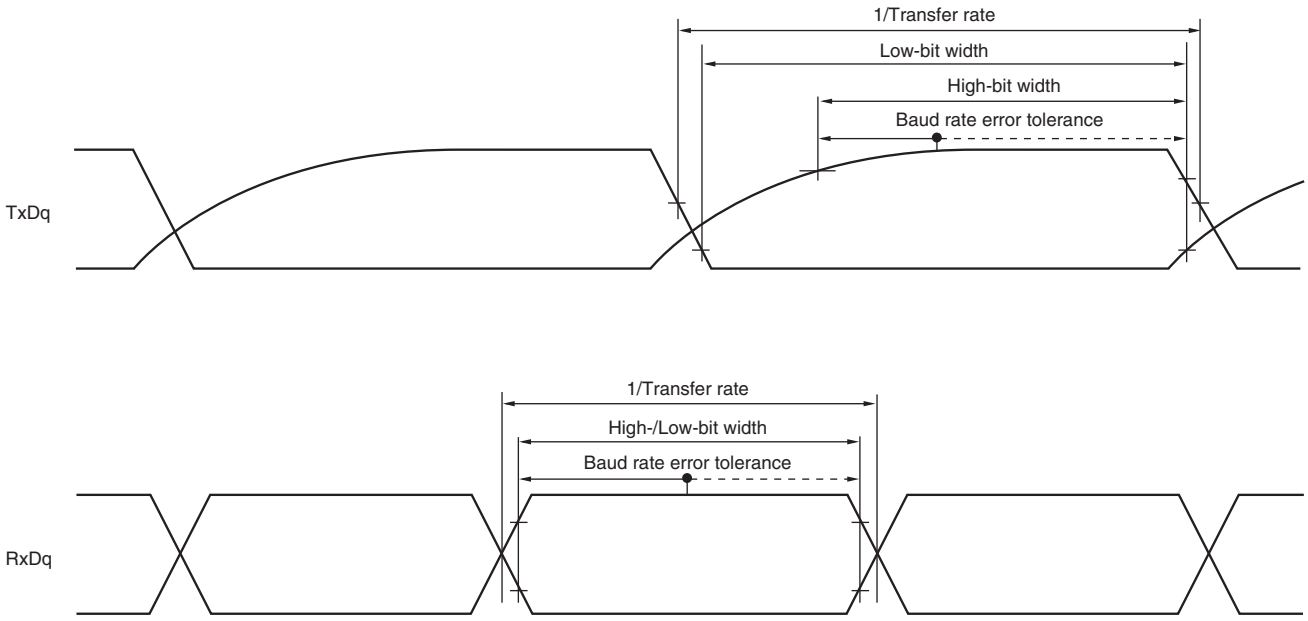

**Remarks 1.** q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**UART mode connection diagram (during communication at different potential)**




**UART mode bit width (during communication at different potential) (reference)**




**Remarks 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance, $C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**4.** UART0 of the 20- and 24-pin products supports communication at different potential only when the peripheral I/O redirection function is not used.

**Notes 1.** When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1

**2.** When DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

**Caution** Select the TTL input buffer for the SI00 pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SO00 pin and SCK00 pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $R_b$ [Ω]:Communication line (SCK00, SO00) pull-up resistance, $C_b$ [F]: Communication line (SCK00, SO00) load capacitance, $V_b$ [V]: Communication line voltage

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS00 bit of serial mode register 00 (SMR00).)

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 81 | | 479 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 177 | | 479 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 100 | | 100 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 195 | | 195 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 483 | | 483 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**2.** Use it with $V_{DD} \geq V_b$.

(**Cautions** and **Remarks** are listed on the next page.)

**(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode)**

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | | 400 Note1 | | 300 Note1 | kHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 400 Note1 | | 300 Note1 | kHz |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, Note2 $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 300 Note1 | | 300 Note1 | kHz |
| Hold time when SCLr = "L" | $t_{LOW}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1150 | | 1550 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1150 | | 1550 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, Note2 $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1550 | | 1550 | | ns |
| Hold time when SCLr = "H" | $t_{HIGH}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 675 | | 610 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 600 | | 610 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, Note2 $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 610 | | 610 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1/$f_{MCK}$ + 190 Note3 | | 1/$f_{MCK}$ + 190 Note3 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 190 Note3 | | 1/$f_{MCK}$ + 190 Note3 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, Note2 $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1/$f_{MCK}$ + 190 Note3 | | 1/$f_{MCK}$ + 190 Note3 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 0 | 355 | 0 | 355 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, Note2 $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 405 | 0 | 405 | ns |

**Notes 1.** The value must also be equal to or less than $f_{MCK}$/4.

**2.** Use it with $V_{DD} \geq V_b$.

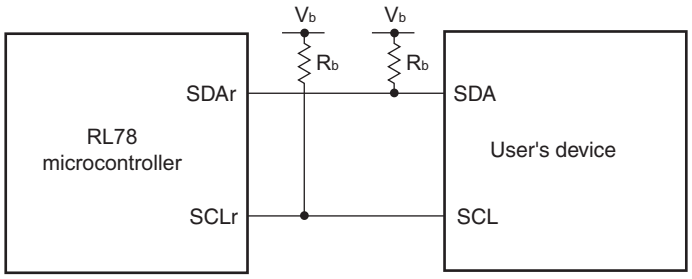
**3.** Set $t_{SU:DAT}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

**Cautions 1.** Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SCLr pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.

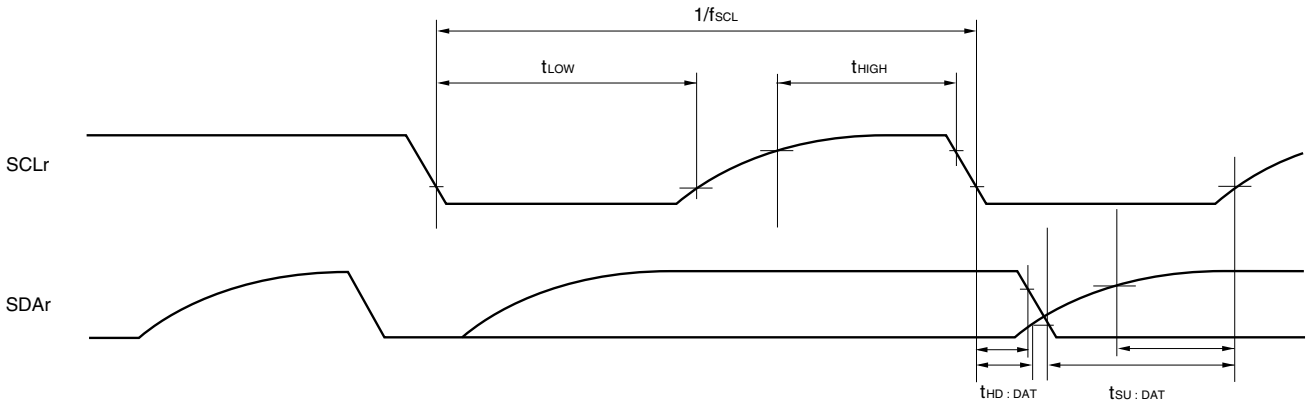
**2.** IIC01 and IIC11 cannot communicate at different potential.

(**Remarks** are listed on the next page.)

**Simplified $I^2C$ mode connection diagram (during communication at different potential)**




**Simplified $I^2C$ mode serial transfer timing (during communication at different potential)**




**Remarks 1.** $R_b$ [Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$ [F]: Communication line (SDAr, SCLr) load capacitance, $V_b$ [V]: Communication line voltage

**2.** r: IIC Number (r = 00, 20)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0,1), n: Channel number (n = 0))

**4.** Simplified $I^2C$ mode is supported only by the R5F102 products.

### 2.5.2 Serial interface IICA

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode / LS (low-speed main) mode | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Standard Mode | | Fast Mode | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | | | 0 | 400 | kHz |
| | | Normal mode: $f_{CLK}$ ≥ 1 MHz | 0 | 100 | | | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | | 4.7 | | 0.6 | | μs |
| Hold time[Note 1] | $t_{HD:STA}$ | | 4.0 | | 0.6 | | μs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | | 4.7 | | 1.3 | | μs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | | 4.0 | | 0.6 | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | | 250 | | 100 | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | | 0 | 3.45 | 0 | 0.9 | μs |
| Setup time of stop condition | $t_{SU:STO}$ | | 4.0 | | 0.6 | | μs |
| Bus-free time | $t_{BUF}$ | | 4.7 | | 1.3 | | μs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

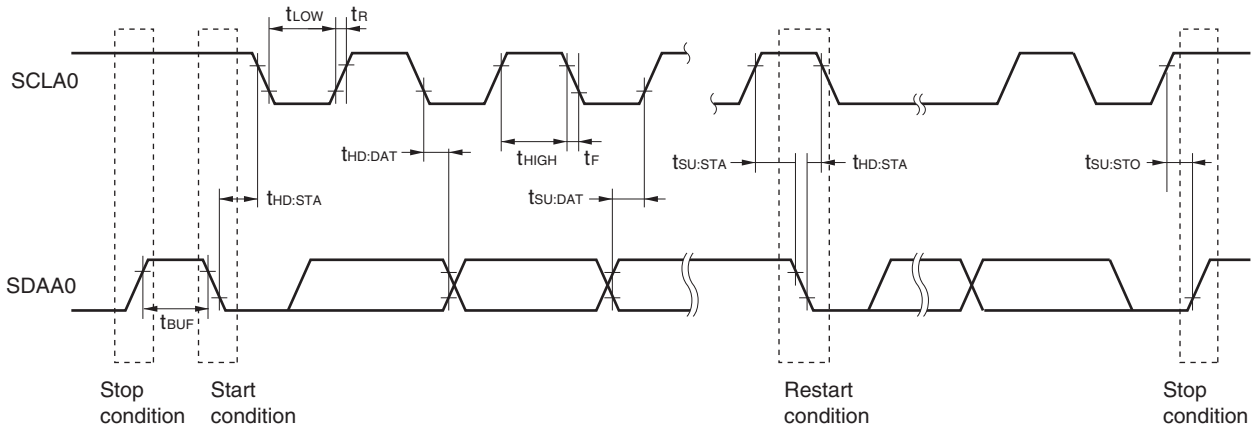
<R> **2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: $C_b$ = 400 pF, Rb = 2.7 kΩ
Fast mode: $C_b$ = 320 pF, Rb = 1.1 kΩ

IICA serial transfer timing



## 3.1 Absolute Maximum Ratings

**Absolute Maximum Ratings ($T_A$ = 25°C)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | | −0.5 to + 6.5 | V |
| REGC terminal input voltage[Note1] | $V_{IREGC}$ | REGC | | −0.3 to +2.8 and −0.3 to $V_{DD}$ + 0.3 [Note 2] | V |
| Input Voltage | $V_{I1}$ | Other than P60, P61 | | −0.3 to $V_{DD}$ + 0.3[Note 3] | V |
| | $V_{I2}$ | P60, P61 (N-ch open drain) | | −0.3 to 6.5 | V |
| Output Voltage | $V_O$ | | | −0.3 to $V_{DD}$ + 0.3[Note 3] | V |
| Analog input voltage | $V_{AI}$ | 20, 24-pin products: ANI0 to ANI3, ANI16 to ANI22<br>30-pin products: ANI0 to ANI3, ANI16 to ANI19 | | −0.3 to $V_{DD}$ + 0.3 and −0.3 to AVREF(+)+0.3 [Notes 3, 4] | V |
| Output current, high | $I_{OH1}$ | Per pin | Other than P20 to P23 | −40 | mA |
| | | Total of all pins | All the terminals other than P20 to P23 | −170 | mA |
| | | | 20-, 24-pin products: P40 to P42<br>30-pin products: P00, P01, P40, P120 | −70 | mA |
| | | | 20-, 24-pin products: P00 to P03[Note 5], P10 to P14<br>30-pin products: P10 to P17, P30, P31, P50, P51, P147 | −100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P23 | −0.5 | mA |
| | | Total of all pins | | −2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | Other than P20 to P23 | 40 | mA |
| | | Total of all pins | All the terminals other than P20 to P23 | 170 | mA |
| | | | 20-, 24-pin products: P40 to P42<br>30-pin products: P00, P01, P40, P120 | 70 | mA |
| | | | 20-, 24-pin products: P00 to P03 [Note 5], P10 to P14, P60, P61<br>30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P23 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | | | −40 to +105 | °C |
| Storage temperature | $T_{stg}$ | | | −65 to +150 | °C |

**Notes 1.** 30-pin product only.

**2.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.

**3.** Must be 6.5 V or lower.

**4.** Do not exceed $AV_{REF}(+)$ + 0.3 V in case of A/D conversion target pin.

**5.** 24-pin products only.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** $AV_{REF}(+)$ : + side reference voltage of the A/D converter.

**3.** $V_{SS}$ : Reference voltage

## 3.2 Oscillator Characteristics

### 3.2.1 X1 oscillator characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$)Note | Ceramic resonator / crystal oscillator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 8.0 | |

**Note** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

**Remark** When using the X1 oscillator, refer to **5.4 System Clock Oscillator**.

### 3.2.2 On-chip oscillator characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{IH}$ | | | 1 | | 24 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | R5F102 products | $T_A$ = –20 to +85°C | -1.0 | | +1.0 | % |
| | | | $T_A$ = –40 to –20°C | -1.5 | | +1.5 | % |
| | | | $T_A$ = +85 to +105°C | -2.0 | | +2.0 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | -15 | | +15 | % |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

**2.** This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

**(1) 20-, 24-pin products**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD2}$[Note 2] | HALT mode | HS (High-speed main) mode[Note 6] | $f_{IH}$ = 24 MHz[Note 4] | $V_{DD}$ = 5.0 V | | 440 | 2230 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 2230 | |
| | | | | $f_{IH}$ = 16 MHz[Note 4] | $V_{DD}$ = 5.0 V | | 400 | 1650 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 1650 | |
| | | | | $f_{MX}$ = 20 MHz[Note 3], $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 20 MHz[Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 10 MHz[Note 3], $V_{DD}$ = 5.0 V | Square wave input | | 190 | 1010 | μA |
| | | | | | Resonator connection | | 260 | 1090 | |
| | | | | $f_{MX}$ = 10 MHz[Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 190 | 1010 | μA |
| | | | | | Resonator connection | | 260 | 1090 | |
| | $I_{DD3}$[Note 5] | STOP mode | $T_A$ = –40°C | | | | 0.19 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.32 | 0.80 | |
| | | | $T_A$ = +70°C | | | | 0.48 | 1.20 | |
| | | | $T_A$ = +85°C | | | | 0.74 | 2.20 | |
| | | | $T_A$ = +105°C | | | | 1.50 | 10.20 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz

$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except temperature condition of the TYP. value is $T_A$ = 25°C, other than STOP mode

### (2) 30-pin products

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 6 | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 440 | 2300 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 2300 | |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 400 | 1700 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 1700 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 190 | 1020 | μA |
| | | | | | Resonator connection | | 260 | 1100 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 190 | 1020 | μA |
| | | | | | Resonator connection | | 260 | 1100 | |
| | $I_{DD3}$ Note 5 | STOP mode | $T_A$ = –40°C | | | | 0.18 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.30 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.46 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.75 | 3.30 | |
| | | | $T_A$ = +105°C | | | | 2.94 | 15.30 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C.

### (4) During communication at same potential (simplified I²C mode)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

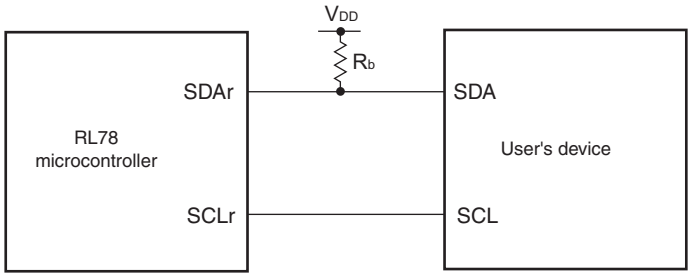
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 580 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 1420 | ns |

**Notes 1.** The value must also be equal to or less than $f_{MCK}$/4.

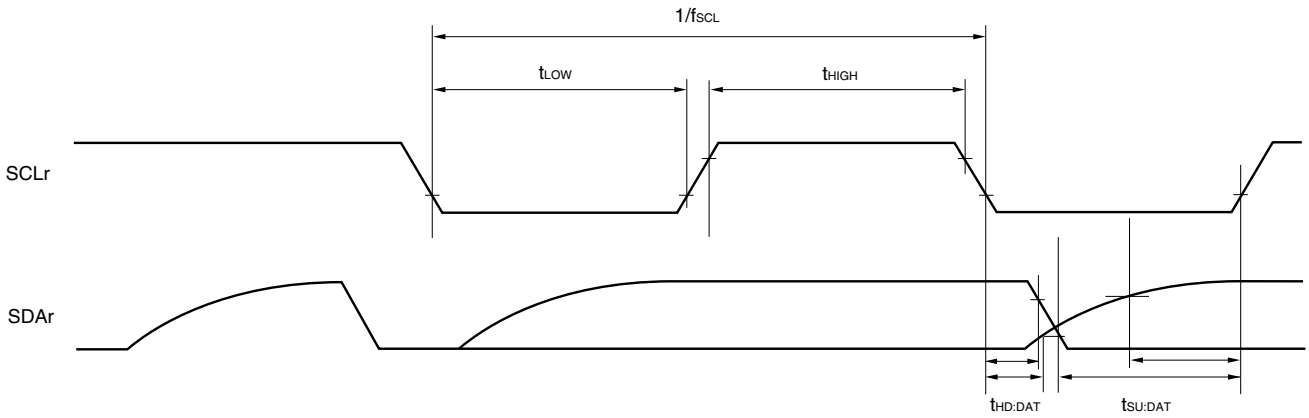
**2.** Set $t_{SU:DAT}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

**Caution** Select the N-ch open drain output ($V_{DD}$ tolerance) mode for SDAr by using port output mode register h (POMh).

**Simplified I²C mode connection diagram (during communication at same potential)**




**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remarks 1.** $R_b$ [Ω]:Communication line (SDAr) pull-up resistance

$C_b$ [F]: Communication line (SCLr, SDAr) load capacitance

**2.** r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1, 4, 5)

**3.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number (m = 0, 1), n: Channel number (0, 1, 3))

### (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| Transfer rate Note4 | | Reception | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |
| | | Transmission | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | **Note 3** | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.0 Note 4 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, | | **Note 5** | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 6 | Mbps |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | **Notes 2, 7** | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 8 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**3.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ $V_{DD}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**4.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**5.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ $V_{DD}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3}\ [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**6.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

**7.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3}\ [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**8.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 7** above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). **For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**

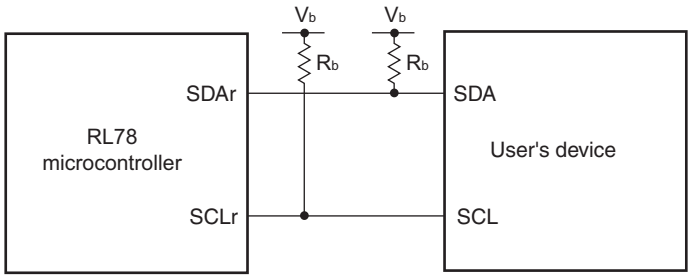
**($T_A$ = −40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 162 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 354 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 958 | | ns |
| SIp hold time (from SCKp↑) Note | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 200 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 390 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 966 | ns |

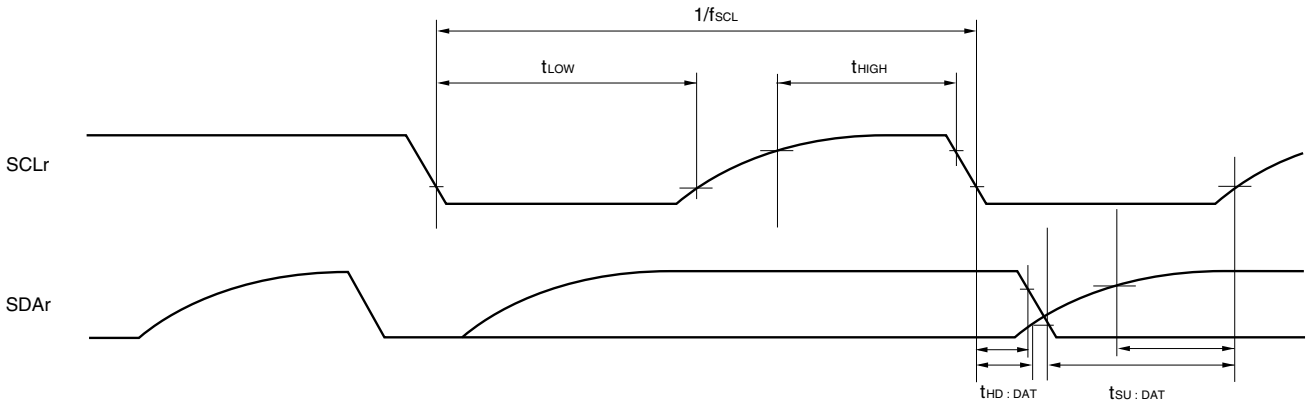
**Note** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

(**Cautions** and **Remarks** are listed on the next page.)

**Simplified $I^2C$ mode connection diagram (during communication at different potential)**




**Simplified $I^2C$ mode serial transfer timing (during communication at different potential)**




**Remarks 1.** $R_b$ [Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$ [F]: Communication line (SDAr, SCLr) load capacitance, $V_b$ [V]: Communication line voltage

**2.** r: IIC Number (r = 00, 20)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0,1), n: Channel number (n = 0))

**(3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = $V_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (–) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution | | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI3, ANI16 to ANI22 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error[Notes 1, 2] | EZS | 10-bit resolution | | | | ±0.60 | %FSR |
| Full-scale error[Notes 1, 2] | EFS | 10-bit resolution | | | | ±0.60 | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution | | | | ±4.0 | LSB |
| Differential linearity error[Note 1] | DLE | 10-bit resolution | | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI3, ANI16 to ANI22 | | 0 | | $V_{DD}$ | V |
| | | Internal reference voltage (HS (high-speed main) mode) | | $V_{BGR}$[Note 3] | | | V |
| | | Temperature sensor output voltage (HS (high-speed main) mode) | | $V_{TMPS25}$[Note 3] | | | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{REFM}$ (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (–) = $AV_{REFM}$ Note 4 = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | EZS | 8-bit resolution | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | 0 | | $V_{BGR}$ Note 3 | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

**4.** When reference voltage (–) = $V_{SS}$, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.