What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1026agsp-x0

Table 1-1. List of Ordering Part Numbers

	Pin count	Package	Data flash	Fields of Application	Part Number
\<R\>	20 pins	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)	Mounted	A	R5F1026AASP#V5, R5F10269ASP#V5, R5F10268ASP#V5, R5F10267ASP#V5, R5F10266ASP#V5 R5F1026AASP#X5, R5F10269ASP#X5, R5F10268ASP#X5, R5F10267ASP#X5, R5F10266ASP#X5
				D	R5F1026ADSP#V5, R5F10269DSP#V5, R5F10268DSP#V5, R5F10267DSP#V5, R5F10266DSP#V5 R5F1026ADSP#X5, R5F10269DSP#X5, R5F10268DSP#X5, R5F10267DSP#X5, R5F10266DSP#X5
				G	R5F1026AGSP#V5, R5F10269GSP#V5, R5F10268GSP#V5, R5F10267GSP#V5, R5F10266GSP#V5 R5F1026AGSP#X5, R5F10269GSP#X5, R5F10268GSP#X5, R5F10267GSP#X5, R5F10266GSP#X5
			Not mounted	A	R5F1036AASP#V5, R5F10369ASP#V5, R5F10368ASP#V5, R5F10367ASP#V5, R5F10366ASP#V5 R5F1036AASP#X5, R5F10369ASP#X5, R5F10368ASP#X5, R5F10367ASP#X5, R5F10366ASP#X5
				D	R5F1036ADSP#V5, R5F10369DSP#V5, R5F10368DSP#V5, R5F10367DSP#V5, R5F10366DSP#V5 R5F1036ADSP#X5, R5F10369DSP#X5, R5F10368DSP#X5, R5F10367DSP#X5, R5F10366DSP#X5
\<R\>	24 pins	24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)	Mounted	A	R5F1027AANA#U5, R5F10279ANA#U5, R5F10278ANA#U5, R5F10277ANA#U5 R5F1027AANA#W5, R5F10279ANA#W5, R5F10278ANA#W5, R5F10277ANA#W5
				D	R5F1027ADNA#U5, R5F10279DNA#U5, R5F10278DNA#U5, R5F10277DNA#U5 R5F1027ADNA#W5, R5F10279DNA#W5, R5F10278DNA#W5, R5F10277DNA#W5
				G	R5F1027AGNA#U5, R5F10279GNA#U5, R5F10278GNA#U5, R5F10277GNA#U5 R5F1027AGNA#W5, R5F10279GNA#W5, R5F10278GNA#W5, R5F10277GNA#W5
			Not mounted	A	R5F1037AANA#V5, R5F10379ANA#V5, R5F10378ANA#V5, R5F10377ANA#V5 R5F1037AANA#X5, R5F10379ANA#X5, R5F10378ANA#X5, R5F10377ANA#X5
				D	R5F1037ADNA#V5, R5F10379DNA#V5, R5F10378DNA#V5, R5F10377DNA#V5 R5F1037ADNA#X5, R5F10379DNA#X5, R5F10378DNA#X5, R5F10377DNA#X5
	30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A	R5F102AAASP#V0, R5F102A9ASP#V0, R5F102A8ASP#V0, R5F102A7ASP#V0 R5F102AAASP#X0, R5F102A9ASP#X0, R5F102A8ASP#X0, R5F102A7ASP#X0
				D	R5F102AADSP#V0, R5F102A9DSP#V0, R5F102A8DSP#V0, R5F102A7DSP#V0 R5F102AADSP#X0, R5F102A9DSP#X0, R5F102A8DSP#X0, R5F102A7DSP#X0
				G	R5F102AAGSP#V0, R5F102A9GSP#V0, R5F102A8GSP#V0, R5F102A7GSP#V0 R5F102AAGSP#X0, R5F102A9GSP#X0, R5F102A8GSP#X0, R5F102A7GSP#X0
			Not mounted	A	R5F103AAASP#V0, R5F103A9ASP#V0, R5F103A8ASP#V0, R5F103A7ASP#V0 R5F103AAASP#X0, R5F103A9ASP#X0, R5F103A8ASP#X0, R5F103A7ASP#X0
				D	R5F103AADSP#V0, R5F103A9DSP#V0, R5F103A8DSP#V0, R5F103A7DSP#V0 R5F103AADSP#X0, R5F103A9DSP#X0, R5F103A8DSP#X0, R5F103A7DSP#X0

Note For fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G12**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.2 On-chip oscillator characteristics

(1) High-speed on-chip oscillator oscillation frequency of the R5F102 products

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = -20 to +85 °C	-1.0	+1.0	%
	T_A = -40 to -20 °C	-1.5	+1.5	
	T_A = +85 to +105 °C	-2.0	+2.0	

(2) High-speed on-chip oscillator oscillation frequency of the R5F103 products

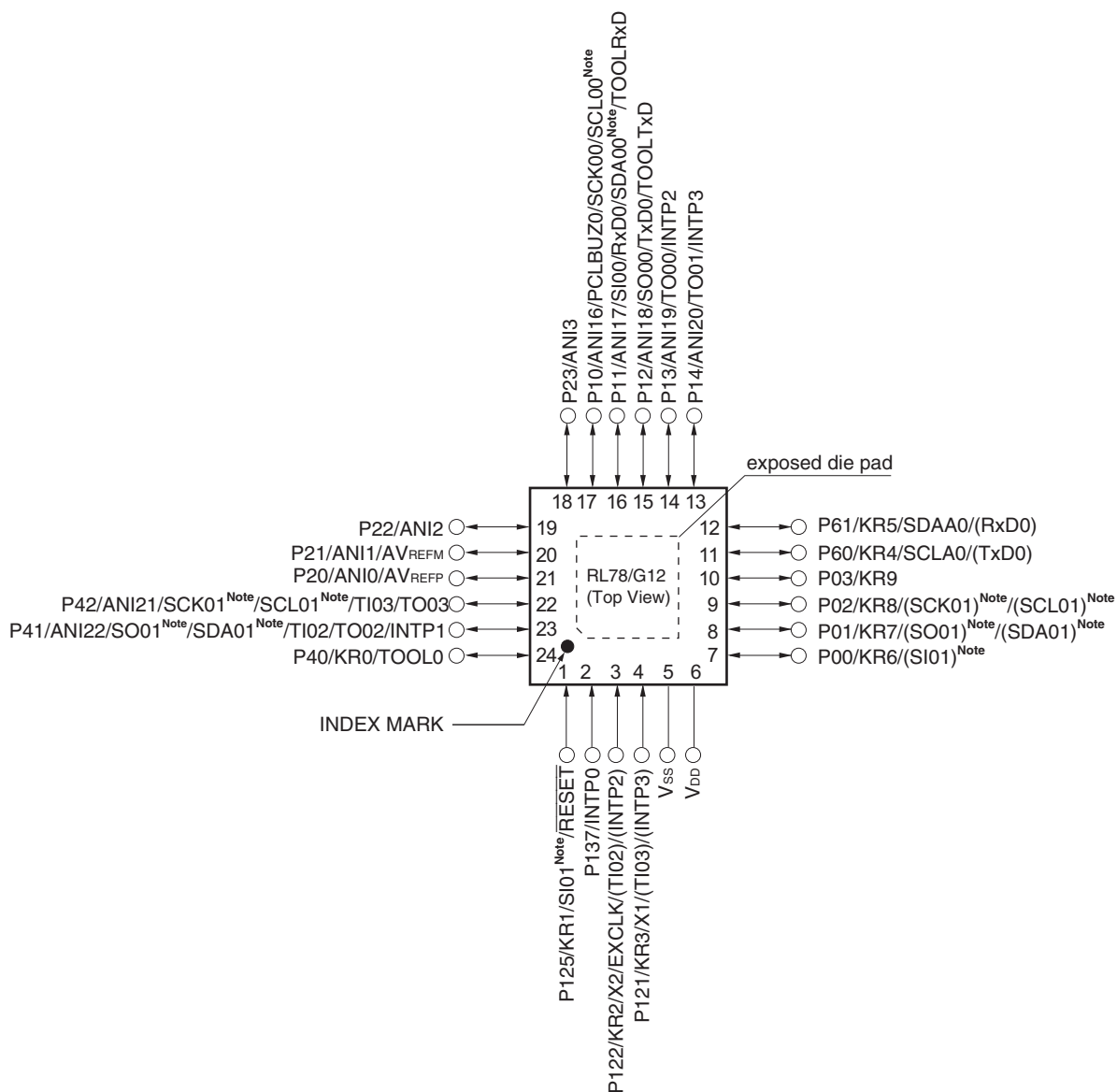| Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = -40 to + 85 °C	-5.0	+5.0	%

1.3.3 Peripheral Functions

The following are differences in peripheral functions between the R5F102 products and the R5F103 products.

RL78/G12		R5F102 product		R5F103 product	
		20, 24 pin product	30 pin product	20, 24 pin product	30 pin product
Serial interface	UART	1 channel	3 channels	1 channel	
	CSI	2 channels	3 channels	1 channel	
	Simplified I²C	2 channels	3 channels	None	
DMA function		2 channels		None	
Safety function	CRC operation	Yes		None	
	RAM guard	Yes		None	
	SFR guard	Yes		None	

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1.4.2 24-pin products

<R> • 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)

P23/ANI3
P10/ANI16/PCLBUZ0/SCK00/SCL00^Note
P11/ANI17/SI00/RxD0/SDA00^Note/TOOLRxD
P12/ANI18/SO00/TxD0/TOOLTxD
P13/ANI19/TO00/INTP2
P14/ANI20/TO01/INTP3

exposed die pad

```
                18 17  16 15 14 13
P22/ANI2    19  ┌────────────────┐ 12   P61/KR5/SDAA0/(RxD0)
P21/ANI1/AVREFM 20 │                │ 11   P60/KR4/SCLA0/(TxD0)
P20/ANI0/AVREFP 21 │   RL78/G12     │ 10   P03/KR9
P42/ANI21/SCK01^Note/SCL01^Note/TI03/TO03 22 │ (Top View) │ 9   P02/KR8/(SCK01)^Note/(SCL01)^Note
P41/ANI22/SO01^Note/SDA01^Note/TI02/TO02/INTP1 23 │          │ 8   P01/KR7/(SO01)^Note/(SDA01)^Note
P40/KR0/TOOL0 24 └────────────────┘ 7   P00/KR6/(SI01)^Note
                 1  2  3  4  5  6
```

INDEX MARK

P125/KR1/SI01^Note/RESET
P137/INTP0
P122/KR2/X2/EXCLK/(TI02)/(INTP2)
P121/KR3/X1/(TI03)/(INTP3)
V_SS
V_DD

Note Provided only in the R5F102 products.

Remarks 1. For pin identification, see **1.5 Pin Identification**.
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.
3. It is recommended to connect an exposed die pad to Vss.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T$_A$ = 25°C)

Parameter	Symbols	Conditions			Ratings	Unit
Supply Voltage	V$_{DD}$				−0.5 to + 6.5	V
REGC terminal input voltage[Note1]	V$_{IREGC}$	REGC			−0.3 to +2.8 and −0.3 to V$_{DD}$ + 0.3 [Note 2]	V
Input Voltage	V$_{I1}$	Other than P60, P61			−0.3 to V$_{DD}$ + 0.3[Note 3]	V
	V$_{I2}$	P60, P61 (N-ch open drain)			−0.3 to 6.5	V
Output Voltage	V$_O$				−0.3 to V$_{DD}$ + 0.3[Note 3]	V
Analog input voltage	V$_{AI}$	20-, 24-pin products: ANI0 to ANI3, ANI16 to ANI22 30-pin products: ANI0 to ANI3, ANI16 to ANI19			−0.3 to V$_{DD}$ + 0.3 and −0.3 to AVREF(+)+0.3[Notes 3, 4]	V
Output current, high	I$_{OH1}$	Per pin	Other than P20 to P23		−40	mA
		Total of all pins	All the terminals other than P20 to P23		−170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120		−70	mA
			20-, 24-pin products: P00 to P03[Note 5], P10 to P14 30-pin products: P10 to P17, P30, P31, P50, P51, P147		−100	mA
	I$_{OH2}$	Per pin	P20 to P23		−0.5	mA
		Total of all pins			−2	mA
Output current, low	I$_{OL1}$	Per pin	Other than P20 to P23		40	mA
		Total of all pins	All the terminals other than P20 to P23		170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120		70	mA
			20-, 24-pin products: P00 to P03[Note 5], P10 to P14, P60, P61 30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147		100	mA
	I$_{OL2}$	Per pin	P20 to P23		1	mA
		Total of all pins			5	mA
Operating ambient temperature	T$_A$				−40 to +85	°C
Storage temperature	T$_{stg}$				−65 to +150	°C

Notes 1. 30-pin product only.
     2. Connect the REGC pin to V$_{SS}$ via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.
     3. Must be 6.5 V or lower.
     4. Do not exceed AV$_{REF}$(+) + 0.3 V in case of A/D conversion target pin.
     5. 24-pin products only.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
     2. AV$_{REF}$(+) : + side reference voltage of the A/D converter.
     3. V$_{SS}$: Reference voltage

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)   **(2/4)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I$_{OL1}$	20-, 24-pin products: Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42 30-pin products: Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147				20.0 Note 2	mA
		Per pin for P60, P61				15.0 Note 2	mA
		20-, 24-pin products: Total of P40 to P42 30-pin products: Total of P00, P01, P40, P120 (When duty ≤ 70%[Note 3])	4.0 V ≤ V$_{DD}$ ≤ 5.5 V			60.0	mA
			2.7 V ≤ V$_{DD}$ < 4.0 V			9.0	mA
			1.8 V ≤ V$_{DD}$ < 2.7 V			1.8	mA
		20-, 24-pin products: Total of P00 to P03[Note 4], P10 to P14, P60, P61 30-pin products: Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147 (When duty ≤ 70%[Note 3])	4.0 V ≤ V$_{DD}$ ≤ 5.5 V			80.0	mA
			2.7 V ≤ V$_{DD}$ < 4.0 V			27.0	mA
			1.8 V ≤ V$_{DD}$ < 2.7 V			5.4	mA
		Total of all pins (When duty ≤ 70%[Note 3])				140	mA
	I$_{OL2}$	Per pin for P20 to P23				0.4	mA
		Total of all pins				1.6	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V$_{SS}$ pin.

2. However, do not exceed the total current value.

3. The output current value under conditions where the duty factor ≤ 70%.

If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = (I$_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and I$_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. 24-pin products only.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V) **(4/4)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V$_{OL1}$	20-, 24-pin products: P00 to P03^{Note}, P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 20.0 mA			1.3	V
			4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 8.5 mA			0.7	V
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 3.0 mA			0.6	V
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 1.5 mA			0.4	V
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 0.6 mA			0.4	V
	V$_{OL2}$	P20 to P23	I$_{OL2}$ = 400 μA			0.4	V
	V$_{OL3}$	P60, P61	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 15.0 mA			2.0	V
			4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 5.0 mA			0.4	V
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 3.0 mA			0.4	V
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 2.0 mA			0.4	V
Input leakage current, high	I$_{LIH1}$	Other than P121, P122	V$_I$ = V$_{DD}$			1	μA
	I$_{LIH2}$	P121, P122 (X1, X2/EXCLK)	V$_I$ = V$_{DD}$ — Input port or external clock input			1	μA
			When resonator connected			10	μA
Input leakage current, low	I$_{LIL1}$	Other than P121, P122	V$_I$ = V$_{SS}$			−1	μA
	I$_{LIL2}$	P121, P122 (X1, X2/EXCLK)	V$_I$ = V$_{SS}$ — Input port or external clock input			−1	μA
			When resonator connected			−10	μA
On-chip pull-up resistance	R$_U$	20-, 24-pin products: P00 to P03^{Note}, P10 to P14, P40 to P42, P125, $\overline{RESET}$ 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	V$_I$ = V$_{SS}$, input port	10	20	100	kΩ

Note 24-pin products only.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
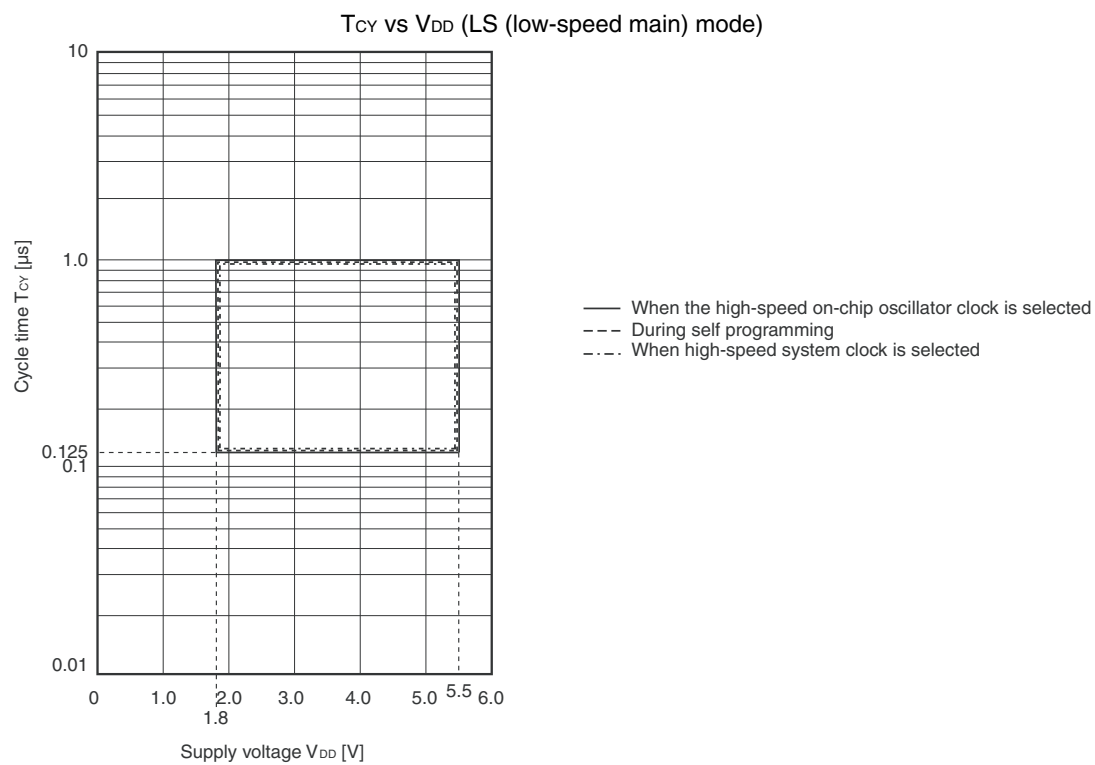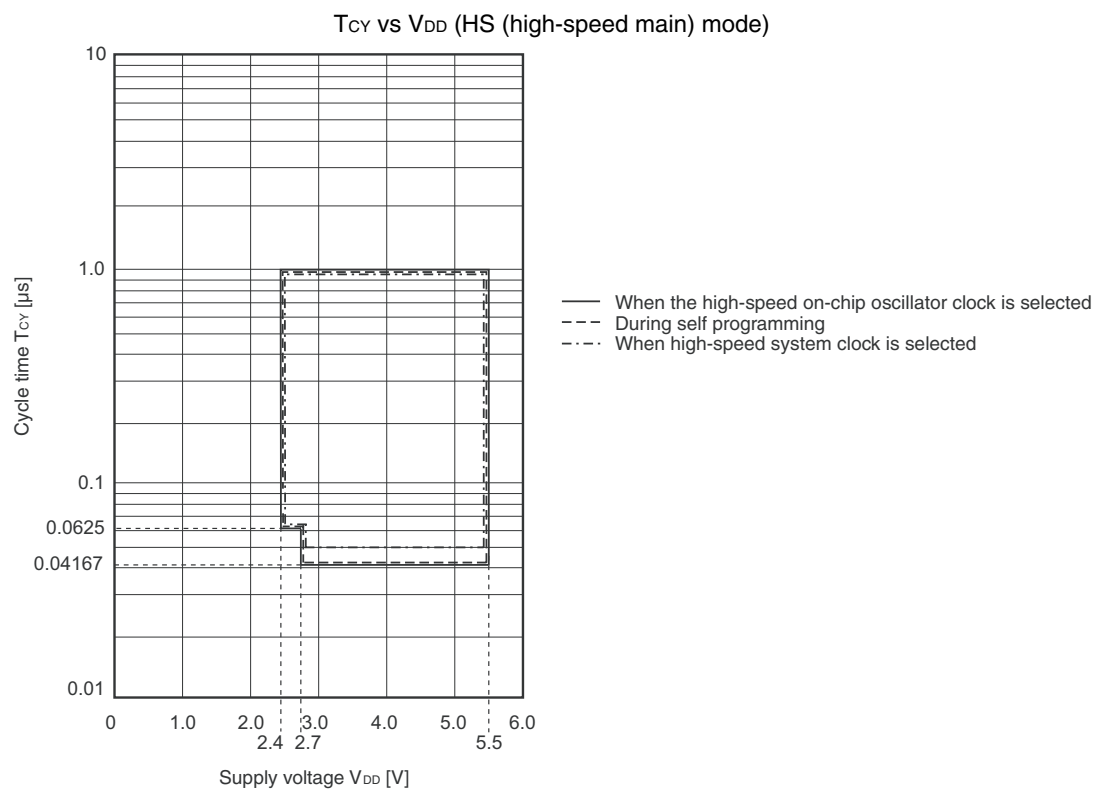
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(1) 20-, 24-pin products

(TA = −40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)   **(2/2)**

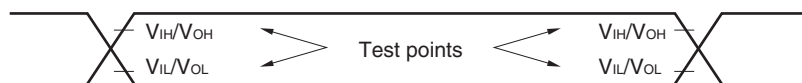| Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I_{DD2} [Note 2]	HALT mode	HS (High-speed main) mode [Note 6]	f_{IH} = 24 MHz [Note 4]	V_{DD} = 5.0 V		440	1210	μA
					V_{DD} = 3.0 V		440	1210	
				f_{IH} = 16 MHz [Note 4]	V_{DD} = 5.0 V		400	950	μA
					V_{DD} = 3.0 V		400	950	
			LS (Low-speed main) mode [Note 6]	f_{IH} = 8 MHz [Note 4]	V_{DD} = 3.0 V		270	542	μA
					V_{DD} = 2.0 V		270	542	
			HS (High-speed main) mode [Note 6]	f_{MX} = 20 MHz [Note 3], V_{DD} = 5.0 V	Square wave input		280	1000	μA
					Resonator connection		450	1170	
				f_{MX} = 20 MHz [Note 3], V_{DD} = 3.0 V	Square wave input		280	1000	μA
					Resonator connection		450	1170	
				f_{MX} = 10 MHz [Note 3], V_{DD} = 5.0 V	Square wave input		190	590	μA
					Resonator connection		260	660	
				f_{MX} = 10 MHz [Note 3], V_{DD} = 3.0 V	Square wave input		190	590	μA
					Resonator connection		260	660	
			LS (Low-speed main) mode [Note 6]	f_{MX} = 8 MHz [Note 3], V_{DD} = 3.0 V	Square wave input		110	360	μA
					Resonator connection		150	416	
				f_{MX} = 8 MHz [Note 3], V_{DD} = 2.0 V	Square wave input		110	360	μA
					Resonator connection		150	416	
	I_{DD3} [Note 5]	STOP mode	T_A = −40°C				0.19	0.50	μA
			T_A = +25°C				0.24	0.50	
			T_A = +50°C				0.32	0.80	
			T_A = +70°C				0.48	1.20	
			T_A = +85°C				0.74	2.20	

Notes **1.** Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

    2. During HALT instruction execution by flash memory.

    3. When high-speed on-chip oscillator clock is stopped.

    4. When high-speed system clock is stopped.

    5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

    6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

        HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz

                                       V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

        LS(Low speed main) mode: V_{DD} = 1.8 V to 5.5 V @1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

    2. f_{IH}: high-speed on-chip oscillator clock frequency

    3. Except temperature condition of the TYP. value is T_A = 25°C, other than STOP mode

Minimum Instruction Execution Time during Main System Clock Operation

T$_{CY}$ vs V$_{DD}$ (HS (high-speed main) mode)

- —— When the high-speed on-chip oscillator clock is selected
- − − − During self programming
- −·−· When high-speed system clock is selected

T$_{CY}$ vs V$_{DD}$ (LS (low-speed main) mode)

- —— When the high-speed on-chip oscillator clock is selected
- − − − During self programming
- −·−· When high-speed system clock is selected

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2.5 Peripheral Functions Characteristics

AC Timing Test Point

2.5.1 Serial array unit

(1) During communication at same potential (UART mode)
(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1				f$_{MCK}$/6		f$_{MCK}$/6	bps
		Theoretical value of the maximum transfer rate f$_{CLK}$ = f$_{MCK}$Note2		4.0		1.3	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

   2. The maximum operating frequencies of the CPU/peripheral hardware clock (f$_{CLK}$) are:

    HS (high-speed main) mode: 24 MHz (2.7 V ≤ V$_{DD}$ ≤ 5.5 V)

               16 MHz (2.4 V ≤ V$_{DD}$ ≤ 5.5 V)

    LS (low-speed main) mode: 8 MHz (1.8 V ≤ V$_{DD}$ ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)
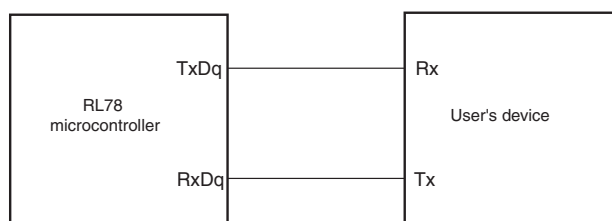
UART mode bit width (during communication at same potential) (reference)
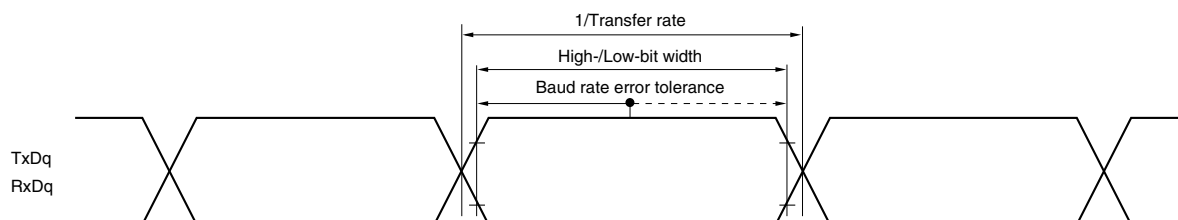
Remarks 1. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

    2. f$_{MCK}$: Serial array unit operation clock frequency

    (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

    m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

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(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	81		479		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	177		479		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	479		479		ns
SIp hold time (from SCKp↑) [Note 1]	t$_{KSI1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	19		19		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	19		19		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	19		19		ns
Delay time from SCKp↓ to SOp output [Note 1]	t$_{KSO1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		100		100	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		195		195	ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		483		483	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. Use it with V$_{DD}$ ≥ V$_b$.

(**Cautions** and **Remarks** are listed on the next page.)

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(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 1	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	44		110		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	44		110		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	110		110		ns
SIp hold time (from SCKp↓) Note 1	t$_{KSI1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	19		19		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	19		19		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	19		19		ns
Delay time from SCKp↑ to SOp output Note 1	t$_{KSO1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		25		25	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		25		25	ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V Note 2, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
   2. Use it with V$_{DD}$ ≥ V$_b$.

Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.
   **2.** CSI01 and CSI11 cannot communicate at different potential.

Remarks 1. R$_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, C$_b$ [F]: Communication line (SCKp, SOp) load capacitance, V$_b$ [V]: Communication line voltage
   2. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

CSI mode connection diagram (during communication at different potential)
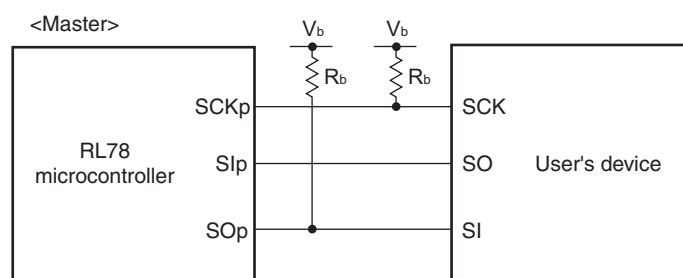
CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
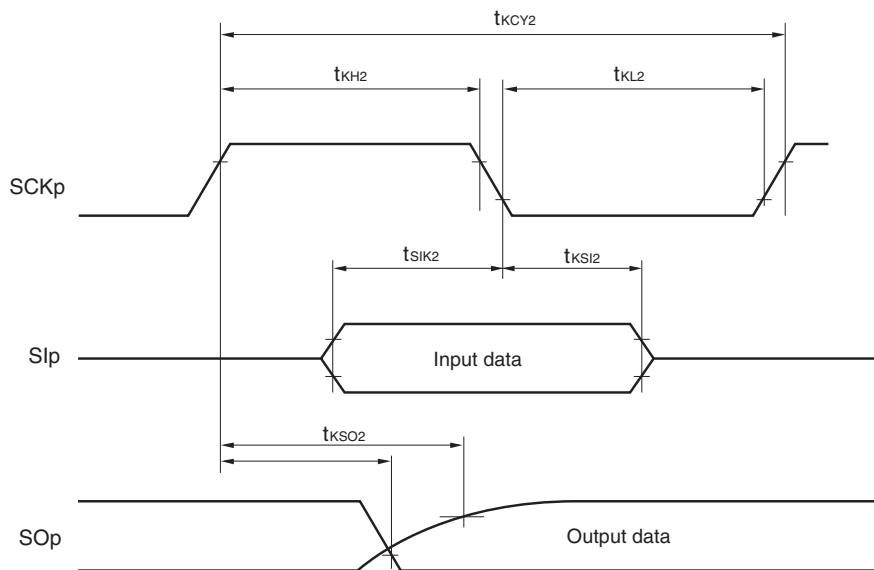
Remark   p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

2.5.2 Serial interface IICA

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode LS (low-speed main) mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode: f$_{CLK}$ ≥ 3.5 MHz			0	400	kHz
		Normal mode: f$_{CLK}$ ≥ 1 MHz	0	100			kHz
Setup time of restart condition	t$_{SU:STA}$		4.7		0.6		μs
Hold time[Note 1]	t$_{HD:STA}$		4.0		0.6		μs
Hold time when SCLA0 = "L"	t$_{LOW}$		4.7		1.3		μs
Hold time when SCLA0 = "H"	t$_{HIGH}$		4.0		0.6		μs
Data setup time (reception)	t$_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	t$_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	t$_{SU:STO}$		4.0		0.6		μs
Bus-free time	t$_{BUF}$		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R>   **2.** The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.
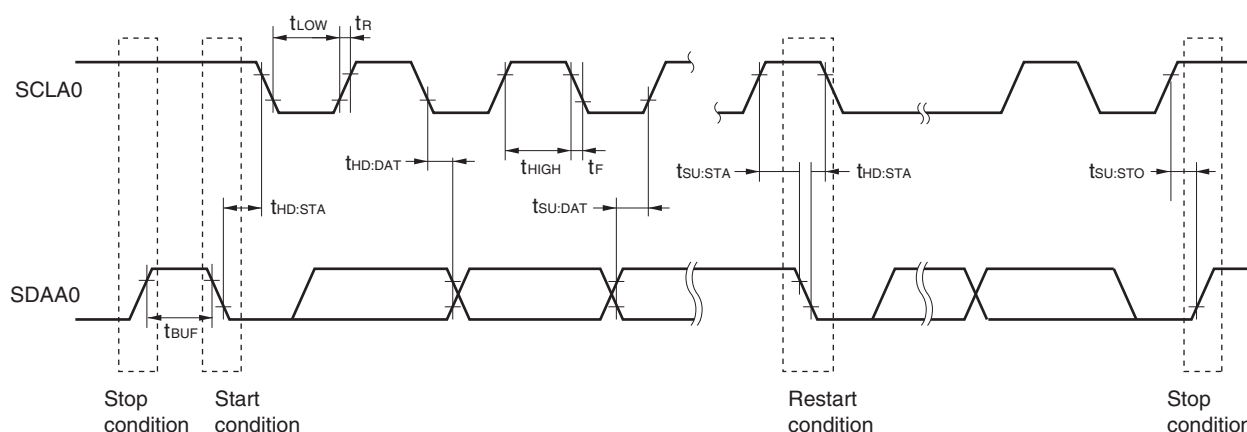
Caution Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I$_{OH1}$, I$_{OL1}$, V$_{OH1}$, V$_{OL1}$) must satisfy the values in the redirect destination.

Remark The maximum value of C$_b$ (communication line capacitance) and the value of R$_b$ (communication line pull-up resistor) at that time in each mode are as follows.

     Normal mode: C$_b$ = 400 pF, R$_b$ = 2.7 kΩ
     Fast mode: C$_b$ = 320 pF, R$_b$ = 1.1 kΩ

IICA serial transfer timing

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Notes 1. Excludes quantization error ($\pm$1/2 LSB).

      2. This value is indicated as a ratio (%FSR) to the full-scale value.

      3. When AV$_{REFP}$ < V$_{DD}$, the MAX. values are as follows.

          Overall error: Add $\pm$1.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

          Zero-scale error/Full-scale error: Add $\pm$0.05%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

          Integral linearity error/ Differential linearity error: Add $\pm$0.5 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

      4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

      5. Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22

(T$_A$ = −40 to +85°C, 1.8 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (−) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$			8		10	bit
Overall error [Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]			1.2	$\pm$5.0	LSB
					1.2	$\pm$8.5 [Note 4]	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target ANI pin: ANI16 to ANI22	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
				57		95	μs
Zero-scale error [Notes 1, 2]	EZS	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]				$\pm$0.35	%FSR
						$\pm$0.60 [Note 4]	%FSR
Full-scale error [Notes 1, 2]	EFS	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]				$\pm$0.35	%FSR
						$\pm$0.60 [Note 4]	%FSR
Integral linearity error [Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]				$\pm$3.5	LSB
						$\pm$6.0 [Note 4]	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]				$\pm$2.0	LSB
						$\pm$2.5 [Note 4]	LSB
Analog input voltage	V$_{AIN}$	ANI16 to ANI22		0		AV$_{REFP}$ and V$_{DD}$	V

Notes 1. Excludes quantization error ($\pm$1/2 LSB).

      2. This value is indicated as a ratio (%FSR) to the full-scale value.

      3. When AV$_{REFP}$ ≤ V$_{DD}$, the MAX. values are as follows.

          Overall error: Add $\pm$4.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

          Zero-scale error/Full-scale error: Add $\pm$0.20%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

          Integral linearity error/ Differential linearity error: Add $\pm$2.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

      4. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

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2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T$_A$ = −40 to +85°C, V$_{PDR}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	V$_{LVD0}$	Power supply rise time	3.98	4.06	4.14	V
		Power supply fall time	3.90	3.98	4.06	V
	V$_{LVD1}$	Power supply rise time	3.68	3.75	3.82	V
		Power supply fall time	3.60	3.67	3.74	V
	V$_{LVD2}$	Power supply rise time	3.07	3.13	3.19	V
		Power supply fall time	3.00	3.06	3.12	V
	V$_{LVD3}$	Power supply rise time	2.96	3.02	3.08	V
		Power supply fall time	2.90	2.96	3.02	V
	V$_{LVD4}$	Power supply rise time	2.86	2.92	2.97	V
		Power supply fall time	2.80	2.86	2.91	V
	V$_{LVD5}$	Power supply rise time	2.76	2.81	2.87	V
		Power supply fall time	2.70	2.75	2.81	V
	V$_{LVD6}$	Power supply rise time	2.66	2.71	2.76	V
		Power supply fall time	2.60	2.65	2.70	V
	V$_{LVD7}$	Power supply rise time	2.56	2.61	2.66	V
		Power supply fall time	2.50	2.55	2.60	V
	V$_{LVD8}$	Power supply rise time	2.45	2.50	2.55	V
		Power supply fall time	2.40	2.45	2.50	V
	V$_{LVD9}$	Power supply rise time	2.05	2.09	2.13	V
		Power supply fall time	2.00	2.04	2.08	V
	V$_{LVD10}$	Power supply rise time	1.94	1.98	2.02	V
		Power supply fall time	1.90	1.94	1.98	V
	V$_{LVD11}$	Power supply rise time	1.84	1.88	1.91	V
		Power supply fall time	1.80	1.84	1.87	V
Minimum pulse width	t$_{LW}$		300			µs
Detection delay time					300	µs

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(2) 30-pin products

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)   (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (High-speed main) mode [Note 6]	f$_{IH}$ = 24 MHz [Note 4]	V$_{DD}$ = 5.0 V		440	2300	μA
					V$_{DD}$ = 3.0 V		440	2300	
				f$_{IH}$ = 16 MHz [Note 4]	V$_{DD}$ = 5.0 V		400	1700	μA
					V$_{DD}$ = 3.0 V		400	1700	
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		190	1020	μA
					Resonator connection		260	1100	
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		190	1020	μA
					Resonator connection		260	1100	
	I$_{DD3}$ [Note 5]	STOP mode	T$_A$ = −40°C				0.18	0.50	μA
			T$_A$ = +25°C				0.23	0.50	
			T$_A$ = +50°C				0.30	1.10	
			T$_A$ = +70°C				0.46	1.90	
			T$_A$ = +85°C				0.75	3.30	
			T$_A$ = +105°C				2.94	15.30	

Notes 1. Total current flowing into V$_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$ or V$_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator clock is stopped.

4. When high-speed system clock is stopped.

5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: V$_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz

V$_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
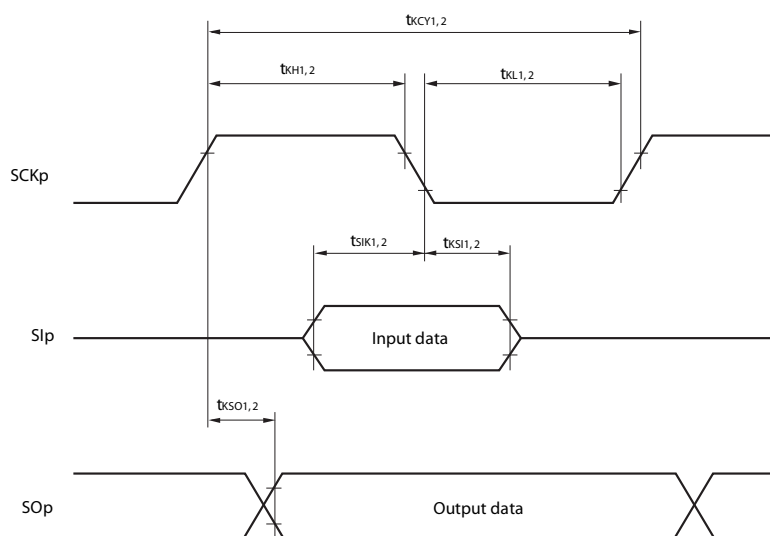
2. f$_{IH}$: high-speed on-chip oscillator clock frequency

3. Except STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C.

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CSI mode serial transfer timing (during communication at same potential)
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**
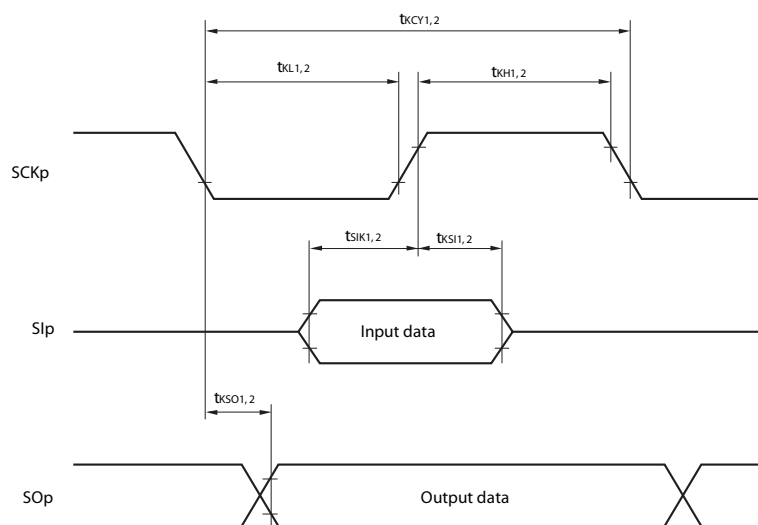
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)

    2. f$_{MCK}$: Serial array unit operation clock frequency

     (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0,1), n: Channel number (n = 0, 1, 3))

(4) During communication at same potential (simplified I²C mode)

(T_A = −40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	C_b = 100 pF, R_b = 3 kΩ		100 [Note 1]	kHz
Hold time when SCLr = "L"	t_{LOW}	C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 580 [Note 2]		ns
Data hold time (transmission)	$t_{HD:DAT}$	C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Notes **1.**   The value must also be equal to or less than f_{MCK}/4.

        2.   Set $t_{SU:DAT}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

Caution   Select the N-ch open drain output (V_{DD} tolerance) mode for SDAr by using port output mode register h (POMh).

Simplified I²C mode connection diagram (during communication at same potential)
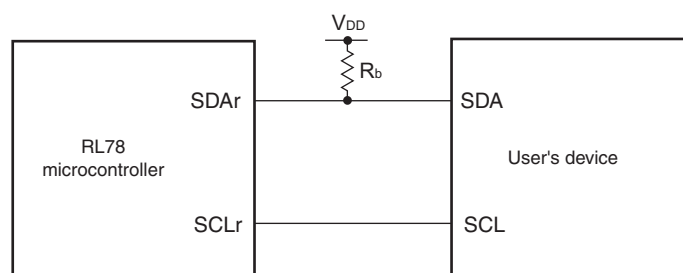
Simplified I²C mode serial transfer timing (during communication at same potential)
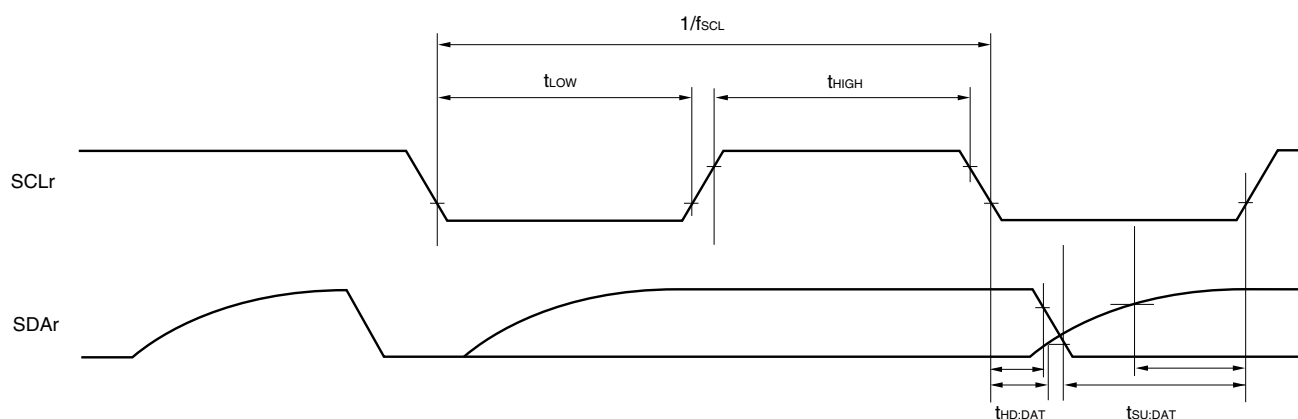
Remarks 1. R_b [Ω]:Communication line (SDAr) pull-up resistance

           C_b [F]: Communication line (SCLr, SDAr) load capacitance

      2.   r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1, 4, 5)

      3. f_{MCK}: Serial array unit operation clock frequency

           (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

           m: Unit number (m = 0, 1), n: Channel number (0, 1, 3))

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = −40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time [Note 1]	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	$24/f_{MCK}$		ns
			8 MHz < f_{MCK} ≤ 20 MHz	$20/f_{MCK}$		ns
			4 MHz < f_{MCK} ≤ 8 MHz	$16/f_{MCK}$		ns
			f_{MCK} ≤ 4 MHz	$12/f_{MCK}$		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	$32/f_{MCK}$		ns
			16 MHz < f_{MCK} ≤ 20 MHz	$28/f_{MCK}$		ns
			8 MHz < f_{MCK} ≤ 16 MHz	$24/f_{MCK}$		ns
			4 MHz < f_{MCK} ≤ 8 MHz	$16/f_{MCK}$		ns
			f_{MCK} ≤ 4 MHz	$12/f_{MCK}$		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	20 MHz < f_{MCK} ≤ 24 MHz	$72/f_{MCK}$		ns
			16 MHz < f_{MCK} ≤ 20 MHz	$64/f_{MCK}$		ns
			8 MHz < f_{MCK} ≤ 16 MHz	$52/f_{MCK}$		ns
			4 MHz < f_{MCK} ≤ 8 MHz	$32/f_{MCK}$		ns
			f_{MCK} ≤ 4 MHz	$20/f_{MCK}$		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		$t_{KCY2}/2 − 24$		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		$t_{KCY2}/2 − 36$		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		$t_{KCY2}/2 − 100$		ns
SIp setup time (to SCKp↑) [Note 2]	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_{DD} ≤ 4.0 V		$1/f_{MCK} + 40$		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		$1/f_{MCK} + 40$		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_{DD} ≤ 2.0 V		$1/f_{MCK} + 60$		ns
SIp hold time (from SCKp↑) [Note 3]	t_{KSI2}			$1/f_{MCK} + 62$		ns
Delay time from SCKp↓ to SOp output [Note 4]	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			$2/f_{MCK} + 240$	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			$2/f_{MCK} + 428$	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			$2/f_{MCK} + 1146$	ns

Notes 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Cautions 1. Select the TTL input buffer for the SIp and SCKp pins and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

2. CSI01 and CSI11 cannot communicate at different potential.

3.5.2 Serial interface IICA

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode: f$_{CLK}$ ≥ 3.5 MHz			0	400	kHz
		Normal mode: f$_{CLK}$ ≥ 1 MHz	0	100			kHz
Setup time of restart condition	t$_{SU:STA}$		4.7		0.6		µs
Hold time[Note 1]	t$_{HD:STA}$		4.0		0.6		µs
Hold time when SCLA0 = "L"	t$_{LOW}$		4.7		1.3		µs
Hold time when SCLA0 = "H"	t$_{HIGH}$		4.0		0.6		µs
Data setup time (reception)	t$_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	t$_{HD:DAT}$		0	3.45	0	0.9	µs
Setup time of stop condition	t$_{SU:STO}$		4.0		0.6		µs
Bus-free time	t$_{BUF}$		4.7		1.3		µs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R>   **2.** The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution   Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I$_{OH1}$, I$_{OL1}$, V$_{OH1}$, V$_{OL1}$) must satisfy the values in the redirect destination.

Remark   The maximum value of C$_b$ (communication line capacitance) and the value of R$_b$ (communication line pull-up resistor) at that time in each mode are as follows.

     Normal mode: C$_b$ = 400 pF, R$_b$ = 2.7 kΩ
     Fast mode: C$_b$ = 320 pF, R$_b$ = 1.1 kΩ

IICA serial transfer timing

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