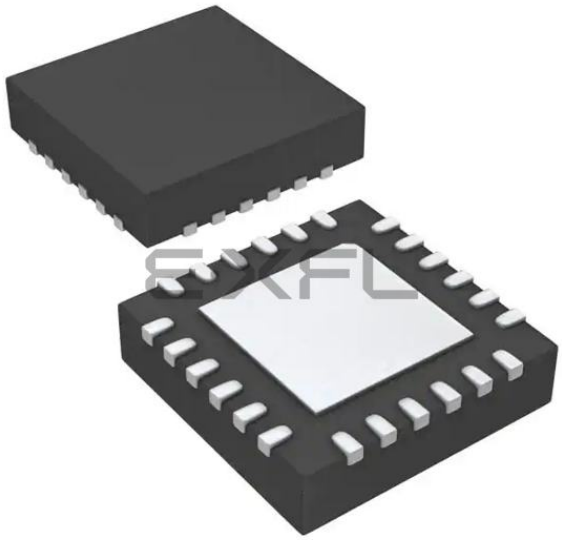

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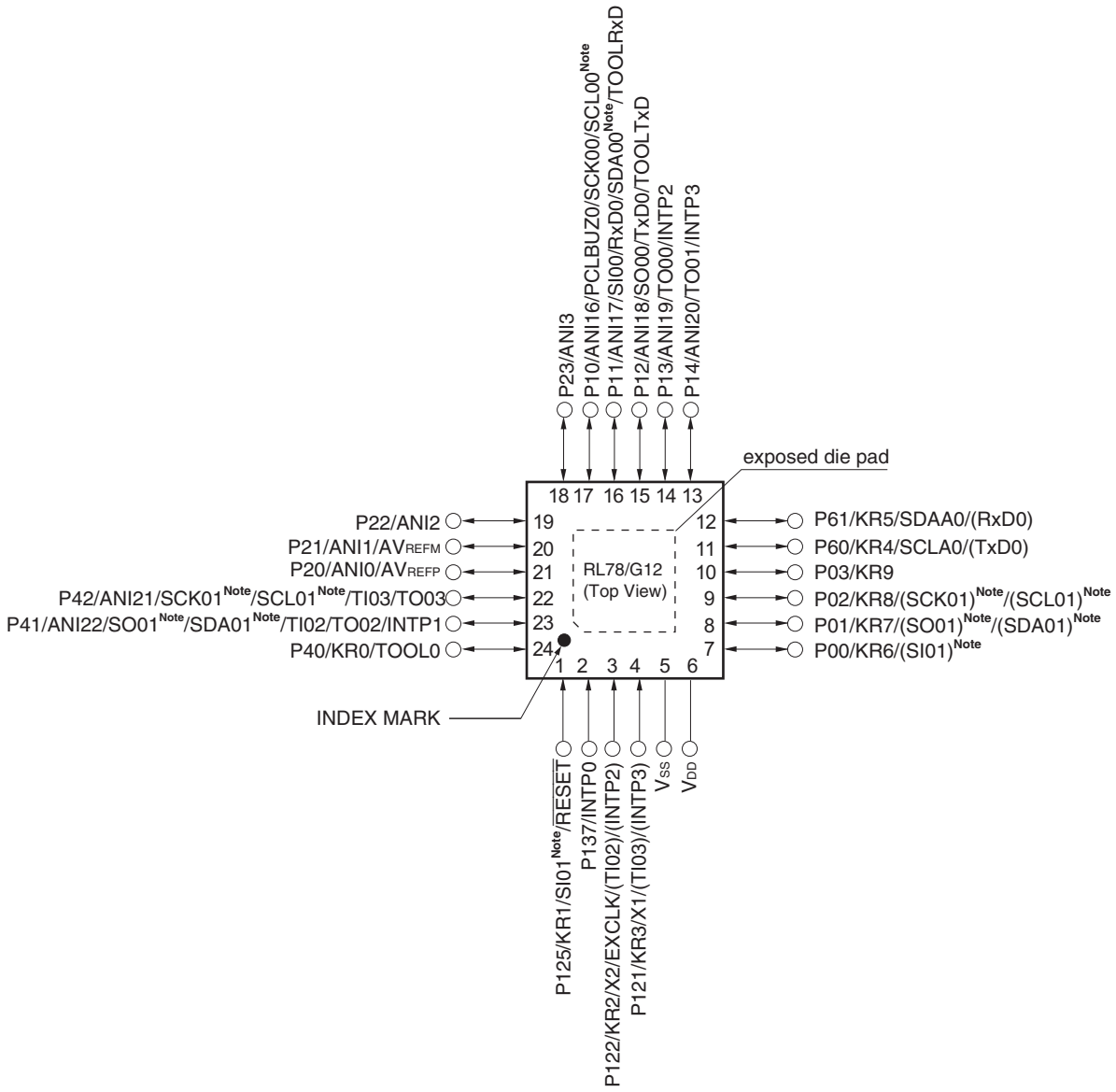
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-HWQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10277ana-u5

1.4.2 24-pin products

<R> • 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)



Note Provided only in the R5F102 products.

Remarks 1. For pin identification, see **1.5 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

3. It is recommended to connect an exposed die pad to Vss.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			−0.5 to + 6.5	V
REGC terminal input voltage[Note1]	V_{IREGC}	REGC		−0.3 to +2.8 and −0.3 to V_{DD} + 0.3 [Note 2]	V
Input Voltage	V_{I1}	Other than P60, P61		−0.3 to V_{DD} + 0.3[Note 3]	V
	V_{I2}	P60, P61 (N-ch open drain)		−0.3 to 6.5	V
Output Voltage	V_O			−0.3 to V_{DD} + 0.3[Note 3]	V
Analog input voltage	V_{AI}	20-, 24-pin products: ANI0 to ANI3, ANI16 to ANI22 30-pin products: ANI0 to ANI3, ANI16 to ANI19		−0.3 to V_{DD} + 0.3 and −0.3 to AVREF(+)+0.3[Notes 3, 4]	V
Output current, high	I_{OH1}	Per pin	Other than P20 to P23	−40	mA
		Total of all pins	All the terminals other than P20 to P23	−170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	−70	mA
			20-, 24-pin products: P00 to P03[Note 5], P10 to P14 30-pin products: P10 to P17, P30, P31, P50, P51, P147	−100	mA
	I_{OH2}	Per pin	P20 to P23	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	Other than P20 to P23	40	mA
		Total of all pins	All the terminals other than P20 to P23	170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	70	mA
			20-, 24-pin products: P00 to P03[Note 5], P10 to P14, P60, P61 30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147	100	mA
	I_{OL2}	Per pin	P20 to P23	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Notes 1. 30-pin product only.

2. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.

3. Must be 6.5 V or lower.

4. Do not exceed $AV_{REF}(+)$ + 0.3 V in case of A/D conversion target pin.

5. 24-pin products only.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF}(+)$: + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

(2) 30-pin products

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (High-speed main) mode Note 4	f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.5		mA
						V_{DD} = 3.0 V		1.5		
					Normal operation	V_{DD} = 5.0 V		3.7	5.5	mA
						V_{DD} = 3.0 V		3.7	5.5	
				f_{IH} = 16 MHz Note 3		V_{DD} = 5.0 V		2.7	4.0	mA
						V_{DD} = 3.0 V		2.7	4.0	
			LS (Low-speed main) mode Note 4	f_{IH} = 8 MHz Note 3		V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	
			HS (High-speed main) mode Note 4	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V		Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V		Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V		Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V		Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
			LS (Low-speed main) mode Note 4	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.

3. When high-speed system clock is stopped

4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS(Low speed main) mode: V_{DD} = 1.8 V to 5.5 V @1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C.

(2) 30-pin products

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (High-speed main) mode Note 6	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		440	1280	μA
					V_{DD} = 3.0 V		440	1280	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		400	1000	μA
					V_{DD} = 3.0 V		400	1000	
			LS (Low-speed main) mode Note 6	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		260	530	μA
					V_{DD} = 2.0 V		260	530	
			HS (High-speed main) mode Note 6	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		280	1000	μA
					Resonator connection		450	1170	
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		280	1000	μA
					Resonator connection		450	1170	
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		190	600	μA
					Resonator connection		260	670	
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		190	600	μA
					Resonator connection		260	670	
			LS (Low-speed main) mode Note 6	f_{MX} = 8 MHz Note 3, V_{DD} = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
				f_{MX} = 8 MHz Note 3 V_{DD} = 2.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
	I_{DD3} Note 5	STOP mode	T_A = –40°C				0.18	0.50	μA
			T_A = +25°C				0.23	0.50	
			T_A = +50°C				0.30	1.10	
			T_A = +70°C				0.46	1.90	
			T_A = +85°C				0.75	3.30	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator clock is stopped.

4. When high-speed system clock is stopped.

5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS (Low speed main) mode: V_{DD} = 1.8 V to 5.5 V @1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Except STOP mode, temperature condition of the TYP. value is T_A = 25°C.

2.4 AC Characteristics

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (High-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
		During self programming	HS (High-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V_{DD} < 2.4 V			1.0		8.0	MHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
		1.8 V ≤ V_{DD} < 2.4 V			60			ns
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK} + 10			ns
TO00 to TO07 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V					12	MHz
		2.7 V ≤ V_{DD} < 4.0 V					8	MHz
		1.8 V ≤ V_{DD} < 2.7 V					4	MHz
PCLBUZ0, or PCLBUZ1 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V					16	MHz
		2.7 V ≤ V_{DD} < 4.0 V					8	MHz
		1.8 V ≤ V_{DD} < 2.7 V					4	MHz
INTP0 to INTP5 input high-level width, low-level width	t_{INTH}, t_{INTL}				1			μs
KR0 to KR9 input available width	t_{KR}				250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	167		500		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	250		500		ns
			1.8 V ≤ V_{DD} ≤ 5.5 V	–		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2−12		t_{KCY1}/2−50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2−18		t_{KCY1}/2−50		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2−38		t_{KCY1}/2−50		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		–		t_{KCY1}/2−50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		44		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		44		110		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		75		110		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		–		110		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note4			25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products.))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note4	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		–		ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	16 MHz < f_{MCK}	8/f_{MCK}		–		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		–		6/f_{MCK} and 750		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2−7		t_{KCY2}/2−7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2−8		t_{KCY2}/2−8		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2−18		t_{KCY2}/2−18		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		–		t_{KCY2}/2−18		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		–		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note4	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 44		2/f_{MCK} + 110	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 75		2/f_{MCK} + 110	ns
			1.8 V ≤ V_{DD} ≤ 5.5 V		–		2/f_{MCK} + 110	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

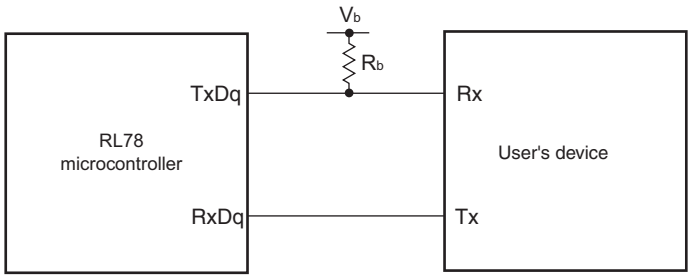
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

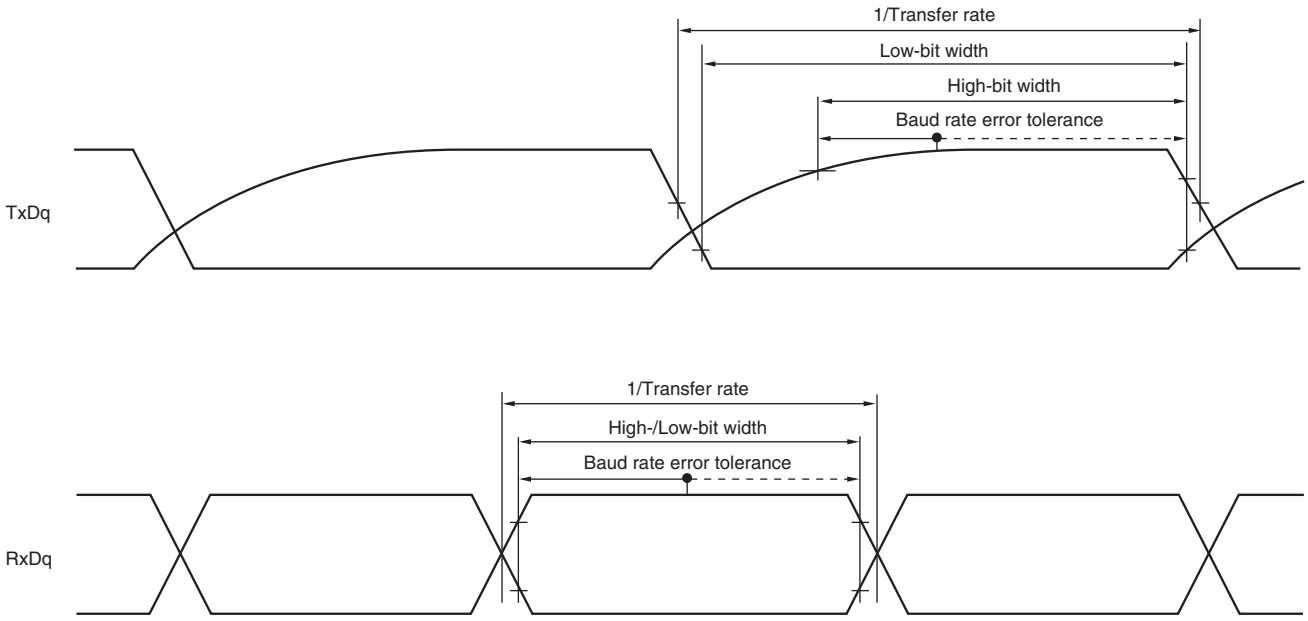
5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remarks 1. R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

4. UART0 of the 20- and 24-pin products supports communication at different potential only when the peripheral I/O redirection function is not used.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		ns
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 −75		t_{KCY1}/2−75		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 −170		t_{KCY1}/2−170		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 −458		t_{KCY1}/2−458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 −12		t_{KCY1}/2−50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 −18		t_{KCY1}/2−50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 −50		t_{KCY1}/2−50		ns

Note Use it with $V_{DD} \geq V_b$.

Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

2. CSI01 and CSI11 cannot communicate at different potential.

Remarks 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSI number (p = 00, 20)

2.9 Dedicated Flash Memory Programmer Communication (UART)

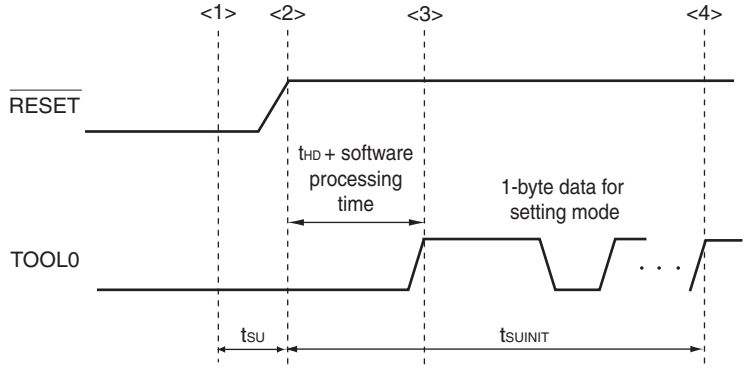
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset are released before external reset release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset are released before external reset release	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset are released before external reset release	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	20-, 24-pin products: Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42 30-pin products: Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147				8.5 [Note 2]	mA
		Per pin for P60, P61				15.0 [Note 2]	mA
		20-, 24-pin products: Total of P40 to P42 30-pin products: Total of P00, P01, P40, P120 (When duty ≤ 70% [Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			25.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			9.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			1.8	mA
		20-, 24-pin products: Total of P00 to P03[Note 4], P10 to P14, P60, P61 30-pin products: Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147 (When duty ≤ 70% [Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			27.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			5.4	mA
		Total of all pins (When duty ≤ 70% [Note 3])				65.5	mA
	I_{OL2}	Per pin for P20 to P23				0.4	mA
		Total of all pins				1.6	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. The output current value under conditions where the duty factor ≤ 70%.
If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. 24-pin products only.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.4 AC Characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (High-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
		During self programming	HS (High-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	MHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK} + 10			ns
TO00 to TO07 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V					12	MHz
		2.7 V ≤ V_{DD} < 4.0 V					8	MHz
		2.4 V ≤ V_{DD} < 2.7 V					4	MHz
PCLBUZ0, or PCLBUZ1 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V					16	MHz
		2.7 V ≤ V_{DD} < 4.0 V					8	MHz
		2.4 V ≤ V_{DD} < 2.7 V					4	MHz
INTP0 to INTP5 input high-level width, low-level width	t_{INTH}, t_{INTL}				1			μs
KR0 to KR9 input available width	t_{KR}				250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	334		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2–24		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2–36		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2–76		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		66		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		66		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		113		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			38		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note4			50	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate Note4		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps
		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		**Note 3**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.0 Note 4	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V,		**Note 5**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 6	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		**Notes 2, 7**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 8	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

3. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	600		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	1000		ns
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	2300		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 –150		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 –340		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 –916		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 –24		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 –36		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 –100		ns

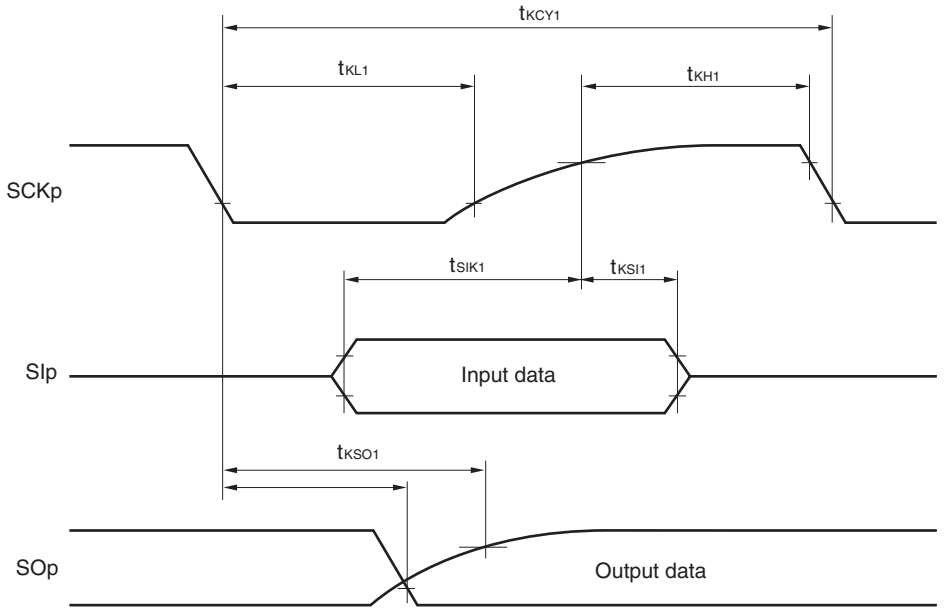
Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

2. CSI01 and CSI11 cannot communicate at different potential.

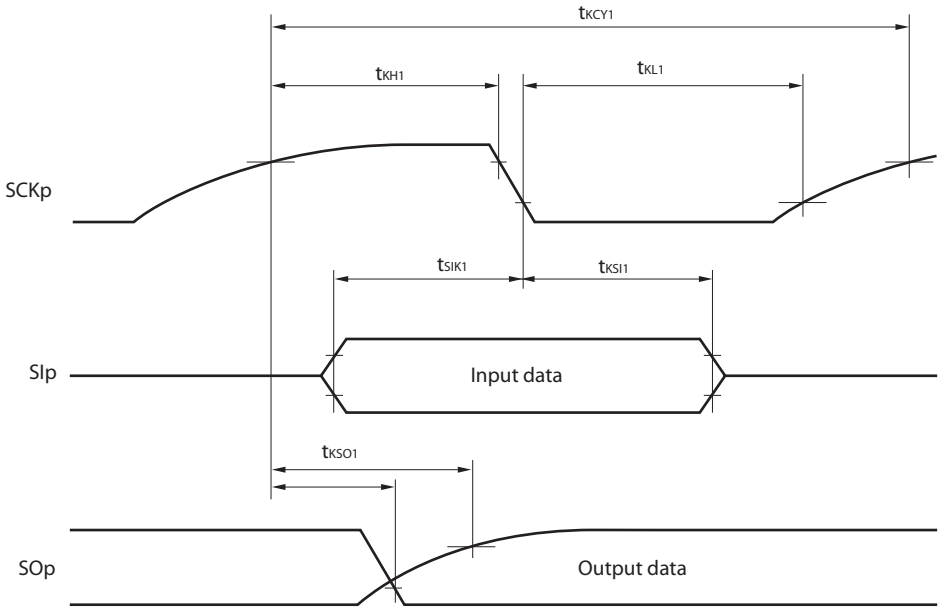
Remarks 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSI number (p = 00, 20)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22

(T_A = –40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error Note 1	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3			1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI22	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3				±0.35	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3				±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3				±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ Note 3				±2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI22		0		AV_{REFP} and V_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

3.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +105°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	V_{LVD0}	Power supply rise time	3.90	4.06	4.22	V
		Power supply fall time	3.83	3.98	4.13	V
	V_{LVD1}	Power supply rise time	3.60	3.75	3.90	V
		Power supply fall time	3.53	3.67	3.81	V
	V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
		Power supply fall time	2.94	3.06	3.18	V
	V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
		Power supply fall time	2.85	2.96	3.07	V
	V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
		Power supply fall time	2.75	2.86	2.97	V
	V_{LVD5}	Power supply rise time	2.70	2.81	2.92	V
		Power supply fall time	2.64	2.75	2.86	V
	V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
		Power supply fall time	2.55	2.65	2.75	V
	V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
		Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width	t_{LW}		300			μs
Detection delay time					300	μs

LVD detection voltage of interrupt & reset mode

(T_A = –40 to +105°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC1} = 0, 1, 1, falling reset voltage			2.64	2.75	2.86	V
	V_{LVDD1}		LVIS1, LVIS0 = 1, 0	Rising reset release voltage	2.81	2.92	3.03	V
				Falling interrupt voltage	2.75	2.86	2.97	V
	V_{LVDD2}		LVIS1, LVIS0 = 0, 1	Rising reset release voltage	2.90	3.02	3.14	V
				Falling interrupt voltage	2.85	2.96	3.07	V
	V_{LVDD3}		LVIS1, LVIS0 = 0, 0	Rising reset release voltage	3.90	4.06	4.22	V
				Falling interrupt voltage	3.83	3.98	4.13	V

3.6.5 Power supply voltage rising slope characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

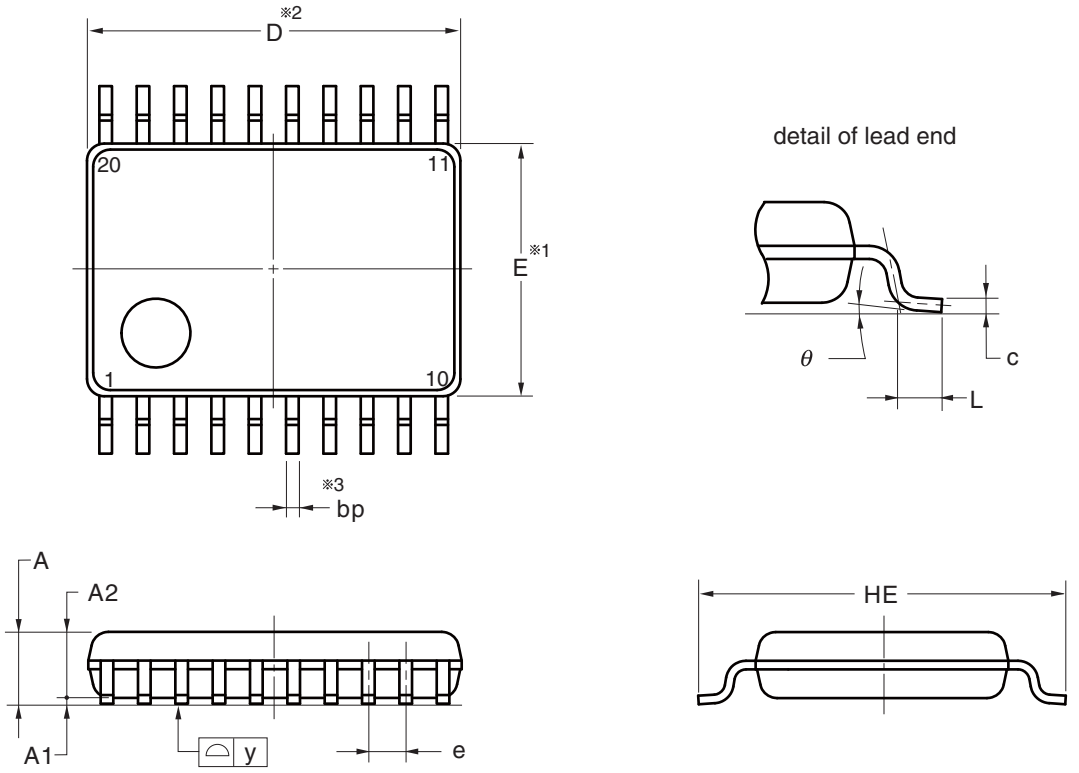
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 29.4 AC Characteristics.

4. PACKAGE DRAWINGS

4.1 20-pin products

R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP
R5F1036AASP, R5F10369ASP, R5F10368ASP, R5F10367ASP, R5F10366ASP
R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP
R5F1036ADSP, R5F10369DSP, R5F10368DSP, R5F10367DSP, R5F10366DSP
<R> R5F1026AGSP, R5F10269GSP, R5F10268GSP, R5F10267GSP, R5F10266GSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1



(UNIT:mm)

ITEM	DIMENSIONS
D	6.50±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.45 MAX.
A1	0.10±0.10
A2	1.15
e	0.65±0.12
bp	$0.22^{+0.10}_{-0.05}$
c	$0.15^{+0.05}_{-0.02}$
L	0.50±0.20
y	0.10
θ	0° to 10°

NOTE

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.