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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

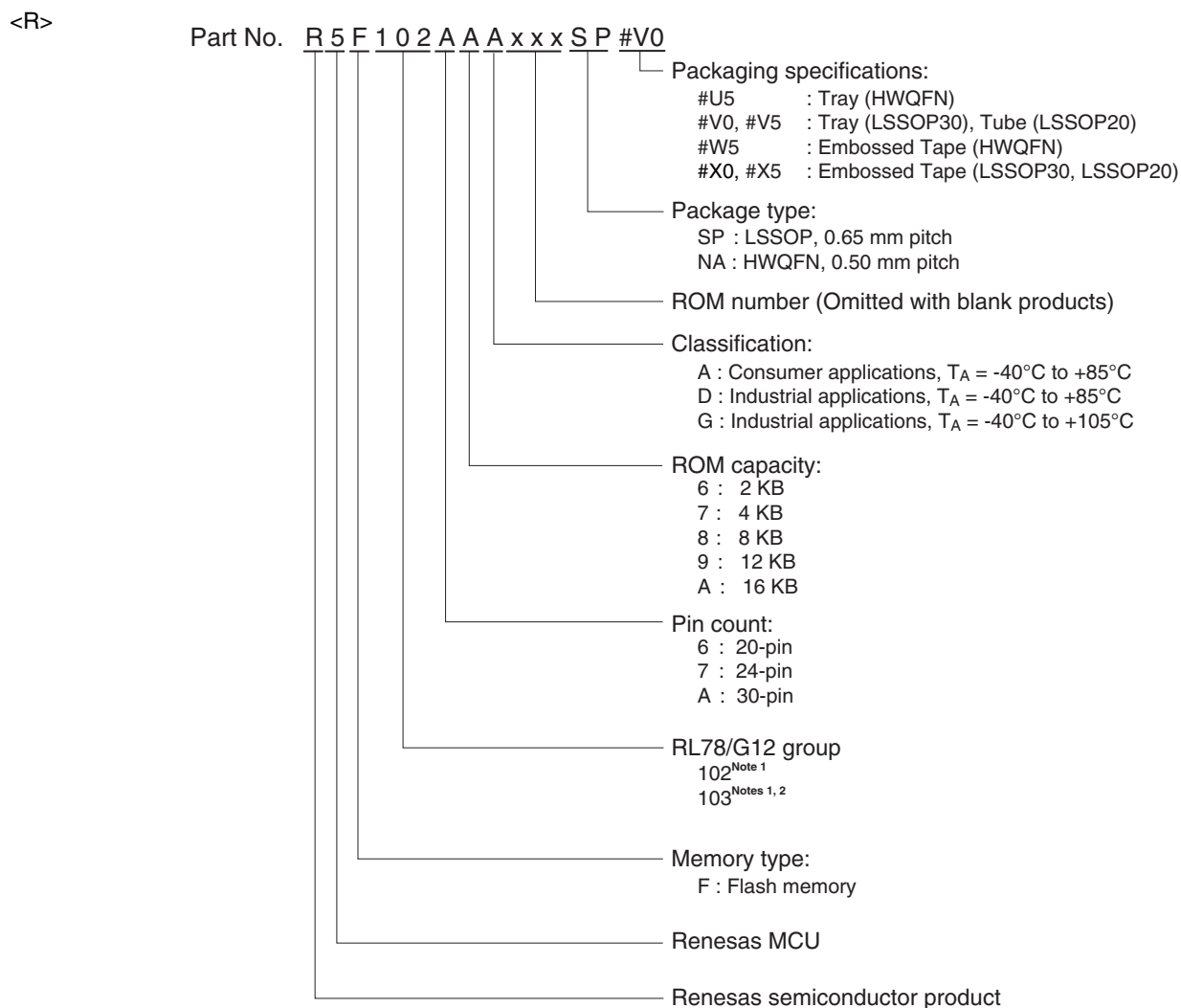
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-HWQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10278ana-u5

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G12



- Notes**
- For details about the differences between the R5F102 products and the R5F103 products of RL78/G12, see **1.1 Differences between the R5F102 Products and the R5F103 Products**.
 - Products only for "A: Consumer applications ($T_A = -40$ to $+85^{\circ}\text{C}$)" and "D: Industrial applications ($T_A = -40$ to $+85^{\circ}\text{C}$)"

1.3 Differences between the R5F102 Products and the R5F103 Products

The following are differences between the R5F102 products and the R5F103 products.

- Whether the data flash memory is mounted or not
- High-speed on-chip oscillator oscillation frequency accuracy
- Number of channels in serial interface
- Whether the DMA function is mounted or not
- Whether a part of the safety functions are mounted or not

1.3.1 Data Flash

The data flash memory of 2 KB is mounted on the R5F102 products, but not on the R5F103 products.

Product	Data Flash
R5F102 products R5F1026A, R5F1027A, R5F102AA, R5F10269, R5F10279, R5F102A9, R5F10268, R5F10278, R5F102A8, R5F10267, R5F10277, R5F102A7, R5F10266 ^{Note}	2KB
R5F103 products R5F1036A, R5F1037A, R5F103AA, R5F10369, R5F10379, R5F103A9, R5F10368, R5F10378 R5F103A8, R5F10367, R5F10377, R5F103A7, R5F10366	Not mounted

Note The RAM in the R5F10266 has capacity as small as 256 bytes. Depending on the customer's program specification, the stack area to execute the data flash library may not be kept and data may not be written to or erased from the data flash memory.

Caution When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			-0.5 to $+6.5$	V
REGC terminal input voltage ^{Note 1}	V_{IREGC}	REGC		-0.3 to $+2.8$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Input Voltage	V_{I1}	Other than P60, P61		-0.3 to $V_{DD} + 0.3$ ^{Note 3}	V
	V_{I2}	P60, P61 (N-ch open drain)		-0.3 to 6.5	V
Output Voltage	V_O			-0.3 to $V_{DD} + 0.3$ ^{Note 3}	V
Analog input voltage	V_{AI}	20-, 24-pin products: ANI0 to ANI3, ANI16 to ANI22 30-pin products: ANI0 to ANI3, ANI16 to ANI19		-0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF}(+) + 0.3$ ^{Notes 3, 4}	V
Output current, high	I_{OH1}	Per pin	Other than P20 to P23	-40	mA
		Total of all pins	All the terminals other than P20 to P23	-170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	-70	mA
			20-, 24-pin products: P00 to P03 ^{Note 5} , P10 to P14 30-pin products: P10 to P17, P30, P31, P50, P51, P147	-100	mA
	I_{OH2}	Per pin	P20 to P23	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I_{OL1}	Per pin	Other than P20 to P23	40	mA
		Total of all pins	All the terminals other than P20 to P23	170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	70	mA
			20-, 24-pin products: P00 to P03 ^{Note 5} , P10 to P14, P60, P61 30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147	100	mA
	I_{OL2}	Per pin	P20 to P23	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A			-40 to $+85$	$^{\circ}\text{C}$
Storage temperature	T_{stg}			-65 to $+150$	$^{\circ}\text{C}$

Notes 1. 30-pin product only.

2. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.
3. Must be 6.5 V or lower.
4. Do not exceed $AV_{REF}(+) + 0.3$ V in case of A/D conversion target pin.
5. 24-pin products only.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks** 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
2. $AV_{REF}(+)$: + side reference voltage of the A/D converter.
 3. V_{SS} : Reference voltage

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

(3/4)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	Normal input buffer 20-, 24-pin products: P00 to P03 ^{Note 2} , P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	0.8V _{DD}		V _{DD}	V
	V _{IH2}	TTL input buffer 20-, 24-pin products: P10, P11 30-pin products: P01, P10, P11, P13 to P17	4.0 V ≤ V _{DD} ≤ 5.5 V	2.2	V _{DD}	V
			3.3 V ≤ V _{DD} < 4.0 V	2.0	V _{DD}	V
			1.8 V ≤ V _{DD} < 3.3 V	1.5	V _{DD}	V
	V _{IH3}	P20 to P23	0.7V _{DD}		V _{DD}	V
	V _{IH4}	P60, P61	0.7V _{DD}		6.0	V
	V _{IH5}	P121, P122, P125 ^{Note 1} , P137, EXCLK, RESET	0.8V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}	Normal input buffer 20-, 24-pin products: P00 to P03 ^{Note 2} , P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	0		0.2V _{DD}	V
	V _{IL2}	TTL input buffer 20-, 24-pin products: P10, P11 30-pin products: P01, P10, P11, P13 to P17	4.0 V ≤ V _{DD} ≤ 5.5 V	0	0.8	V
			3.3 V ≤ V _{DD} < 4.0 V	0	0.5	V
			1.8 V ≤ V _{DD} < 3.3 V	0	0.32	V
	V _{IL3}	P20 to P23	0		0.3V _{DD}	V
	V _{IL4}	P60, P61	0		0.3V _{DD}	V
	V _{IL5}	P121, P122, P125 ^{Note 1} , P137, EXCLK, RESET	0		0.2V _{DD}	V
Output voltage, high	V _{OH1}	20-, 24-pin products: P00 to P03 ^{Note 2} , P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	4.0 V ≤ V _{DD} ≤ 5.5 V, I _{OH1} = –10.0 mA	V _{DD} –1.5		V
			4.0 V ≤ V _{DD} ≤ 5.5 V, I _{OH1} = –3.0 mA	V _{DD} –0.7		V
			2.7 V ≤ V _{DD} ≤ 5.5 V, I _{OH1} = –2.0 mA	V _{DD} –0.6		V
			1.8 V ≤ V _{DD} ≤ 5.5 V, I _{OH1} = –1.5 mA	V _{DD} –0.5		V
	V _{OH2}	P20 to P23	I _{OH2} = –100 μA	V _{DD} –0.5		V

Notes 1. 20, 24-pin products only.

2. 24-pin products only.

Caution The maximum value of V_{IH} of pins P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products is V_{DD} even in N-ch open-drain mode. High level is not output in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) During communication at same potential (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCK00 cycle time	t _{KCY1}	t _{KCY1} ≥ 2/f _{CLK}	83.3		250		ns
SCK00 high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2–7		t _{KCY1} /2–50		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2–10		t _{KCY1} /2–50		ns
SI00 setup time (to SCK00↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V	23		110		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V	33		110		ns
SI00 hold time (from SCK00↑) ^{Note 2}	t _{KSI1}		10		10		ns
Delay time from SCK00↓ to SO00 output ^{Note 3}	t _{KSO1}	C = 20 pF ^{Note 4}		10		10	ns

- Notes**
1. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 setup time becomes “to SCK00↓” when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.
 2. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 hold time becomes “from SCK00↓” when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.
 3. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The delay time to SO00 output becomes “from SCK00↑” when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.
 4. C is the load capacitance of the SCK00 and SO00 output lines.

Caution Select the normal input buffer for the SI00 pin and the normal output mode for the SO00 and SCK00 pins by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).

- Remarks**
1. This specification is valid only when CSI00's peripheral I/O redirect function is not used.
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS00 bit of serial mode register 00 (SMR00).)

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK}	2.7 V ≤ V _{DD} ≤ 5.5 V	167		500		ns
			2.4 V ≤ V _{DD} ≤ 5.5 V	250		500		ns
			1.8 V ≤ V _{DD} ≤ 5.5 V	–		500		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V		t _{KCY1} /2–12		t _{KCY1} /2–50		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V		t _{KCY1} /2–18		t _{KCY1} /2–50		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V		t _{KCY1} /2–38		t _{KCY1} /2–50		ns
		1.8 V ≤ V _{DD} ≤ 5.5 V		–		t _{KCY1} /2–50		ns
Slp setup time (to SCKp↑) <small>Note 1</small>	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V		44		110		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V		44		110		ns
		2.4 V ≤ V _{DD} ≤ 5.5 V		75		110		ns
		1.8 V ≤ V _{DD} ≤ 5.5 V		–		110		ns
Slp hold time (from SCKp↑) <small>Note 2</small>	t _{SH1}			19		19		ns
Delay time from SCKp↓ to SOp output <small>Note 3</small>	t _{KSO1}	C = 30 pF <small>Note 4</small>			25		25	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

- Remarks**
1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products.))

5. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 4** above to calculate the maximum transfer rate under conditions of the customer.

6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ and $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

8. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

9. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 8** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). **For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.**

- Notes**
1. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1
 2. When DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

Caution Select the TTL input buffer for the SI00 pin and the N-ch open drain output (V_{DD} tolerance) mode for the SO00 pin and SCK00 pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).
For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
1. R_b [Ω]: Communication line (SCK00, SO00) pull-up resistance, C_b [F]: Communication line (SCK00, SO00) load capacitance, V_b [V]: Communication line voltage
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS00 bit of serial mode register 00 (SMR00).)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

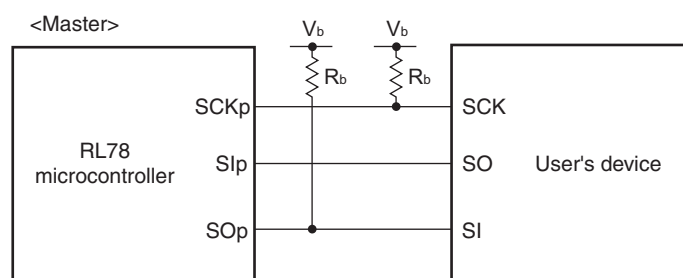
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	44		110		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	44		110		ns
		$1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note 2} , $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	110		110		ns
Slp hold time (from SCKp↓) ^{Note 1}	t_{KSI1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	19		19		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	19		19		ns
		$1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note 2} , $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	19		19		ns
Delay time from SCKp↑ to SOp output ^{Note 1}	t_{KSO1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		25		25	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		25		25	ns
		$1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note 2} , $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.2. Use it with $V_{DD} \geq V_b$.**Cautions** 1. Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

2. CSI01 and CSI11 cannot communicate at different potential.

Remarks 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

CSI mode connection diagram (during communication at different potential)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	20 MHz < f _{MCK} ≤ 24 MHz	12/f _{MCK}		—		ns
			8 MHz < f _{MCK} ≤ 20 MHz	10/f _{MCK}		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/f _{MCK}		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	20 MHz < f _{MCK} ≤ 24 MHz	16/f _{MCK}		—		ns
			16 MHz < f _{MCK} ≤ 20 MHz	14/f _{MCK}		—		ns
			8 MHz < f _{MCK} ≤ 16 MHz	12/f _{MCK}		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/f _{MCK}		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	20 MHz < f _{MCK} ≤ 24 MHz	36/f _{MCK}		—		ns
			16 MHz < f _{MCK} ≤ 20 MHz	32/f _{MCK}		—		ns
			8 MHz < f _{MCK} ≤ 16 MHz	26/f _{MCK}		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	10/f _{MCK}		10/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		t _{KCY2} /2 - 12		t _{KCY2} /2 - 50		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		t _{KCY2} /2 - 18		t _{KCY2} /2 - 50		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}		t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		ns
Slp setup time (to SCKp↑) ^{Note 3}	t _{SIK2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _{DD} ≤ 4.0 V		1/f _{MCK} + 20		1/f _{MCK} + 30		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		1/f _{MCK} + 20		1/f _{MCK} + 30		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _{DD} ≤ 2.0 V ^{Note 2}		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
Slp hold time (from SCKp↑) ^{Note 4}	t _{KSI2}			1/f _{MCK} + 31		1/f _{MCK} + 31		ns
Delay time from SCKp↓ to SOP output ^{Note 5}	t _{KSO2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			2/f _{MCK} + 120		2/f _{MCK} + 573	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			2/f _{MCK} + 214		2/f _{MCK} + 573	ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ			2/f _{MCK} + 573		2/f _{MCK} + 573	ns

Notes 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

2. Use it with V_{DD} ≥ V_b.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOP output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Cautions 1. Select the TTL input buffer for the Slp and SCKp pins and the N-ch open drain output (V_{DD} tolerance) mode for the SOP pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).

For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

2. CSI01 and CSI11 cannot communicate at different potential.

2.5.2 Serial interface IICA

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) mode LS (low-speed main) mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz			0	400	kHz
		Normal mode: f _{CLK} ≥ 1 MHz	0	100			kHz
Setup time of restart condition	t _{SU:STA}		4.7		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}		4.0		0.6		μs
Hold time when SCLA0 = “L”	t _{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t _{HIGH}		4.0		0.6		μs
Data setup time (reception)	t _{SU:DAT}		250		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		0	3.45	0	0.9	μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		μs
Bus-free time	t _{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

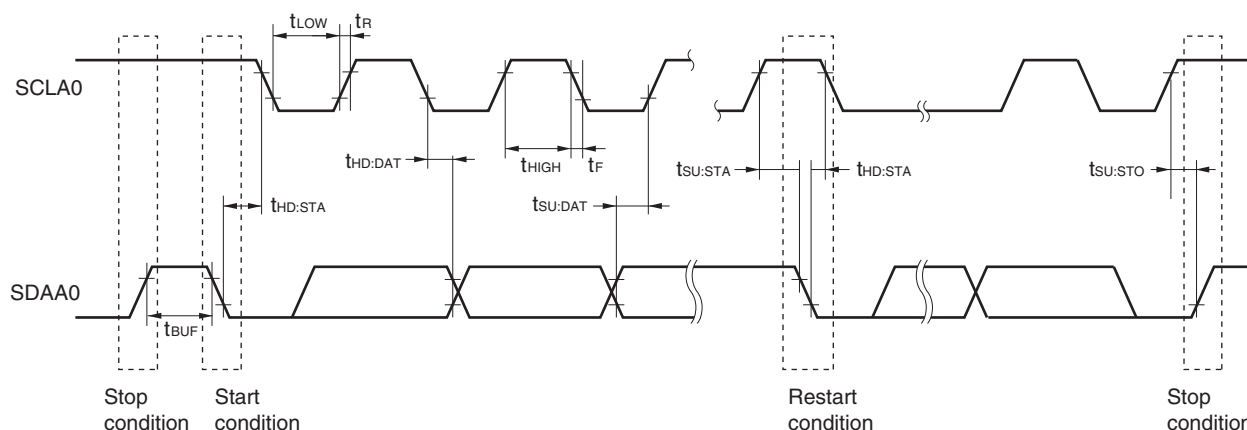
Caution Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1} , I_{OL1} , V_{OH1} , V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: $C_b = 400\text{ pF}$, $R_b = 2.7\text{ k}\Omega$

Fast mode: $C_b = 320\text{ pF}$, $R_b = 1.1\text{ k}\Omega$

IICA serial transfer timing



(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution			1.2	± 7.0	LSB
					1.2	± 10.5 ^{Note 3}	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
				57		95	μs
Conversion time	t_{CONV}	10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZX	10-bit resolution				± 0.60	%FSR
						± 0.85 ^{Note 3}	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution				± 0.60	%FSR
						± 0.85 ^{Note 3}	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution				± 4.0	LSB
						± 6.5 ^{Note 3}	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution				± 2.0	LSB
						± 2.5 ^{Note 3}	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI3, ANI16 to ANI22		0		V_{DD}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} ^{Note 4}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TSP25} ^{Note 4}			V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

2.6.2 Temperature sensor/internal reference voltage characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

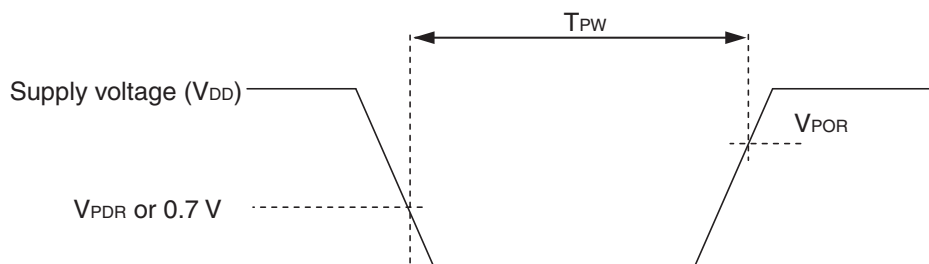
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/ $^\circ\text{C}$
Operation stabilization wait time	t_{AMP}		5			μs

2.6.3 POR circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width ^{Note}	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.9 Dedicated Flash Memory Programmer Communication (UART)

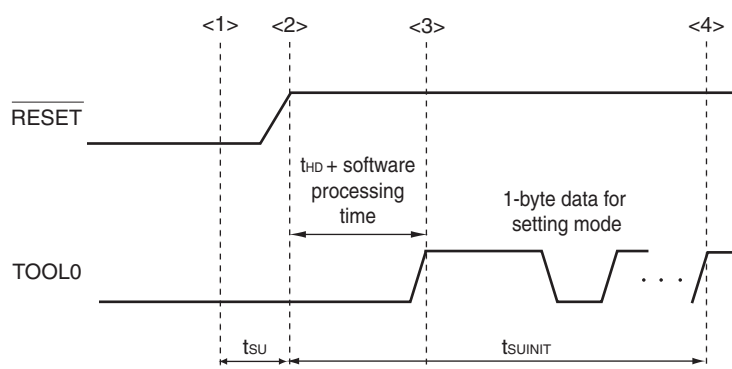
($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUNIT}	POR and LVD reset are released before external reset release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset are released before external reset release	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset are released before external reset release	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

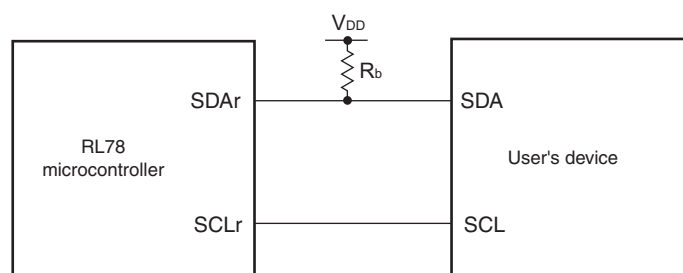
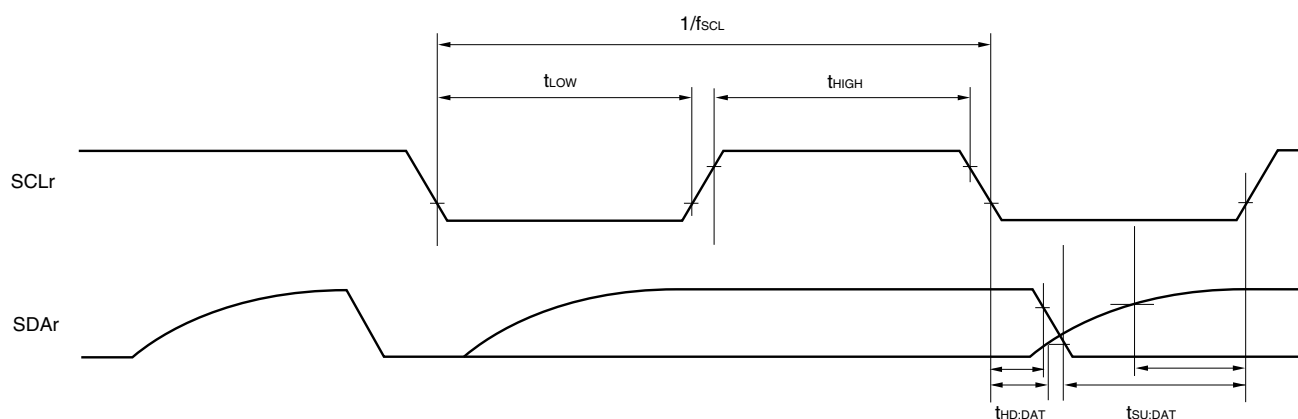
Remark t_{SUNIT} : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

(4) During communication at same potential (simplified I²C mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

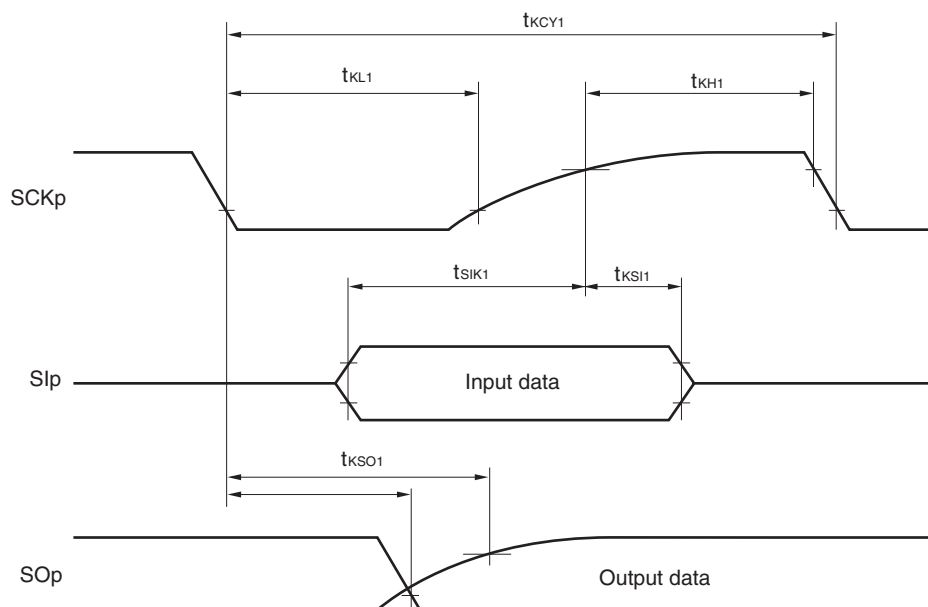
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	$C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$		100 ^{Note 1}	kHz
Hold time when SCLr = "L"	t_{LOW}	$C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	$C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Data setup time (reception)	$t_{\text{SU:DAT}}$	$C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 580$ ^{Note 2}		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	0	1420	ns

Notes 1. The value must also be equal to or less than $f_{\text{MCK}}/4$.**2.** Set $t_{\text{SU:DAT}}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".**Caution** Select the N-ch open drain output (V_{DD} tolerance) mode for SDAr by using port output mode register h (POMh).**Simplified I²C mode connection diagram (during communication at same potential)****Simplified I²C mode serial transfer timing (during communication at same potential)****Remarks 1.** R_b [Ω]: Communication line (SDAr) pull-up resistance C_b [F]: Communication line (SCLr, SDAr) load capacitance**2.** r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1, 4, 5)**3.** f_{MCK} : Serial array unit operation clock frequency

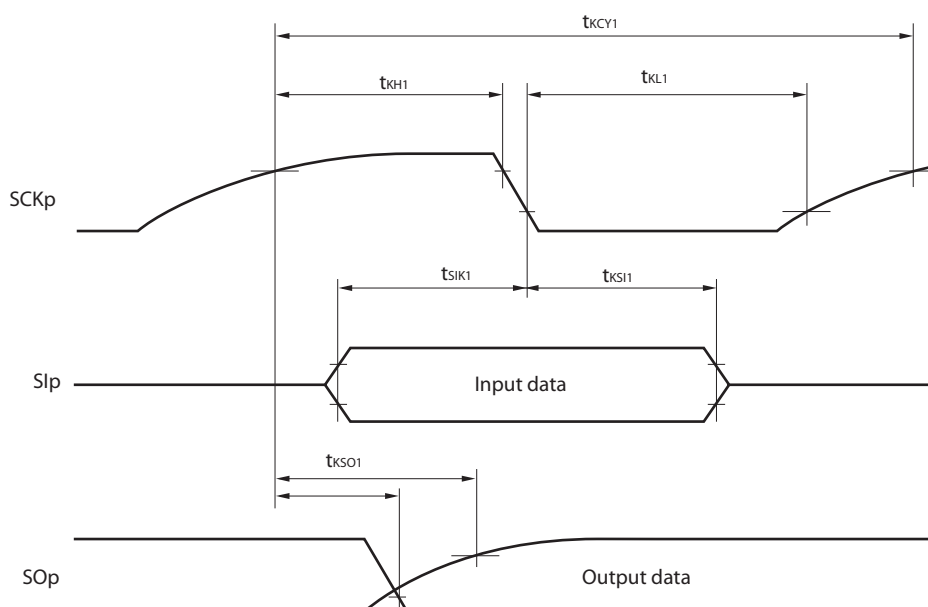
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number (m = 0, 1), n: Channel number (0, 1, 3))

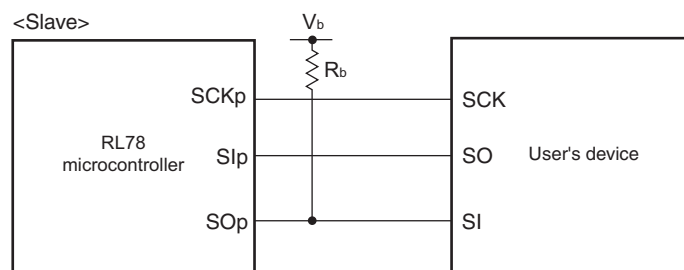
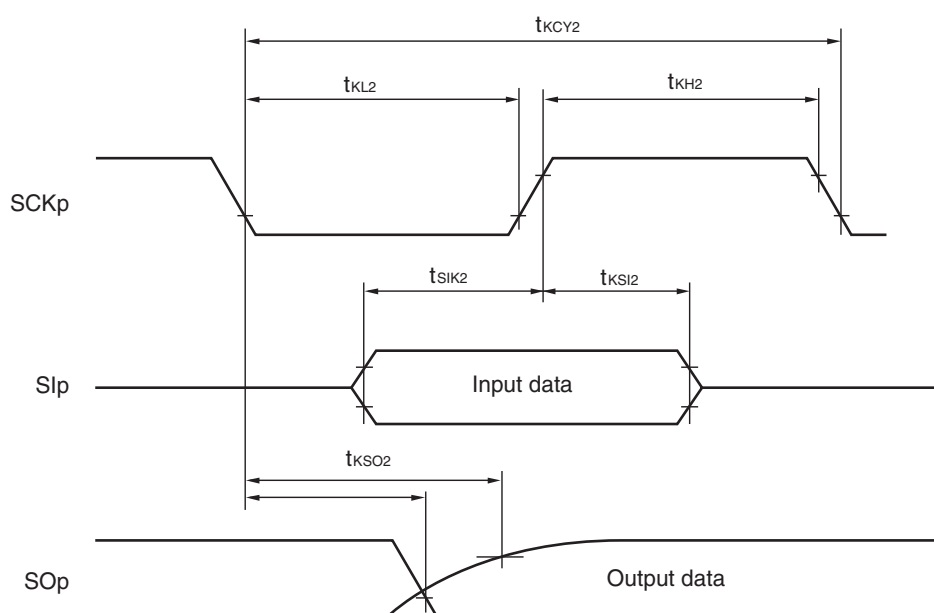
CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

CSI mode connection diagram (during communication at different potential)
CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)


- Remarks**
1. R_b [Ω]: Communication line (SO_p) pull-up resistance, C_b [F]: Communication line (SO_p) load capacitance, V_b [V]: Communication line voltage
 2. p: CSI number ($p = 00, 20$), m: Unit number ($m = 0, 1$), n: Channel number ($n = 0$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn))

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution		1.2	± 7.0	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Conversion time	t _{CONV}	10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution			± 0.60	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution			± 4.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution			± 2.0	LSB
Analog input voltage	V _{AIN}	ANI0 to ANI3, ANI16 to ANI22	0		V_{DD}	V
		Internal reference voltage (HS (high-speed main) mode)	V_{BGR} ^{Note 3}			V
		Temperature sensor output voltage (HS (high-speed main) mode)	V_{TMPS25} ^{Note 3}			V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

3.6.2 Temperature sensor/internal reference voltage characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

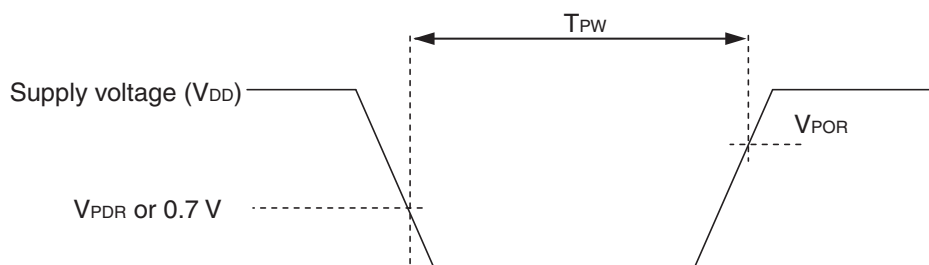
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F_{VTMS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/ $^\circ\text{C}$
Operation stabilization wait time	t_{AMP}		5			μs

3.6.3 POR circuit characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width ^{Note}	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).

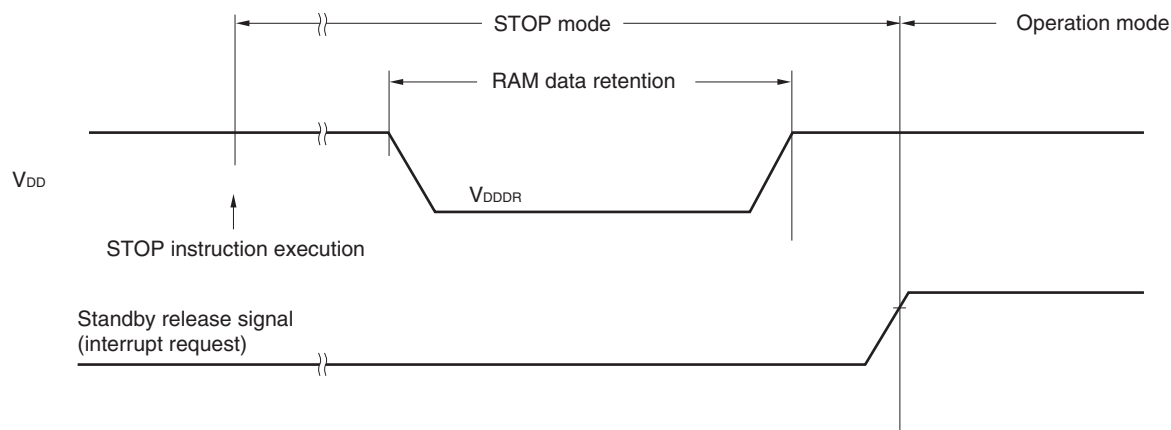


<R> 3.7 RAM Data Retention Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 ^{Note}		5.5	V

<R> Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, 2.4 V $\leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		1		24	MHz
Code flash memory rewritable times <small>Notes 1, 2, 3</small>	C_{erwr}	Retained for 20 years $T_A = 85^\circ\text{C}$ <small>Notes 4</small>	1,000			Times
Data flash memory rewritable times <small>Notes 1, 2, 3</small>		Retained for 1 year $T_A = 25^\circ\text{C}$ <small>Notes 4</small>		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$ <small>Notes 4</small>	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$ <small>Notes 4</small>	10,000			

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library
 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
 4. This temperature is the average value at which data are retained.