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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CSI, I²C, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 30-LSSOP (0.240", 6.10mm Width) |
| Supplier Device Package | 30-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f102a7dsp-v0 |

## 1.3 Differences between the R5F102 Products and the R5F103 Products

The following are differences between the R5F102 products and the R5F103 products.

- Whether the data flash memory is mounted or not
- High-speed on-chip oscillator oscillation frequency accuracy
- Number of channels in serial interface
- Whether the DMA function is mounted or not
- Whether a part of the safety functions are mounted or not

### 1.3.1 Data Flash

The data flash memory of 2 KB is mounted on the R5F102 products, but not on the R5F103 products.

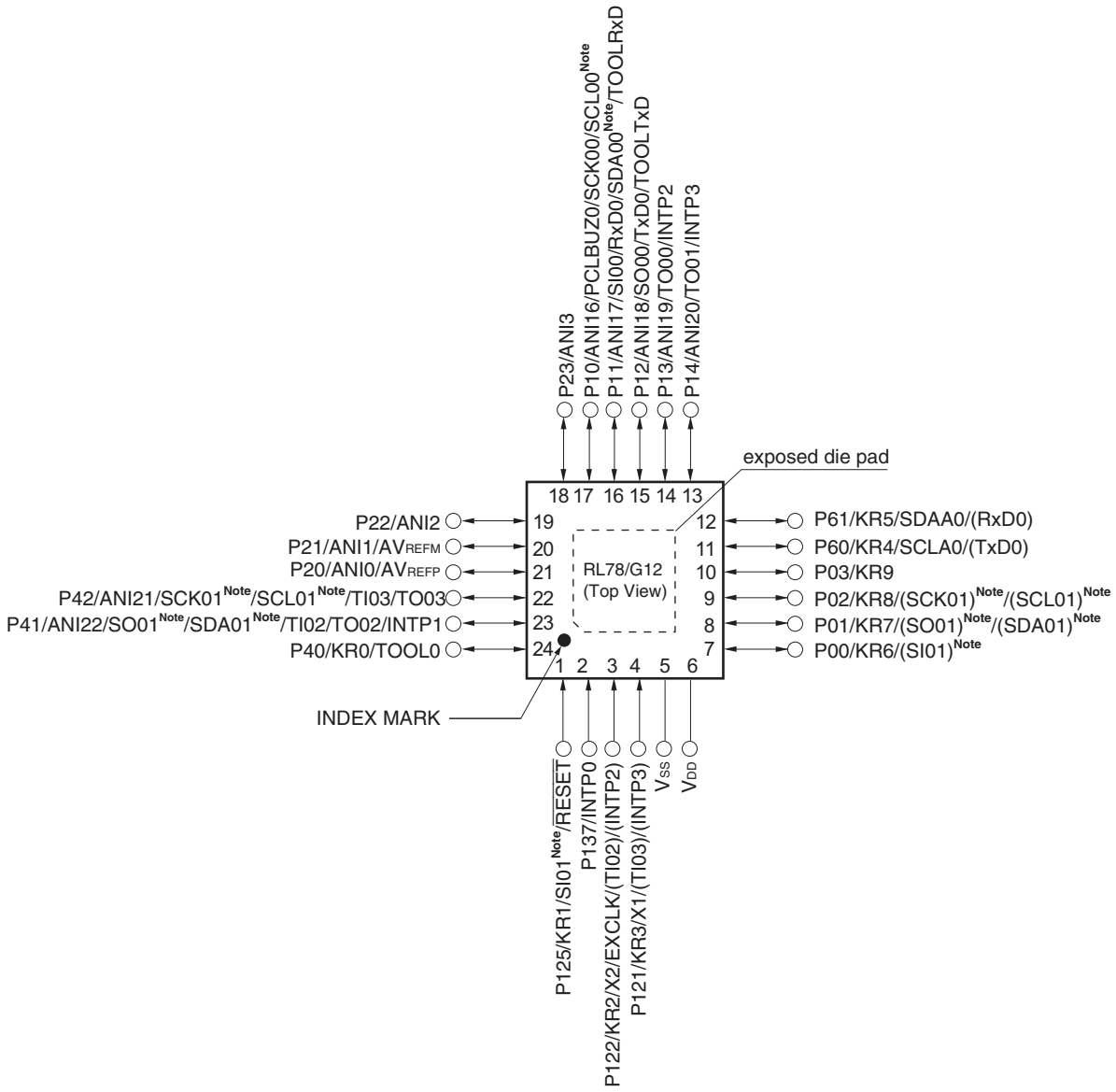
| Product | Data Flash |
|---|---|
| **R5F102 products**<br>R5F1026A, R5F1027A, R5F102AA,<br>R5F10269, R5F10279, R5F102A9,<br>R5F10268, R5F10278, R5F102A8,<br>R5F10267, R5F10277, R5F102A7,<br>R5F10266 Note | 2KB |
| **R5F103 products**<br>R5F1036A, R5F1037A, R5F103AA,<br>R5F10369, R5F10379, R5F103A9,<br>R5F10368, R5F10378 R5F103A8,<br>R5F10367, R5F10377, R5F103A7,<br>R5F10366 | Not mounted |

**Note** The RAM in the R5F10266 has capacity as small as 256 bytes. Depending on the customer's program specification, the stack area to execute the data flash library may not be kept and data may not be written to or erased from the data flash memory.

**Caution** When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

### 1.4.2 24-pin products

<R> • 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)




**Note** Provided only in the R5F102 products.

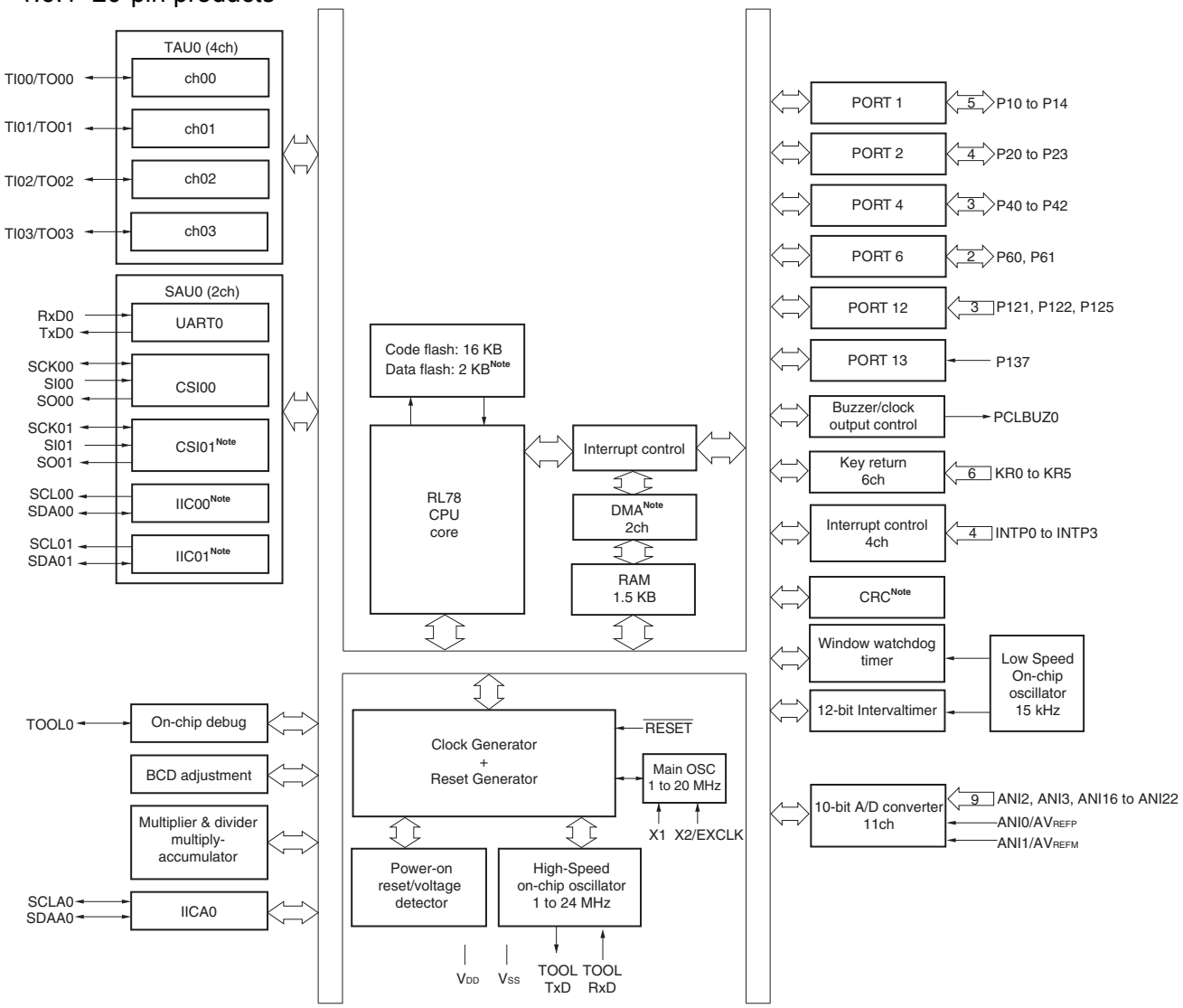
**Remarks 1.** For pin identification, see **1.5 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

**3.** It is recommended to connect an exposed die pad to Vss.

## 1.6 Block Diagram

### 1.6.1 20-pin products




**Note** Provided only in the R5F102 products.

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(1/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high[Note 1] | $I_{OH1}$ | 20-, 24-pin products:<br>Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42<br>30-pin products:<br>Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | | | −10.0 [Note 2] | mA |
| | | 20-, 24-pin products:<br>Total of P40 to P42<br>30-pin products:<br>Total of P00, P01, P40, P120<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | −30.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | −6.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | −4.5 | mA |
| | | 20-, 24-pin products:<br>Total of P00 to P03[Note 4], P10 to P14<br>30-pin products:<br>Total of P10 to P17, P30, P31, P50, P51, P147<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | −80.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | −18.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | −10.0 | mA |
| | | Total of all pins (When duty ≤ 70% [Note 3]) | | | | −100 | mA |
| | $I_{OH2}$ | Per pin for P20 to P23 | | | | −0.1 | mA |
| | | Total of all pins | | | | −0.4 | mA |

**Notes 1.** value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ pin to an output pin.

**2.** However, do not exceed the total current value.

**3.** The output current value under conditions where the duty factor ≤ 70%.
If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = −10.0 mA

Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ −8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**4.** 24-pin products only.

**Caution** P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (2/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low[Note 1] | $I_{OL1}$ | 20-, 24-pin products:<br>Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42<br>30-pin products:<br>Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | | | 20.0 [Note 2] | mA |
| | | Per pin for P60, P61 | | | | 15.0 [Note 2] | mA |
| | | 20-, 24-pin products:<br>Total of P40 to P42<br>30-pin products:<br>Total of P00, P01, P40, P120<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 60.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 9.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 1.8 | mA |
| | | 20-, 24-pin products:<br>Total of P00 to P03[Note 4], P10 to P14, P60, P61<br>30-pin products:<br>Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 80.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 27.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 5.4 | mA |
| | | Total of all pins (When duty ≤ 70% [Note 3]) | | | | 140 | mA |
| | $I_{OL2}$ | Per pin for P20 to P23 | | | | 0.4 | mA |
| | | Total of all pins | | | | 1.6 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $V_{SS}$ pin.

**2.** However, do not exceed the total current value.

**3.** The output current value under conditions where the duty factor ≤ 70%.
If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).
- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**4.** 24-pin products only.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**(1) 20-, 24-pin products**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 6 | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 440 | 1210 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 1210 | |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 400 | 950 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 950 | |
| | | | LS (Low-speed main) mode Note 6 | $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 270 | 542 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 270 | 542 | |
| | | | HS (High-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1000 | μA |
| | | | | | Resonator connection | | 450 | 1170 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1000 | μA |
| | | | | | Resonator connection | | 450 | 1170 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 190 | 590 | μA |
| | | | | | Resonator connection | | 260 | 660 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 190 | 590 | μA |
| | | | | | Resonator connection | | 260 | 660 | |
| | | | LS (Low-speed main) mode Note 6 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 360 | μA |
| | | | | | Resonator connection | | 150 | 416 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 360 | μA |
| | | | | | Resonator connection | | 150 | 416 | |
| | $I_{DD3}$ Note 5 | STOP mode | $T_A$ = –40°C | | | | 0.19 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.32 | 0.80 | |
| | | | $T_A$ = +70°C | | | | 0.48 | 1.20 | |
| | | | $T_A$ = +85°C | | | | 0.74 | 2.20 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS(Low speed main) mode: $V_{DD}$ = 1.8 V to 5.5 V @1 MHz to 8 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except temperature condition of the TYP. value is $T_A$ = 25°C, other than STOP mode

**5.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 4** above to calculate the maximum transfer rate under conditions of the customer.

**6.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ $V_{DD}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**7.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

**8.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**9.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 8** above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). **For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCK00 cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 2/f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 200 | | 1150 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 300 | | 1150 | | ns |
| SCK00 high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2– 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 120 | | $t_{KCY1}$/2 – 120 | | ns |
| SCK00 low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 7 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 10 | | $t_{KCY1}$/2 – 50 | | ns |
| SI00 setup time (to SCK00↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 58 | | 479 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 121 | | 479 | | ns |
| SI00 hold time (from SCK00↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | ns |
| Delay time from SCK00↓ to SO00 output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 60 | | 60 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 130 | | 130 | ns |
| SI00 setup time (to SCK00↓) Note 2 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 23 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 33 | | 110 | | ns |
| SI00 hold time (from SCK00↓) Note 2 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | ns |
| Delay time from SCK00↑ to SO00 output Note 2 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 10 | | 10 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 10 | | 10 | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 300 | | 1150 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 500 | | 1150 | | ns |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 −75 | | $t_{KCY1}$/2−75 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 −170 | | $t_{KCY1}$/2−170 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 −458 | | $t_{KCY1}$/2−458 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 −12 | | $t_{KCY1}$/2−50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 −18 | | $t_{KCY1}$/2−50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 −50 | | $t_{KCY1}$/2−50 | | ns |

**Note** Use it with $V_{DD} \geq V_b$.

**Cautions 1.** Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.

**2.** CSI01 and CSI11 cannot communicate at different potential.

**Remarks 1.** $R_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$ [F]: Communication line (SCKp, SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20)

**(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 12/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 10/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 − 12 | | $t_{KCY2}$/2 − 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 − 18 | | $t_{KCY2}$/2 − 50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | $t_{KCY2}$/2 − 50 | | $t_{KCY2}$/2 − 50 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_{DD}$ ≤ 4.0 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_{DD}$ ≤ 2.0 V Note 2 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 5 | $t_{KSO2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 120 | | 2/$f_{MCK}$ + 573 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

**Notes 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**2.** Use it with $V_{DD} \geq V_b$.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Cautions 1.** Select the TTL input buffer for the SIp and SCKp pins and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**2.** CSI01 and CSI11 cannot communicate at different potential.

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{REFM}$ (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22**

**($T_A$ = −40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (–) = $AV_{REFM}$ Note 4 = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | EZS | 8-bit resolution | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | 0 | | $V_{BGR}$ Note 3 | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

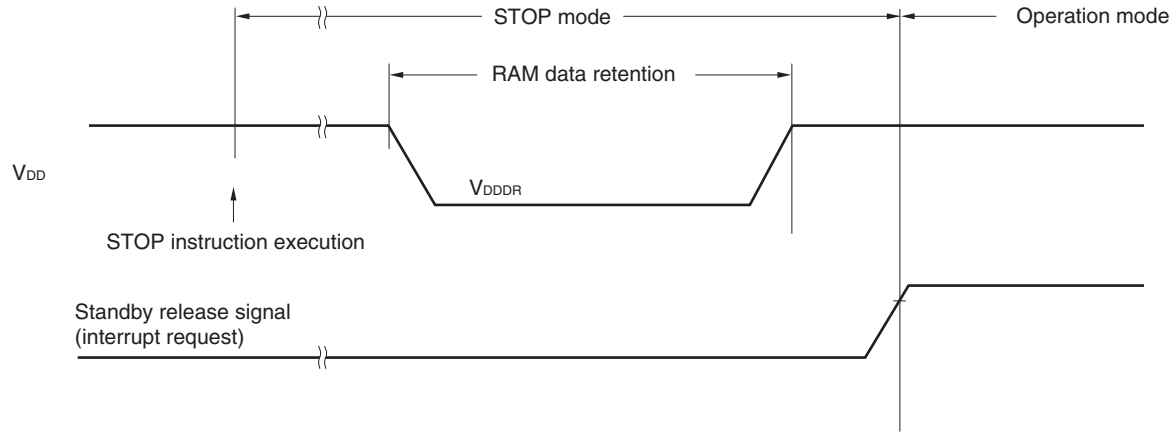
**4.** When reference voltage (–) = $V_{SS}$, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.

## <R> 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

**($T_A$ = −40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.46 Note | | 5.5 | V |

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.




## 2.8 Flash Memory Programming Characteristics

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

<R>

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| System clock frequency | $f_{CLK}$ | | 1 | | 24 | MHz |
| Code flash memory rewritable times Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years $T_A$ = 85°C | 1,000 | | | Times |
| Data flash memory rewritable times Notes 1, 2, 3 | | Retained for 1 year $T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years $T_A$ = 85°C | 100,000 | | | |
| | | Retained for 20 years $T_A$ = 85°C | 10,000 | | | |

**Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**2.** When using flash memory programmer and Renesas Electronics self programming library

**3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 3.3 DC Characteristics

### 3.3.1 Pin characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(1/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high[Note 1] | $I_{OH1}$ | 20-, 24-pin products:<br>Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42<br>30-pin products:<br>Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | | | –3.0 [Note 2] | mA |
| | | 20-, 24-pin products:<br>Total of P40 to P42<br>30-pin products:<br>Total of P00, P01, P40, P120<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | –9.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | –6.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | –4.5 | mA |
| | | 20-, 24-pin products:<br>Total of P00 to P03[Note 4], P10 to P14<br>30-pin products:<br>Total of P10 to P17, P30, P31, P50, P51, P147<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | –27.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | –18.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | –10.0 | mA |
| | | Total of all pins (When duty ≤ 70%[Note 3]) | | | | –36.0 | mA |
| | $I_{OH2}$ | Per pin for P20 to P23 | | | | –0.1 | mA |
| | | Total of all pins | | | | –0.4 | mA |

**Notes 1.** value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ pin to an output pin.

**2.** However, do not exceed the total current value.

**3.** The output current value under conditions where the duty factor ≤ 70%.
If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = –10.0 mA
Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**4.** 24-pin products only.

**Caution** P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 3.3.2 Supply current characteristics

**(1) 20-, 24-pin products**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD1}$ | Operating mode | HS (High-speed main) mode[Note 4] | $f_{IH}$ = 24 MHz[Note 3] | Basic operation | $V_{DD}$ = 5.0 V | | 1.5 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.5 | | |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.3 | 5.3 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.3 | 5.3 | |
| | | | | $f_{IH}$ = 16 MHz[Note 3] | | $V_{DD}$ = 5.0 V | | 2.5 | 3.9 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.5 | 3.9 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 2.8 | 4.7 | mA |
| | | | | | | Resonator connection | | 3.0 | 4.8 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 2.8 | 4.7 | mA |
| | | | | | | Resonator connection | | 3.0 | 4.8 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 1.8 | 2.8 | mA |
| | | | | | | Resonator connection | | 1.8 | 2.8 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 1.8 | 2.8 | mA |
| | | | | | | Resonator connection | | 1.8 | 2.8 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator clock is stopped.

**3.** When high-speed system clock is stopped

**4.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

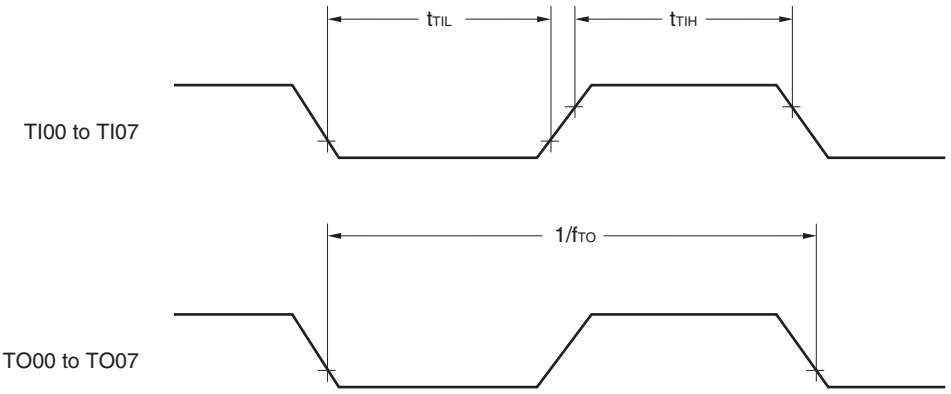
HS(High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

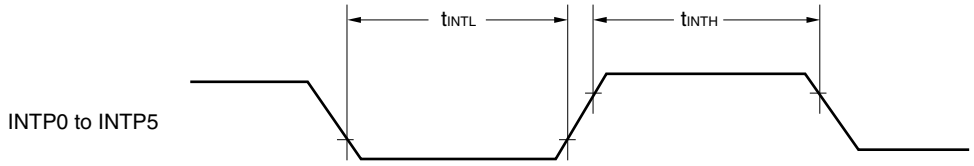
**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Temperature condition of the TYP. value is $T_A$ = 25°C.

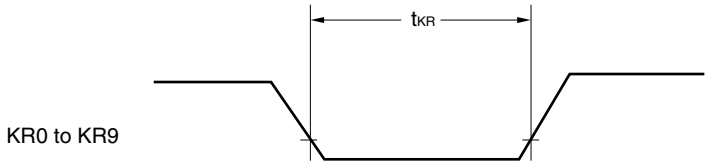
**TI/TO Timing**



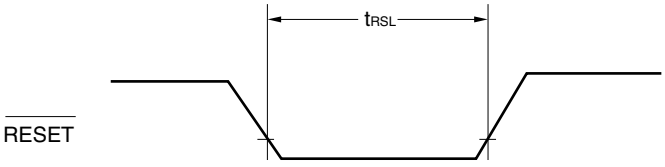

**Interrupt Request Input Timing**




**Key Interrupt Input Timing**




**$\overline{\text{RESET}}$ Input Timing**



### (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note4 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 12/$f_{MCK}$ and 1000 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–14 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–16 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–36 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note4 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 66 | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 113 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

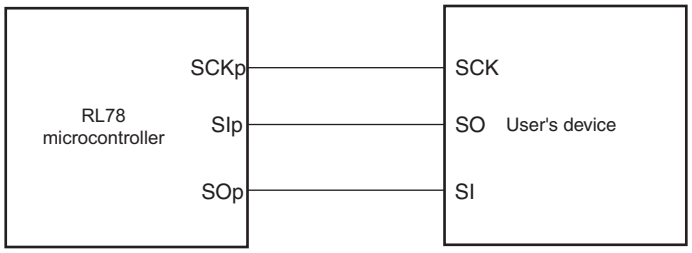
**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SOp output lines.

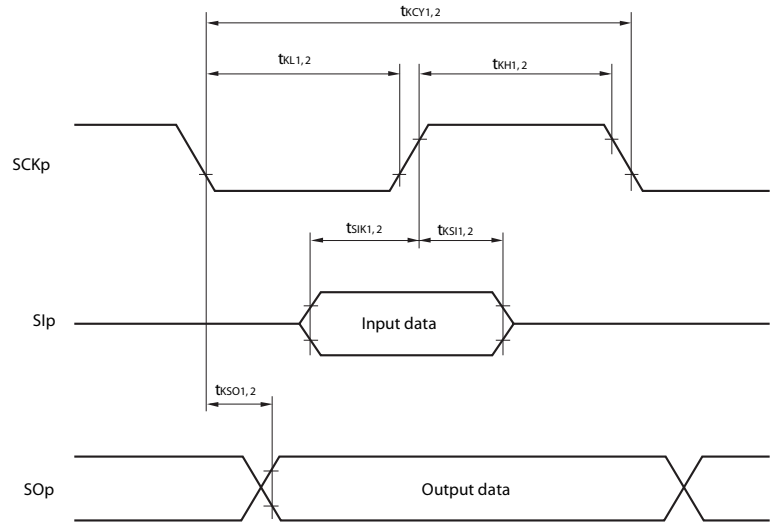
**5.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Caution** Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

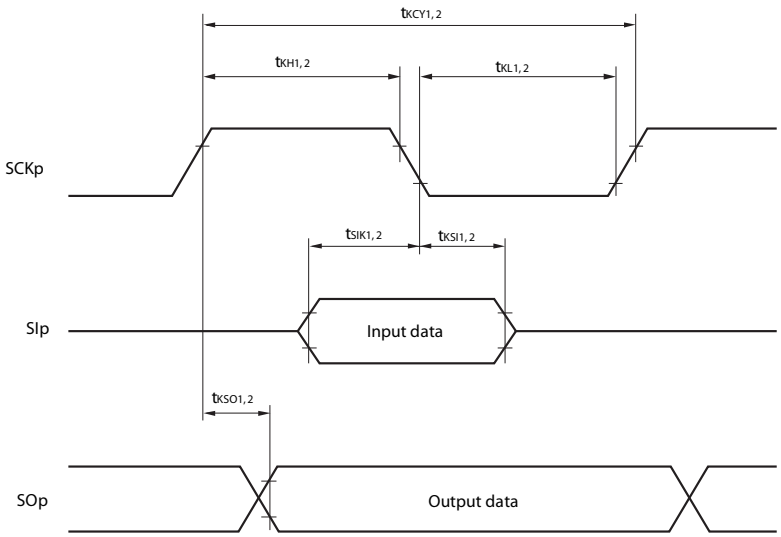
**CSI mode connection diagram (during communication at same potential)**



**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0,1), n: Channel number (n = 0, 1, 3))

### (4) During communication at same potential (simplified I²C mode)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

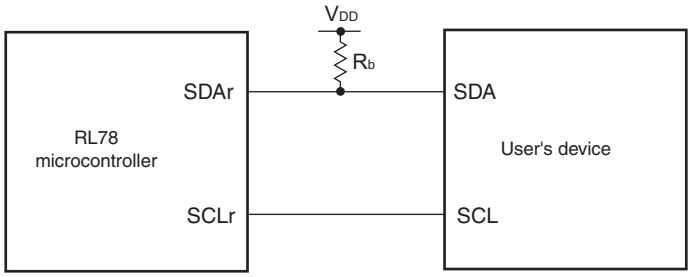
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 580 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 1420 | ns |

**Notes 1.** The value must also be equal to or less than $f_{MCK}$/4.

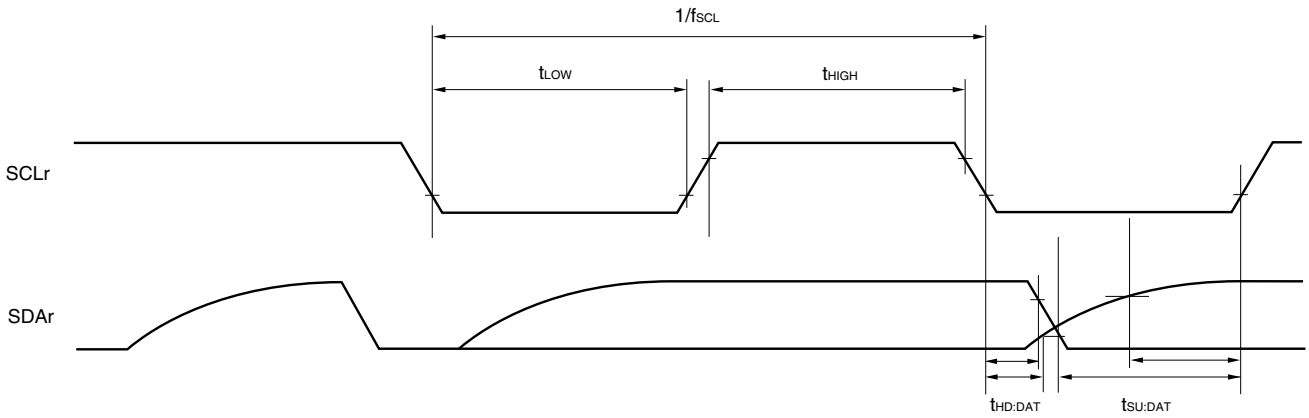
**2.** Set $t_{SU:DAT}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

**Caution** Select the N-ch open drain output ($V_{DD}$ tolerance) mode for SDAr by using port output mode register h (POMh).

**Simplified I²C mode connection diagram (during communication at same potential)**




**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remarks 1.** $R_b$ [Ω]:Communication line (SDAr) pull-up resistance

$C_b$ [F]: Communication line (SCLr, SDAr) load capacitance

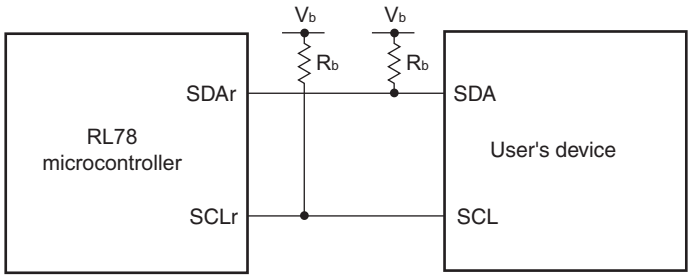
**2.** r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1, 4, 5)

**3.** $f_{MCK}$: Serial array unit operation clock frequency

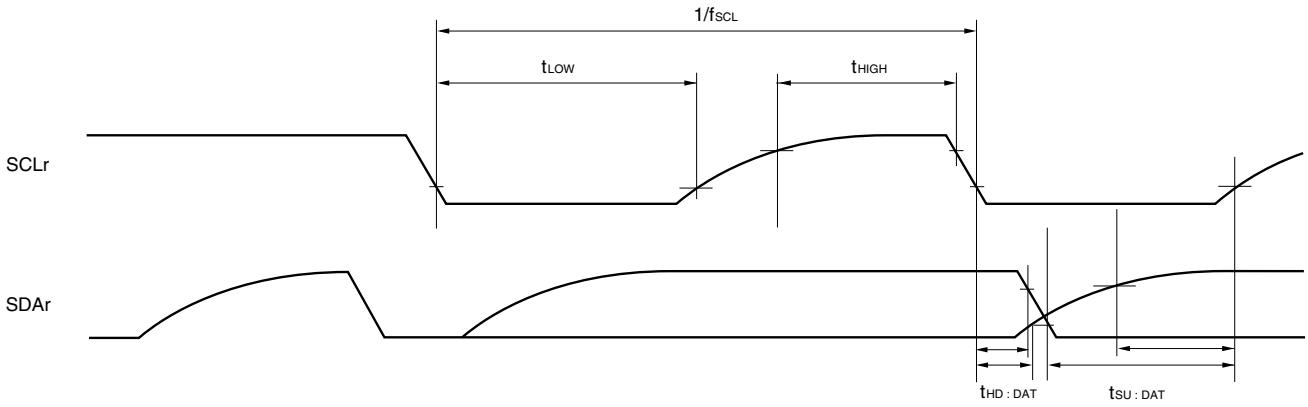
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number (m = 0, 1), n: Channel number (0, 1, 3))

**Simplified $I^2C$ mode connection diagram (during communication at different potential)**




**Simplified $I^2C$ mode serial transfer timing (during communication at different potential)**




**Remarks 1.** $R_b$ [Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$ [F]: Communication line (SDAr, SCLr) load capacitance, $V_b$ [V]: Communication line voltage

**2.** r: IIC Number (r = 00, 20)

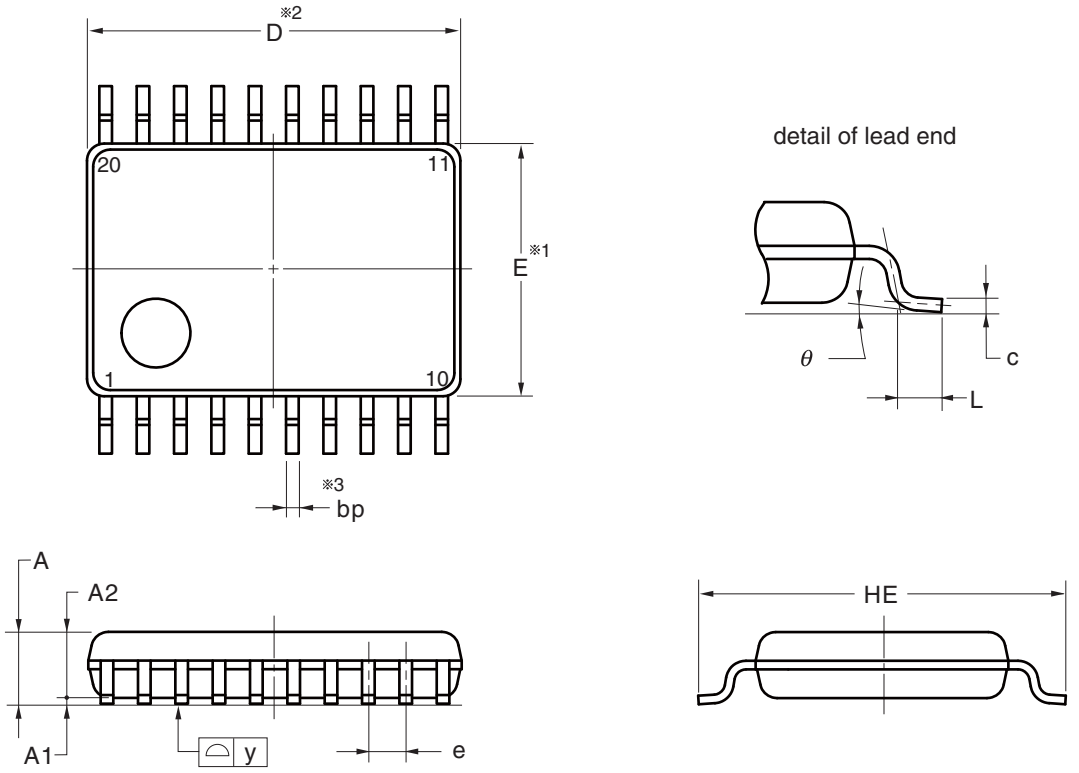
**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0,1), n: Channel number (n = 0))

# 4. PACKAGE DRAWINGS

## 4.1 20-pin products

R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP
R5F1036AASP, R5F10369ASP, R5F10368ASP, R5F10367ASP, R5F10366ASP
R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP
R5F1036ADSP, R5F10369DSP, R5F10368DSP, R5F10367DSP, R5F10366DSP
<R> R5F1026AGSP, R5F10269GSP, R5F10268GSP, R5F10267GSP, R5F10266GSP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LSSOP20-4.4x6.5-0.65 | PLSP0020JB-A | P20MA-65-NAA-1 | 0.1 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 6.50±0.10 |
| E | 4.40±0.10 |
| HE | 6.40±0.20 |
| A | 1.45 MAX. |
| A1 | 0.10±0.10 |
| A2 | 1.15 |
| e | 0.65±0.12 |
| bp | $0.22^{+0.10}_{-0.05}$ |
| c | $0.15^{+0.05}_{-0.02}$ |
| L | 0.50±0.20 |
| y | 0.10 |
| θ | 0° to 10° |

**NOTE**

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.