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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f102a8asp-x0

1.7 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		20-pin		24-pin		30-pin	
		R5F1026x	R5F1036x	R5F1027x	R5F1037x	R5F102Ax	R5F103Ax
Code flash memory		2 to 16 KB Note 1		4 to 16 KB			
Data flash memory		2 KB	–	2 KB	–	2 KB	–
RAM		256 B to 1.5 KB		512 B to 1.5 KB		512 B to 2KB	
Address space		1 MB					
<R> Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode : 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode : 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode : 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V)					
	High-speed on-chip oscillator clock	HS (High-speed main) mode : 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode : 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode : 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V)					
Low-speed on-chip oscillator clock		15 kHz (TYP)					
General-purpose register		(8-bit register × 8) × 4 banks					
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f_{IH} = 24 MHz operation)					
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)					
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.					
I/O port	Total	18		22		26	
	CMOS I/O	12 (N-ch O.D. I/O [V_{DD} withstand voltage]: 4)		16 (N-ch O.D. I/O [V_{DD} withstand voltage]: 5)		21 (N-ch O.D. I/O [V_{DD} withstand voltage]: 9)	
	CMOS input	4		4		3	
	N-ch open-drain I/O (6 V tolerance)	2					
Timer	16-bit timer	4 channels				8 channels	
	Watchdog timer	1 channel					
	12-bit Interval timer	1 channel					
	Timer output	4 channels (PWM outputs: 3 Note 3)				8 channels (PWM outputs: 7 Note 3) Note 2	

Notes 1. The self-programming function cannot be used in the R5F10266 and R5F10366.

2. The maximum number of channels when PIOR0 is set to 1.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). (See **6.9.3 Operation as multiple PWM output function**.)

Caution When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

2.2 Oscillator Characteristics

2.2.1 X1 oscillator characteristics

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)[Note]	Ceramic resonator / crystal oscillator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V	1.0		8.0	

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **5.4 System Clock Oscillator**.

2.2.2 On-chip oscillator characteristics

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency [Notes 1, 2]	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		R5F102 products	T_A = −20 to +85°C	-1.0		+1.0	%
			T_A = −40 to −20°C	-1.5		+1.5	%
		R5F103 products		-5.0		+5.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2.3.2 Supply current characteristics

(1) 20-, 24-pin products

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS(High-speed main) mode[Note 4]	f_{IH} = 24 MHz[Note 3]	Basic operation	V_{DD} = 5.0 V		1.5		mA
						V_{DD} = 3.0 V		1.5		
					Normal operation	V_{DD} = 5.0 V		3.3	5.0	mA
						V_{DD} = 3.0 V		3.3	5.0	
				f_{IH} = 16 MHz[Note 3]		V_{DD} = 5.0 V		2.5	3.7	mA
						V_{DD} = 3.0 V		2.5	3.7	
			LS(Low-speed main) mode[Note 4]	f_{IH} = 8 MHz[Note 3]		V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	
			HS(High-speed main) mode[Note4]	f_{MX} = 20 MHz[Note 2], V_{DD} = 5.0 V		Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	
				f_{MX} = 20 MHz[Note 2], V_{DD} = 3.0 V		Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 5.0 V		Square wave input		1.8	2.6	mA
						Resonator connection		1.8	2.6	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 3.0 V		Square wave input		1.8	2.6	mA
						Resonator connection		1.8	2.6	
			LS(Low-speed main) mode[Note 4]	f_{MX} = 8 MHz[Note 2], V_{DD} = 3.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f_{MX} = 8 MHz[Note 2], V_{DD} = 2.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.

3. When high-speed system clock is stopped

4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS(Low speed main) mode: V_{DD} = 1.8 V to 5.5 V @1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C.

(3) Peripheral functions (Common to all products)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed onchip oscillator operating current	I_{FIL} Note 1				0.20		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 2, 3				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 4	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 5	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.30	1.70	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.50	0.70	mA
A/D converter reference voltage operating current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVD} Notes 1, 6				0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 8				2.00	12.20	mA
BGO operating current	I_{BGO} Notes 1, 7				2.00	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 9		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to the V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{FIL} and I_{TMKA} when the 12-bit interval timer operates.

4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

6. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.

7. Current flowing only during data flash rewrite.

8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. Temperature condition of the TYP. value is T_A = 25°C

2.4 AC Characteristics

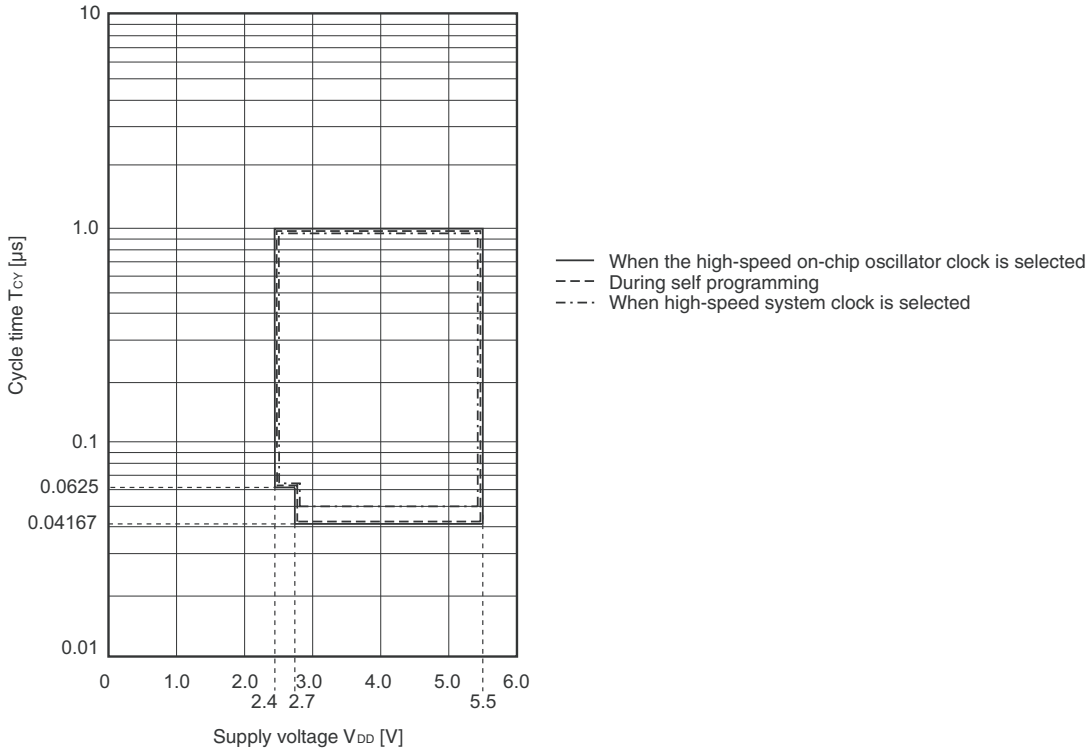
(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (High-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
		During self programming	HS (High-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V_{DD} < 2.4 V			1.0		8.0	MHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
		1.8 V ≤ V_{DD} < 2.4 V			60			ns
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK} + 10			ns
TO00 to TO07 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V					12	MHz
		2.7 V ≤ V_{DD} < 4.0 V					8	MHz
		1.8 V ≤ V_{DD} < 2.7 V					4	MHz
PCLBUZ0, or PCLBUZ1 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V					16	MHz
		2.7 V ≤ V_{DD} < 4.0 V					8	MHz
		1.8 V ≤ V_{DD} < 2.7 V					4	MHz
INTP0 to INTP5 input high-level width, low-level width	t_{INTH}, t_{INTL}				1			μs
KR0 to KR9 input available width	t_{KR}				250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

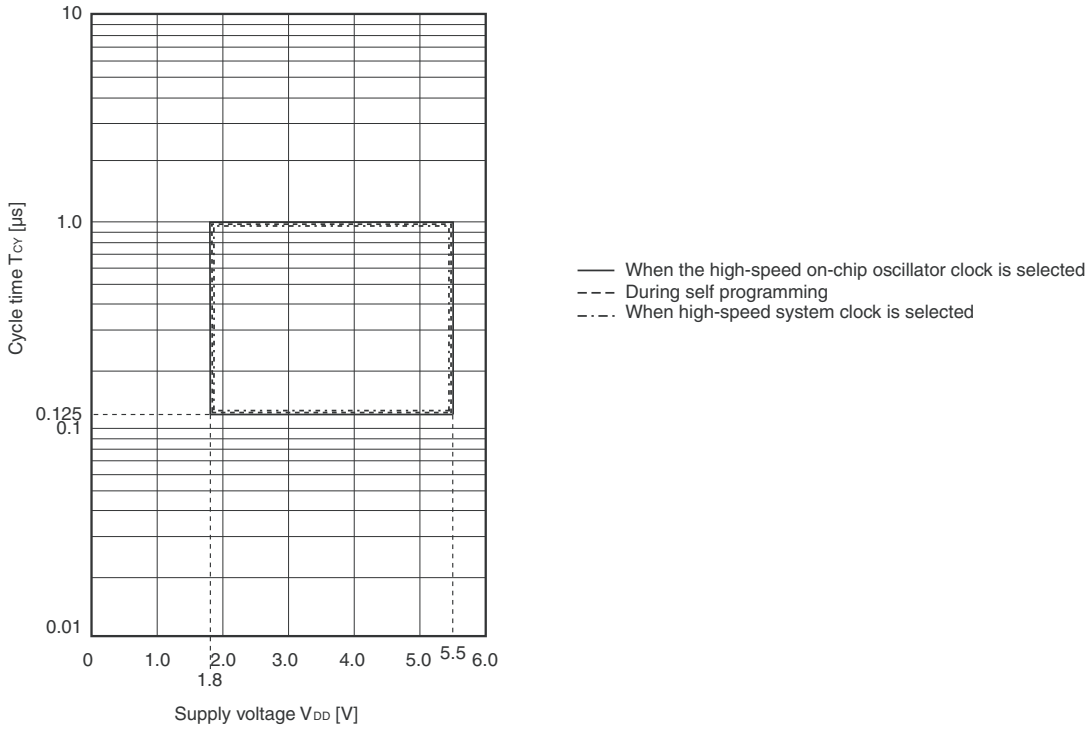
Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation

T_{CY} vs V_{DD} (HS (high-speed main) mode)



T_{CY} vs V_{DD} (LS (low-speed main) mode)



Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products.)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products.))

(5) During communication at same potential (simplified I^2C mode)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode LS (low-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1	kHz
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		ns
Hold time when SCLr = “H”	t_{HIGH}	1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		ns
Data setup time (reception)	$t_{SU:DAT}$	1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 145 Note 2		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	$1/f_{MCK}$ + 230 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	1.8 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

2. Set $t_{SU:DAT}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

Caution Select the N-ch open drain output (V_{DD} tolerance) mode for SDAr by using port output mode register h (POMh).

(**Remarks** are listed on the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}		–		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 − 12		t_{KCY2}/2 − 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 − 18		t_{KCY2}/2 − 50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 − 50		t_{KCY2}/2 − 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_{DD} ≤ 4.0 V		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_{DD} ≤ 2.0 V Note 2		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}			1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 120		2/f_{MCK} + 573	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 214		2/f_{MCK} + 573	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 573		2/f_{MCK} + 573	ns

Notes 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

2. Use it with $V_{DD} \geq V_b$.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

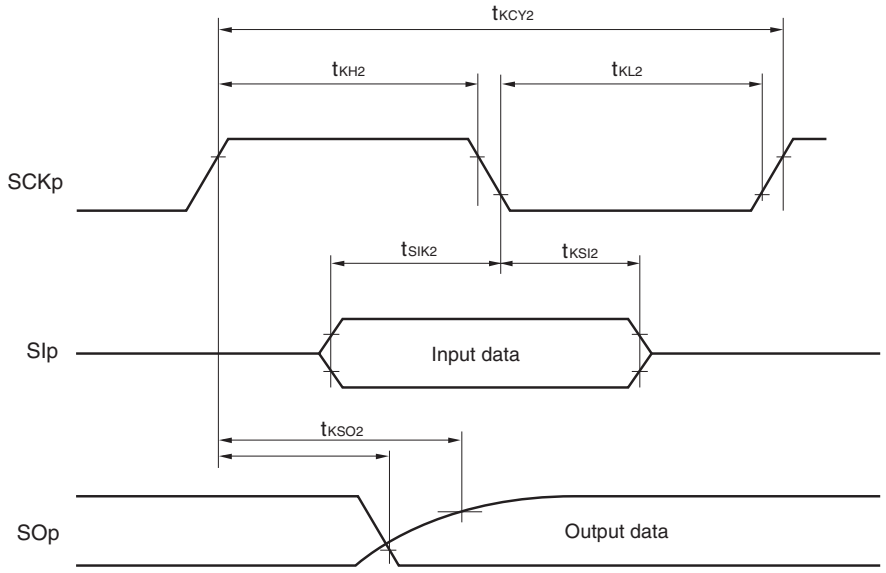
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Cautions 1. Select the TTL input buffer for the SIp and SCKp pins and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

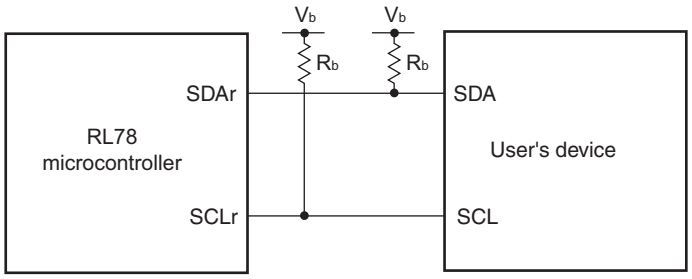
2. CSI01 and CSI11 cannot communicate at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

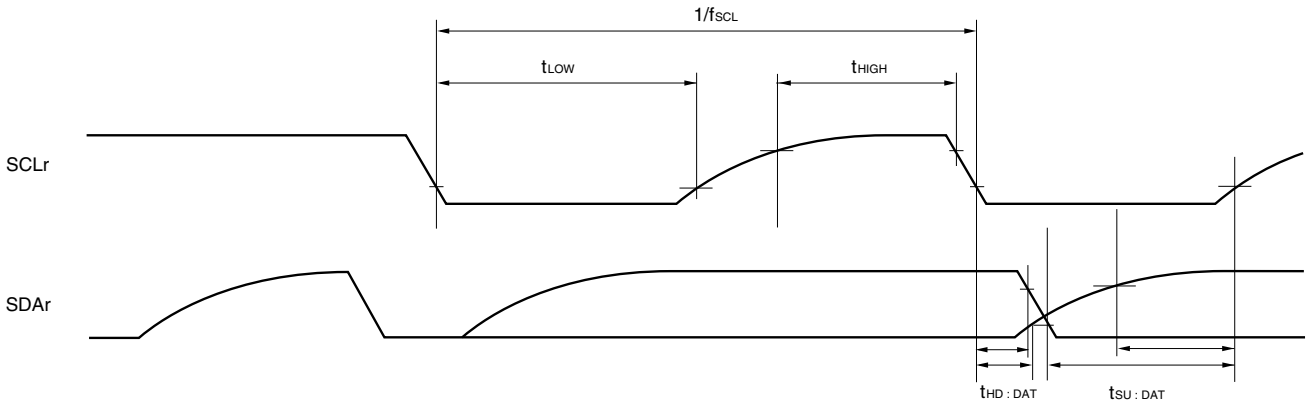


Remark p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

Simplified I^2C mode connection diagram (during communication at different potential)



Simplified I^2C mode serial transfer timing (during communication at different potential)



Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b [V]: Communication line voltage

2. r: IIC Number (r = 00, 20)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0,1), n: Channel number (n = 0))

4. Simplified I^2C mode is supported only by the R5F102 products.

LVD detection voltage of interrupt & reset mode

(T_A = −40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V_{LVDB1}	LVIS1, LVIS0 = 1, 0	Rising reset release voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}	LVIS1, LVIS0 = 0, 1	Rising reset release voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}	LVIS1, LVIS0 = 0, 0	Rising reset release voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V_{LVDC1}	LVIS1, LVIS0 = 1, 0	Rising reset release voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}	LVIS1, LVIS0 = 0, 1	Rising reset release voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDC3}	LVIS1, LVIS0 = 0, 0	Rising reset release voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC1} = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V_{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising reset release voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising reset release voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising reset release voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

2.6.5 Power supply voltage rising slope characteristics

(T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 28.4 AC Characteristics.

3.2 Oscillator Characteristics

3.2.1 X1 oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator / crystal oscillator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		8.0	

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **5.4 System Clock Oscillator**.

3.2.2 On-chip oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		R5F102 products	T_A = –20 to +85°C	-1.0		+1.0	%
			T_A = –40 to –20°C	-1.5		+1.5	%
			T_A = +85 to +105°C	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(4/4)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL1}	20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P23	I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.4	V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 2.0 mA			0.4	V
Input leakage current, high	I_{LIH1}	Other than P121, P122	V_I = V_{DD}			1	μA
	I_{LIH2}	P121, P122 (X1, X2/EXCLK)	V_I = V_{DD} Input port or external clock input			1	μA
			V_I = V_{DD} When resonator connected			10	μA
Input leakage current, low	I_{LIL1}	Other than P121, P122	V_I = V_{SS}			–1	μA
	I_{LIL2}	P121, P122 (X1, X2/EXCLK)	V_I = V_{SS} Input port or external clock input			–1	μA
			V_I = V_{SS} When resonator connected			–10	μA
On-chip pull-up resistance	R_U	20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42, P125, $\overline{\text{RESET}}$ 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	V_I = V_{SS}, input port	10	20	100	kΩ

Note 24-pin products only.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) 30-pin products

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS (High-speed main) mode[Note 4]	f_{IH} = 24 MHz[Note 3]	Basic operation	V_{DD} = 5.0 V		1.5		mA
						V_{DD} = 3.0 V		1.5		
					Normal operation	V_{DD} = 5.0 V		3.7	5.8	mA
						V_{DD} = 3.0 V		3.7	5.8	
				f_{IH} = 16 MHz[Note 3]		V_{DD} = 5.0 V		2.7	4.2	mA
						V_{DD} = 3.0 V		2.7	4.2	
				f_{MX} = 20 MHz[Note 2], V_{DD} = 5.0 V		Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	
				f_{MX} = 20 MHz[Note 2], V_{DD} = 3.0 V		Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 5.0 V		Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 3.0 V		Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.

3. When high-speed system clock is stopped

4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C.

(3) Peripheral functions (Common to all products)

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed onchip oscillator operating current	I_{FIL} Note 1				0.20		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 2, 3				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 4	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 5	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.30	1.70	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.50	0.70	mA
A/D converter reference voltage operating current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVD} Notes 1, 6				0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 8				2.00	12.20	mA
BGO operating current	I_{BGO} Notes 1, 7				2.00	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 9		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	2.04	mA
		CSI/UART operation			0.70	1.54	mA

Notes 1. Current flowing to the V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{FIL} and I_{TMKA} when the 12-bit interval timer operates.

4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

6. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.

7. Current flowing only during data flash rewrite.

8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. Temperature condition of the TYP. value is T_A = 25°C

3.4 AC Characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (High-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
		During self programming	HS (High-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	MHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK} + 10			ns
TO00 to TO07 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V					12	MHz
		2.7 V ≤ V_{DD} < 4.0 V					8	MHz
		2.4 V ≤ V_{DD} < 2.7 V					4	MHz
PCLBUZ0, or PCLBUZ1 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V					16	MHz
		2.7 V ≤ V_{DD} < 4.0 V					8	MHz
		2.4 V ≤ V_{DD} < 2.7 V					4	MHz
INTP0 to INTP5 input high-level width, low-level width	t_{INTH}, t_{INTL}				1			μs
KR0 to KR9 input available width	t_{KR}				250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate Note4		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps
		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		**Note 3**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.0 Note 4	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V,		**Note 5**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 6	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		**Notes 2, 7**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 8	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

3. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)

(T_A = −40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) Note	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	162		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	354		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	958		ns
SIp hold time (from SCKp↑) Note	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output Note	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		200	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		390	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		966	ns

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

(**Cautions** and **Remarks** are listed on the next page.)

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (–) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (–) = AV_{REFM}
ANI0 to ANI3	Refer to **29.6.1 (1)**.	Refer to **29.6.1 (3)**.	Refer to **29.6.1 (4)**.
ANI16 to ANI22	Refer to **29.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **29.6.1 (1)**.		–

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD} [Note 3]			1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2, ANI3	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±0.25	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±0.25	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±2.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±1.5	LSB
Analog input voltage	V_{AIN}	ANI2, ANI3		0		AV_{REFP}	V
		Internal reference voltage (HS (high-speed main) mode)		V_{BGR} [Note 4]			V
		Temperature sensor output voltage (HS (high-speed main) mode)		V_{TMPS25} [Note 4]			V

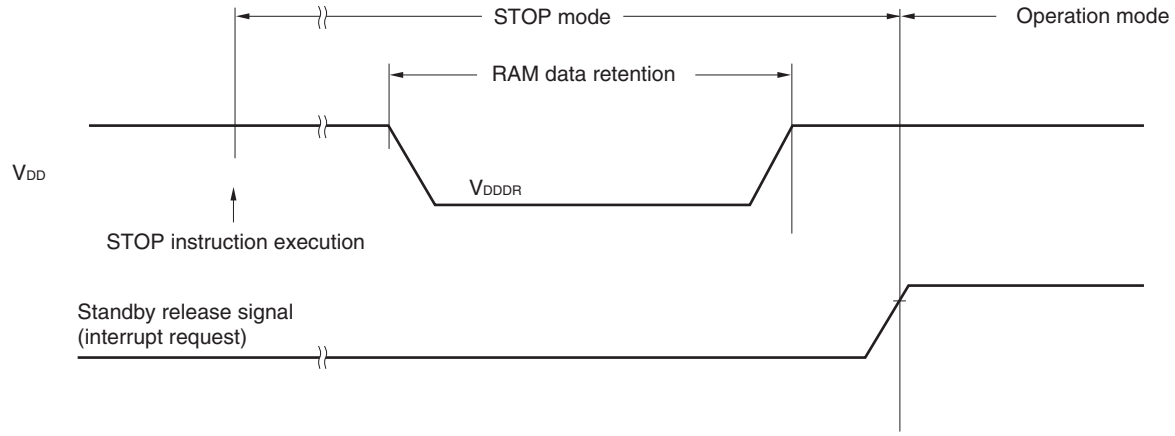
(**Notes** are listed on the next page.)

<R> 3.7 RAM Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

<R> Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.8 Flash Memory Programming Characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
<R> System clock frequency	f_{CLK}		1		24	MHz
Code flash memory rewritable times Notes 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85°C Notes 4	1,000			Times
Data flash memory rewritable times Notes 1, 2, 3		Retained for 1 year T_A = 25°C Notes 4		1,000,000		
		Retained for 5 years T_A = 85°C Notes 4	100,000			
		Retained for 20 years T_A = 85°C Notes 4	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4. This temperature is the average value at which data are retained.