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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I <sup>2</sup> C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f102aaasp-x0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f102aaasp-x0</a>

## ○ ROM, RAM capacities

Code flash	Data flash	RAM	20 pins	24 pins	30 pins
16 KB	2 KB	2 KB	—	—	R5F102AA
	—		—	—	R5F103AA
	2 KB	1.5 KB	R5F1026A <sup>Note 1</sup>	R5F1027A <sup>Note 1</sup>	—
	—		R5F1036A <sup>Note 1</sup>	R5F1037A <sup>Note 1</sup>	—
12 KB	2KB	1 KB	R5F10269 <sup>Note 1</sup>	R5F10279 <sup>Note 1</sup>	R5F102A9
	—		R5F10369 <sup>Note 1</sup>	R5F10379 <sup>Note 1</sup>	R5F103A9
8 KB	2 KB	768 B	R5F10268 <sup>Note 1</sup>	R5F10278 <sup>Note 1</sup>	R5F102A8
	—		R5F10368 <sup>Note 1</sup>	R5F10378 <sup>Note 1</sup>	R5F103A8
4 KB	2KB	512 B	R5F10267	R5F10277	R5F102A7
	—		R5F10367	R5F10377	R5F103A7
2 KB	2 KB	256 B	R5F10266 <sup>Note 2</sup>	—	—
	—		R5F10366 <sup>Note 2</sup>	—	—

**Notes** 1. This is 640 bytes when the self-programming function or data flash function is used. (For details, see **CHAPTER 3 CPU ARCHITECTURE**.)

2. The self-programming function cannot be used for R5F10266 and R5F10366.

**Caution** When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

### 1.3.2 On-chip oscillator characteristics

(1) High-speed on-chip oscillator oscillation frequency of the R5F102 products

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	$T_A = -20$ to $+85$ °C	-1.0	+1.0	%
	$T_A = -40$ to $-20$ °C	-1.5	+1.5	
	$T_A = +85$ to $+105$ °C	-2.0	+2.0	

(2) High-speed on-chip oscillator oscillation frequency of the R5F103 products

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	$T_A = -40$ to $+85$ °C	-5.0	+5.0	%

### 1.3.3 Peripheral Functions

The following are differences in peripheral functions between the R5F102 products and the R5F103 products.

RL78/G12		R5F102 product		R5F103 product	
		20, 24 pin product	30 pin product	20, 24 pin product	30 pin product
Serial interface	UART	1 channel	3 channels	1 channel	
	CSI	2 channels	3 channels	1 channel	
	Simplified I <sup>2</sup> C	2 channels	3 channels	None	
DMA function		2 channels		None	
Safety function	CRC operation	Yes		None	
	RAM guard	Yes		None	
	SFR guard	Yes		None	

## <R> 2. ELECTRICAL SPECIFICATIONS ( $T_A = -40$ to $+85^\circ\text{C}$ )

<R> This chapter describes the following electrical specifications.

Target products A: Consumer applications  $T_A = -40$  to  $+85^\circ\text{C}$

<R> R5F102xxAxx, R5F103xxAxx

D: Industrial applications  $T_A = -40$  to  $+85^\circ\text{C}$

<R> R5F102xxDxx, R5F103xxDxx

G: Industrial applications when  $T_A = -40$  to  $+105^\circ\text{C}$  products is used in the range of  $T_A = -40$  to  $+85^\circ\text{C}$

<R> R5F102xxGxx

**Cautions** 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product.

**( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )****(2/4)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low <sup>Note 1</sup>	I <sub>OL1</sub>	20-, 24-pin products: Per pin for P00 to P03 <sup>Note 4</sup> , P10 to P14, P40 to P42  30-pin products: Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147			20.0 <sup>Note 2</sup>	mA
		Per pin for P60, P61			15.0 <sup>Note 2</sup>	mA
		20-, 24-pin products: Total of P40 to P42  30-pin products: Total of P00, P01, P40, P120 (When duty $\leq 70\%$ <sup>Note 3</sup> )	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		60.0	mA
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		9.0	mA
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		1.8	mA
		20-, 24-pin products: Total of P00 to P03 <sup>Note 4</sup> , P10 to P14, P60, P61  30-pin products: Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147 (When duty $\leq 70\%$ <sup>Note 3</sup> )	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		80.0	mA
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		27.0	mA
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		5.4	mA
		Total of all pins (When duty $\leq 70\%$ <sup>Note 3</sup> )			140	mA
	I <sub>OL2</sub>	Per pin for P20 to P23			0.4	mA
		Total of all pins			1.6	mA

**Notes** 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the  $V_{SS}$  pin.

2. However, do not exceed the total current value.

3. The output current value under conditions where the duty factor  $\leq 70\%$ .

If duty factor  $> 70\%$ : The output current value can be calculated with the following expression (where  $n$  represents the duty factor as a percentage).

- Total output current of pins =  $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where  $n = 80\%$  and  $I_{OL} = 10.0\text{ mA}$

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. 24-pin products only.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	167		500		ns
			2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V	250		500		ns
			1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V	–		500		ns
SCKp high-/low-level width	t <sub>KH1</sub> , t <sub>KL1</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2–12		t <sub>KCY1</sub> /2–50		ns
		2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2–18		t <sub>KCY1</sub> /2–50		ns
		2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2–38		t <sub>KCY1</sub> /2–50		ns
		1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V		–		t <sub>KCY1</sub> /2–50		ns
Slp setup time (to SCKp↑) <small>Note 1</small>	t <sub>SIK1</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V		44		110		ns
		2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V		44		110		ns
		2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V		75		110		ns
		1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V		–		110		ns
Slp hold time (from SCKp↑) <small>Note 2</small>	t <sub>SH1</sub>			19		19		ns
Delay time from SCKp↓ to SOp output <small>Note 3</small>	t <sub>KSO1</sub>	C = 30 pF <small>Note 4</small>			25		25	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  4. C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

- Remarks**
1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products)
  2. f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products.))

5. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 4** above to calculate the maximum transfer rate under conditions of the customer.

6. The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when  $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$  and  $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

8. The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when  $1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$ ,  $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

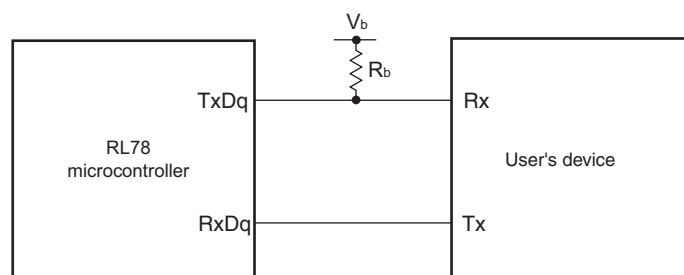
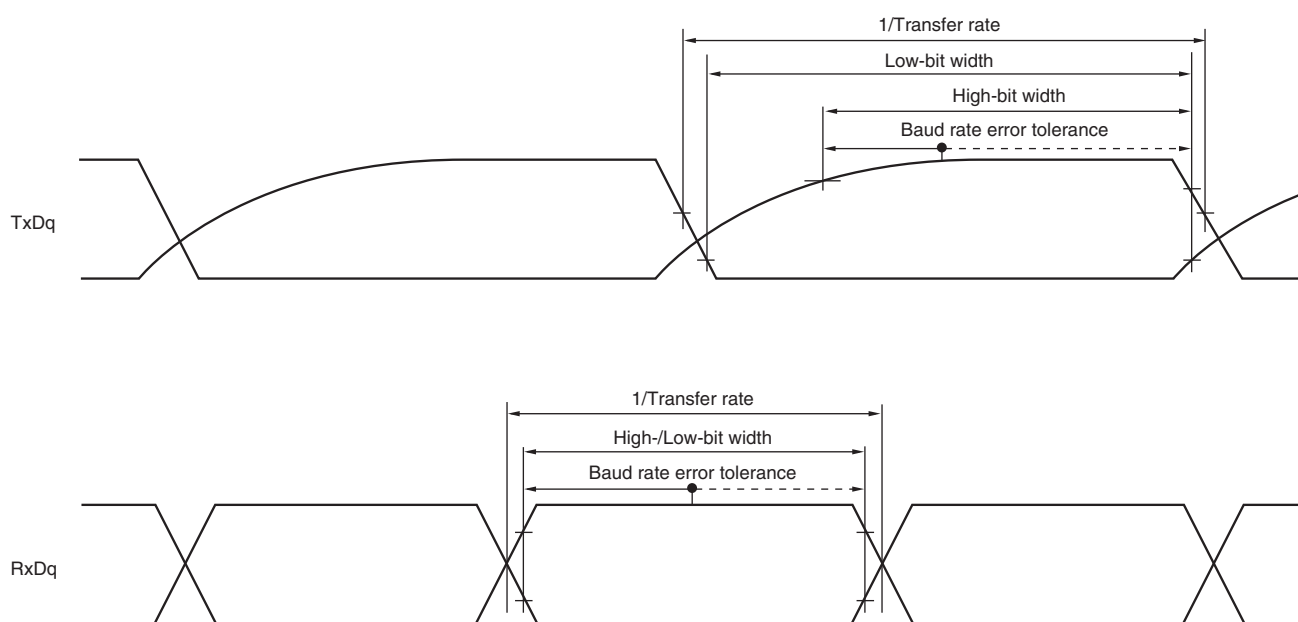
$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

9. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 8** above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output ( $V_{DD}$  tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). **For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.**

**UART mode connection diagram (during communication at different potential)****UART mode bit width (during communication at different potential) (reference)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  $C_b[\text{F}]$ : Communication line (TxDq) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)
  3.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))
  4. UART0 of the 20- and 24-pin products supports communication at different potential only when the peripheral I/O redirection function is not used.



**(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**  
**(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time <sup>Note 1</sup>	t <sub>KCY2</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V	20 MHz < f <sub>MCK</sub> ≤ 24 MHz	12/f <sub>MCK</sub>		—		ns
			8 MHz < f <sub>MCK</sub> ≤ 20 MHz	10/f <sub>MCK</sub>		—		ns
			4 MHz < f <sub>MCK</sub> ≤ 8 MHz	8/f <sub>MCK</sub>		16/f <sub>MCK</sub>		ns
			f <sub>MCK</sub> ≤ 4 MHz	6/f <sub>MCK</sub>		10/f <sub>MCK</sub>		ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V	20 MHz < f <sub>MCK</sub> ≤ 24 MHz	16/f <sub>MCK</sub>		—		ns
			16 MHz < f <sub>MCK</sub> ≤ 20 MHz	14/f <sub>MCK</sub>		—		ns
			8 MHz < f <sub>MCK</sub> ≤ 16 MHz	12/f <sub>MCK</sub>		—		ns
			4 MHz < f <sub>MCK</sub> ≤ 8 MHz	8/f <sub>MCK</sub>		16/f <sub>MCK</sub>		ns
			f <sub>MCK</sub> ≤ 4 MHz	6/f <sub>MCK</sub>		10/f <sub>MCK</sub>		ns
		1.8 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup>	20 MHz < f <sub>MCK</sub> ≤ 24 MHz	36/f <sub>MCK</sub>		—		ns
			16 MHz < f <sub>MCK</sub> ≤ 20 MHz	32/f <sub>MCK</sub>		—		ns
			8 MHz < f <sub>MCK</sub> ≤ 16 MHz	26/f <sub>MCK</sub>		—		ns
			4 MHz < f <sub>MCK</sub> ≤ 8 MHz	16/f <sub>MCK</sub>		16/f <sub>MCK</sub>		ns
			f <sub>MCK</sub> ≤ 4 MHz	10/f <sub>MCK</sub>		10/f <sub>MCK</sub>		ns
SCKp high-/low-level width	t <sub>KH2</sub> , t <sub>KL2</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V		t <sub>KCY2</sub> /2 - 12		t <sub>KCY2</sub> /2 - 50		ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V		t <sub>KCY2</sub> /2 - 18		t <sub>KCY2</sub> /2 - 50		ns
		1.8 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup>		t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		ns
Slp setup time (to SCKp↑) <sup>Note 3</sup>	t <sub>SIK2</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>DD</sub> ≤ 4.0 V		1/f <sub>MCK</sub> + 20		1/f <sub>MCK</sub> + 30		ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V		1/f <sub>MCK</sub> + 20		1/f <sub>MCK</sub> + 30		ns
		1.8 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>DD</sub> ≤ 2.0 V <sup>Note 2</sup>		1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		ns
Slp hold time (from SCKp↑) <sup>Note 4</sup>	t <sub>KSI2</sub>			1/f <sub>MCK</sub> + 31		1/f <sub>MCK</sub> + 31		ns
Delay time from SCKp↓ to SOP output <sup>Note 5</sup>	t <sub>KSO2</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ			2/f <sub>MCK</sub> + 120		2/f <sub>MCK</sub> + 573	ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ			2/f <sub>MCK</sub> + 214		2/f <sub>MCK</sub> + 573	ns
		1.8 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ			2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573	ns

**Notes** 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

2. Use it with V<sub>DD</sub> ≥ V<sub>b</sub>.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

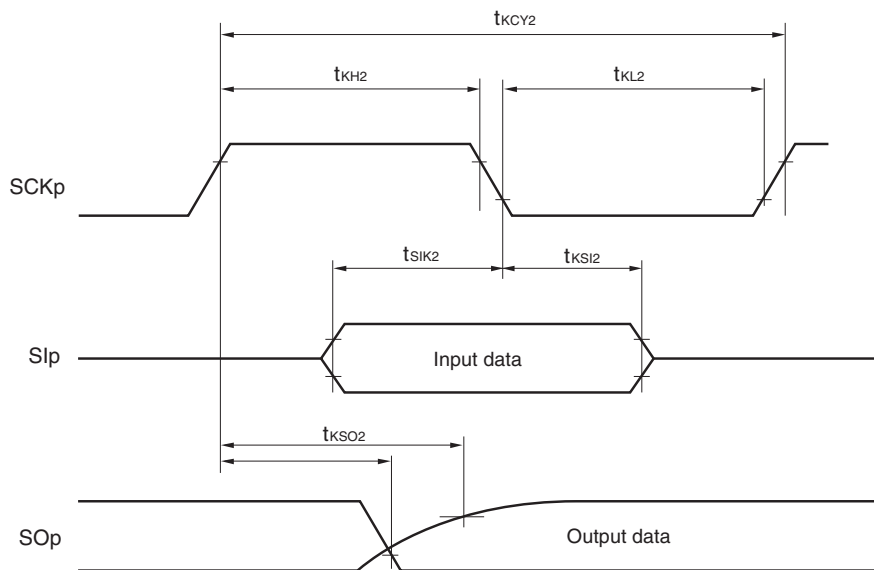
5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOP output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Cautions** 1. Select the TTL input buffer for the Slp and SCKp pins and the N-ch open drain output (V<sub>DD</sub> tolerance) mode for the SOP pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).

**For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.**

2. CSI01 and CSI11 cannot communicate at different potential.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



**Remark** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

## 2.6.2 Temperature sensor/internal reference voltage characteristics

**( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , HS (high-speed main) mode)**

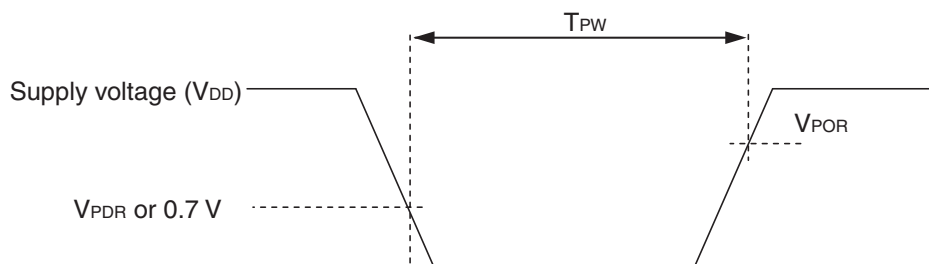
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	$V_{TMPS25}$	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference voltage	$V_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	$F_{VTMPS}$	Temperature sensor output voltage that depends on the temperature		-3.6		mV/ $^\circ\text{C}$
Operation stabilization wait time	$t_{AMP}$		5			$\mu\text{s}$

## 2.6.3 POR circuit characteristics

**( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{POR}$	Power supply rise time	1.47	1.51	1.55	V
	$V_{PDR}$	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width <sup>Note</sup>	$T_{PW}$		300			$\mu\text{s}$

**Note** Minimum time required for a POR reset when  $V_{DD}$  exceeds below  $V_{PDR}$ . This is also the minimum time required for a POR reset from when  $V_{DD}$  exceeds below 0.7 V to when  $V_{DD}$  exceeds  $V_{POR}$  while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 2.6.4 LVD circuit characteristics

## LVD Detection Voltage of Reset Mode and Interrupt Mode

(T<sub>A</sub> = -40 to +85°C, V<sub>PDR</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	V <sub>LVD0</sub>	Power supply rise time	3.98	4.06	4.14	V
		Power supply fall time	3.90	3.98	4.06	V
	V <sub>LVD1</sub>	Power supply rise time	3.68	3.75	3.82	V
		Power supply fall time	3.60	3.67	3.74	V
	V <sub>LVD2</sub>	Power supply rise time	3.07	3.13	3.19	V
		Power supply fall time	3.00	3.06	3.12	V
	V <sub>LVD3</sub>	Power supply rise time	2.96	3.02	3.08	V
		Power supply fall time	2.90	2.96	3.02	V
	V <sub>LVD4</sub>	Power supply rise time	2.86	2.92	2.97	V
		Power supply fall time	2.80	2.86	2.91	V
	V <sub>LVD5</sub>	Power supply rise time	2.76	2.81	2.87	V
		Power supply fall time	2.70	2.75	2.81	V
	V <sub>LVD6</sub>	Power supply rise time	2.66	2.71	2.76	V
		Power supply fall time	2.60	2.65	2.70	V
	V <sub>LVD7</sub>	Power supply rise time	2.56	2.61	2.66	V
		Power supply fall time	2.50	2.55	2.60	V
	V <sub>LVD8</sub>	Power supply rise time	2.45	2.50	2.55	V
		Power supply fall time	2.40	2.45	2.50	V
	V <sub>LVD9</sub>	Power supply rise time	2.05	2.09	2.13	V
		Power supply fall time	2.00	2.04	2.08	V
	V <sub>LVD10</sub>	Power supply rise time	1.94	1.98	2.02	V
		Power supply fall time	1.90	1.94	1.98	V
	V <sub>LVD11</sub>	Power supply rise time	1.84	1.88	1.91	V
		Power supply fall time	1.80	1.84	1.87	V
Minimum pulse width	t <sub>LW</sub>		300			μs
Detection delay time					300	μs

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

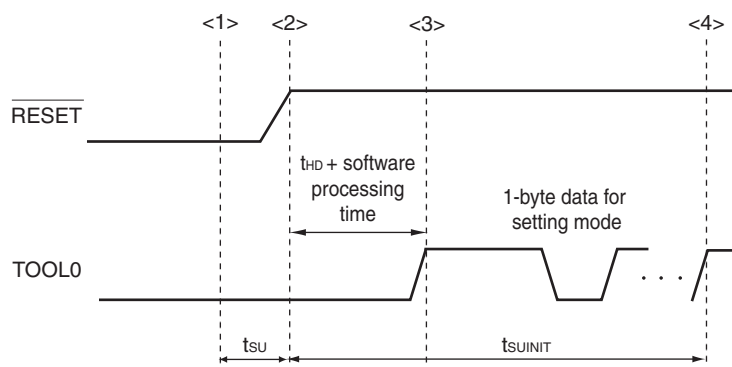
( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

## 2.10 Timing of Entry to Flash Memory Programming Modes

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	$t_{\text{SUNIT}}$	POR and LVD reset are released before external reset release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	$t_{\text{SU}}$	POR and LVD reset are released before external reset release	10			$\mu\text{s}$
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	$t_{\text{HD}}$	POR and LVD reset are released before external reset release	1			ms

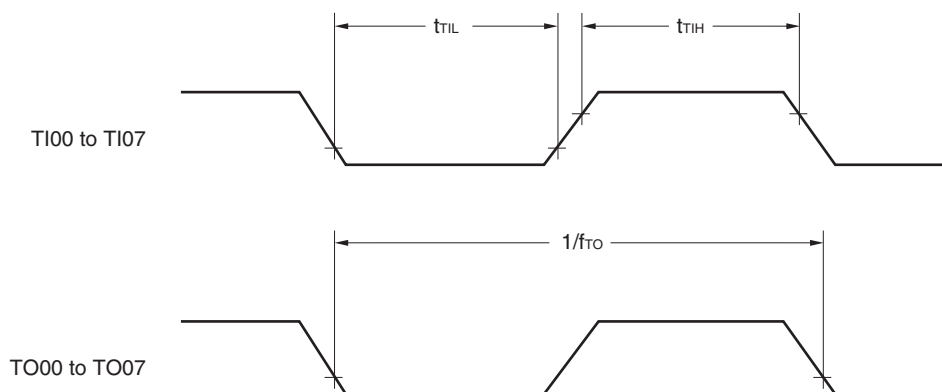
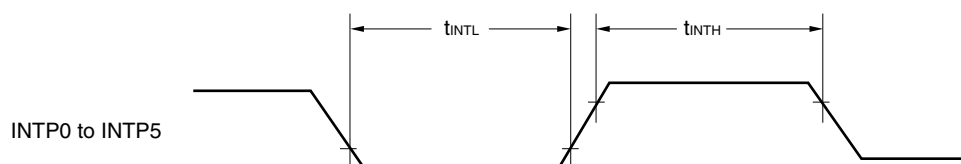
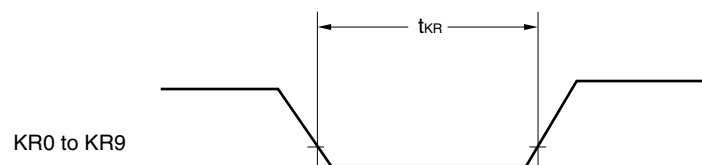
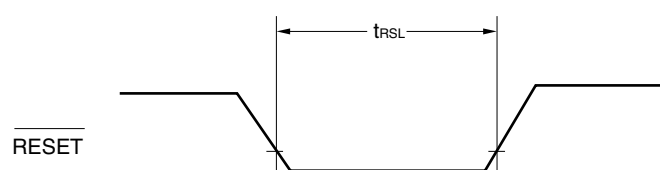


- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark**  $t_{\text{SUNIT}}$ : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{\text{SU}}$ : Time to release the external reset after the TOOL0 pin is set to the low level

$t_{\text{HD}}$ : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

**TI/TO Timing****Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

**(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

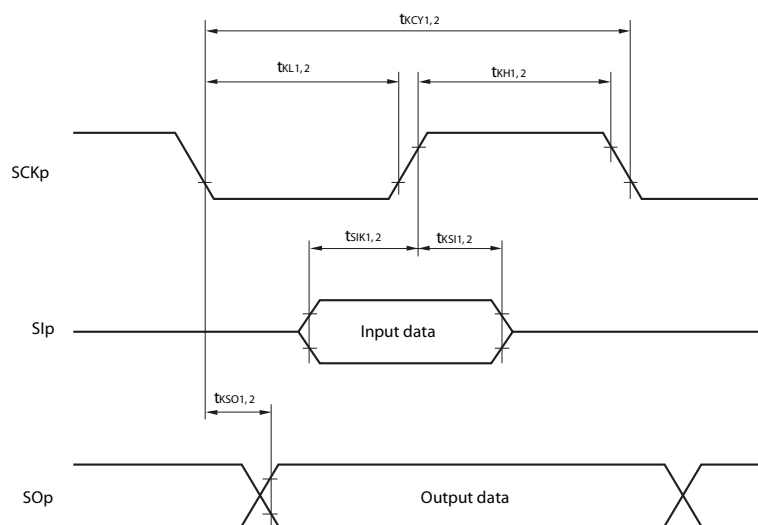
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	$t_{KCY1}$	$t_{KCY1} \geq 4/f_{CLK}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	334	ns
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	500	ns
SCKp high-/low-level width	$t_{KH1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2-24$		ns
	$t_{KL1}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2-36$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2-76$		ns
Slp setup time (to SCKp $\uparrow$ ) <sup>Note 1</sup>	$t_{SIK1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	113		ns
Slp hold time (from SCKp $\uparrow$ ) <sup>Note 2</sup>	$t_{KSI1}$		38		ns
Delay time from SCKp $\downarrow$ to SOp output <sup>Note 3</sup>	$t_{KSO1}$	$C = 30\text{ pF}$ <sup>Note 4</sup>		50	ns

- Notes**
1. When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The Slp setup time becomes “to SCKp $\downarrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
  2. When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The Slp hold time becomes “from SCKp $\downarrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
  3. When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The delay time to SOp output becomes “from SCKp $\uparrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
  4. C is the load capacitance of the SCKp and SOp output lines.

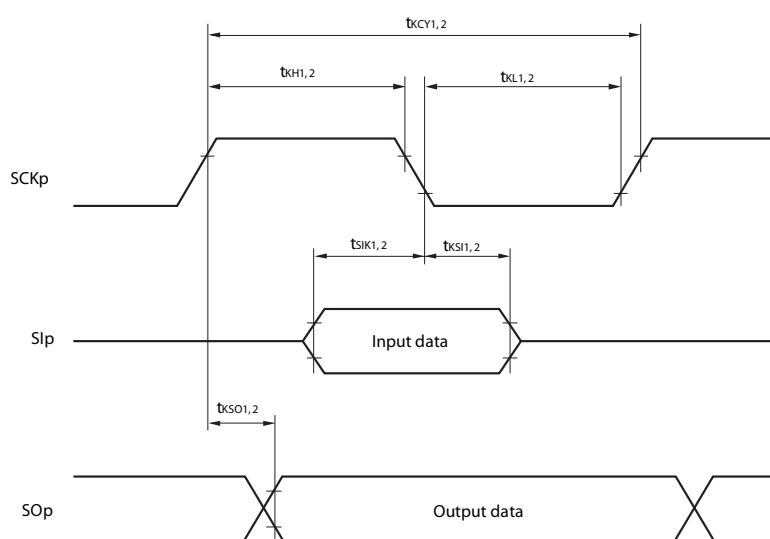
**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

- Remarks**
1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)
  2.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3))

**CSI mode serial transfer timing (during communication at same potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



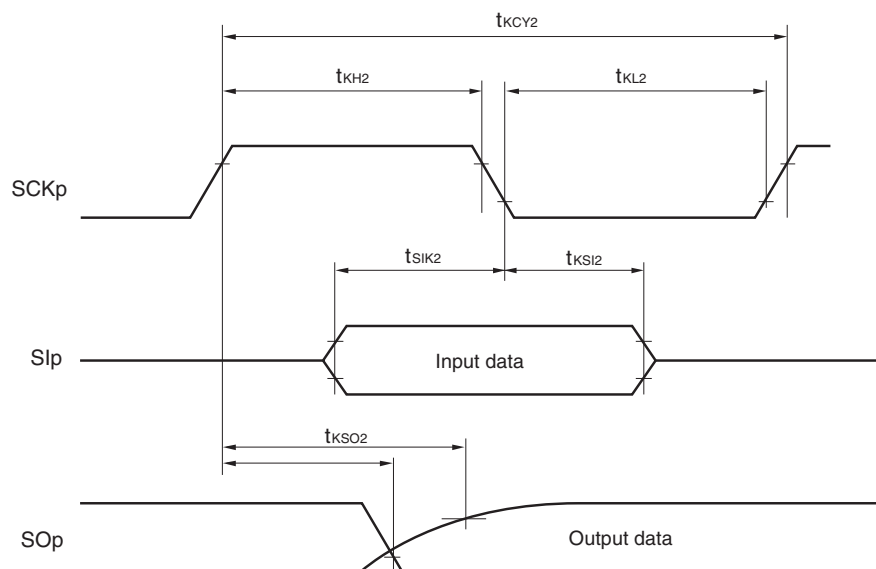
**CSI mode serial transfer timing (during communication at same potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks**
1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)
  2.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3))



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .)**



**Remark** p: CSI number ( $p = 00, 20$ ), m: Unit number ( $m = 0, 1$ ), n: Channel number ( $n = 0$ )

## 3.5.2 Serial interface IICA

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	HS (high-speed main) mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f <sub>SCL</sub>	Fast mode: f <sub>CLK</sub> ≥ 3.5 MHz			0	400	kHz
		Normal mode: f <sub>CLK</sub> ≥ 1 MHz	0	100			kHz
Setup time of restart condition	t <sub>SU:STA</sub>		4.7		0.6		μs
Hold time <sup>Note 1</sup>	t <sub>HD:STA</sub>		4.0		0.6		μs
Hold time when SCLA0 = “L”	t <sub>LOW</sub>		4.7		1.3		μs
Hold time when SCLA0 = “H”	t <sub>HIGH</sub>		4.0		0.6		μs
Data setup time (reception)	t <sub>SU:DAT</sub>		250		100		ns
Data hold time (transmission) <sup>Note 2</sup>	t <sub>HD:DAT</sub>		0	3.45	0	0.9	μs
Setup time of stop condition	t <sub>SU:STO</sub>		4.0		0.6		μs
Bus-free time	t <sub>BUF</sub>		4.7		1.3		μs

**Notes** 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R> 2. The maximum value (MAX.) of  $t_{HD:DAT}$  is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

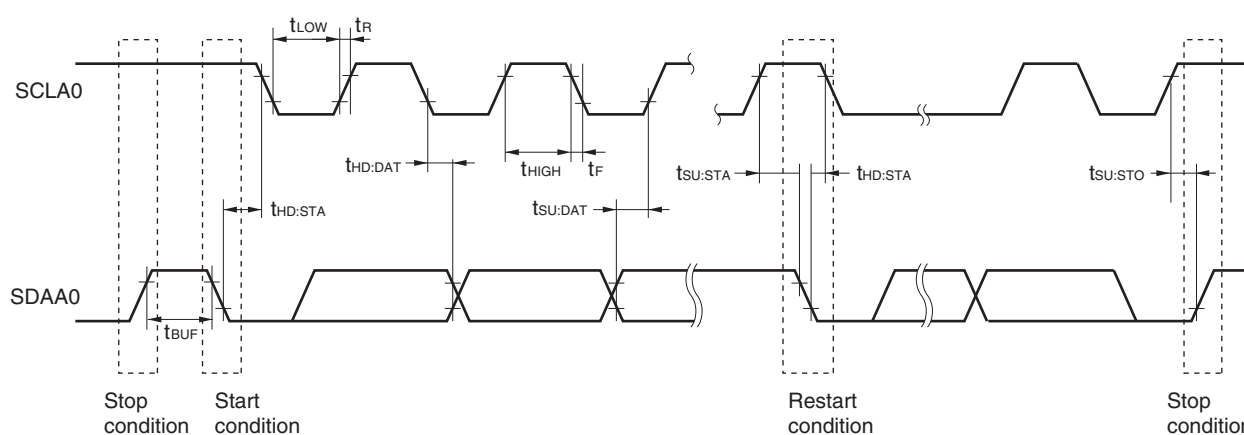
**Caution** Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ( $I_{OH1}$ ,  $I_{OL1}$ ,  $V_{OH1}$ ,  $V_{OL1}$ ) must satisfy the values in the redirect destination.

**Remark** The maximum value of  $C_b$  (communication line capacitance) and the value of  $R_b$  (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode:  $C_b = 400\text{ pF}$ ,  $R_b = 2.7\text{ k}\Omega$

Fast mode:  $C_b = 320\text{ pF}$ ,  $R_b = 1.1\text{ k}\Omega$

IICA serial transfer timing



### 3.6 Analog Characteristics

#### 3.6.1 A/D converter characteristics

##### Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = $AV_{REFP}$ Reference voltage (-) = $AV_{REFM}$	Reference voltage (+) = $V_{DD}$ Reference voltage (-) = $V_{SS}$	Reference voltage (+) = $V_{BGR}$ Reference voltage (-) = $AV_{REFM}$
ANI0 to ANI3	Refer to 29.6.1 (1).	Refer to 29.6.1 (3).	Refer to 29.6.1 (4).
ANI16 to ANI22	Refer to 29.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 29.6.1 (1).		—

(1) When reference voltage (+) =  $AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ), reference voltage (-) =  $AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ , Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ <sup>Note 3</sup>		1.2	$\pm 3.5$	LSB
Conversion time	$t_{CONV}$	10-bit resolution Target pin: ANI2, ANI3	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	$\mu\text{s}$
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	$\mu\text{s}$
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375	39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625	39	$\mu\text{s}$
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ <sup>Note 3</sup>			$\pm 0.25$	%FSR
Full-scale error <sup>Notes 1, 2</sup>	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ <sup>Note 3</sup>			$\pm 0.25$	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ <sup>Note 3</sup>			$\pm 2.5$	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ <sup>Note 3</sup>			$\pm 1.5$	LSB
Analog input voltage	$V_{AIN}$	ANI2, ANI3	0		$AV_{REFP}$	V
		Internal reference voltage (HS (high-speed main) mode)	$V_{BGR}$ <sup>Note 4</sup>			V
		Temperature sensor output voltage (HS (high-speed main) mode)	$V_{TMPS25}$ <sup>Note 4</sup>			V

(Notes are listed on the next page.)

## 3.6.2 Temperature sensor/internal reference voltage characteristics

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , HS (high-speed main) mode)**

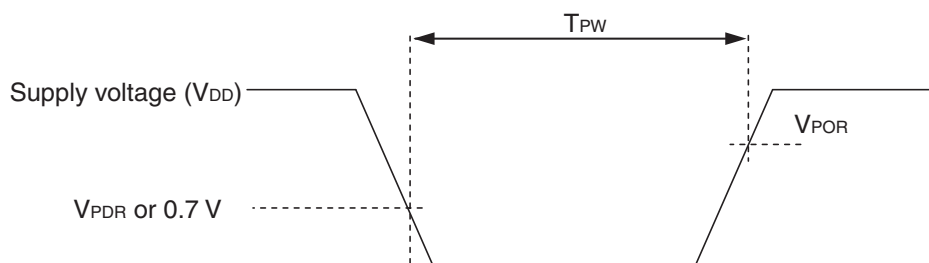
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	$V_{TMS25}$	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference voltage	$V_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	$F_{VTMS}$	Temperature sensor output voltage that depends on the temperature		-3.6		mV/ $^\circ\text{C}$
Operation stabilization wait time	$t_{AMP}$		5			$\mu\text{s}$

## 3.6.3 POR circuit characteristics

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{POR}$	Power supply rise time	1.45	1.51	1.57	V
	$V_{PDR}$	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width <sup>Note</sup>	$T_{PW}$		300			$\mu\text{s}$

**Note** Minimum time required for a POR reset when  $V_{DD}$  exceeds below  $V_{PDR}$ . This is also the minimum time required for a POR reset from when  $V_{DD}$  exceeds below 0.7 V to when  $V_{DD}$  exceeds  $V_{POR}$  while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 3.9 Dedicated Flash Memory Programmer Communication (UART)

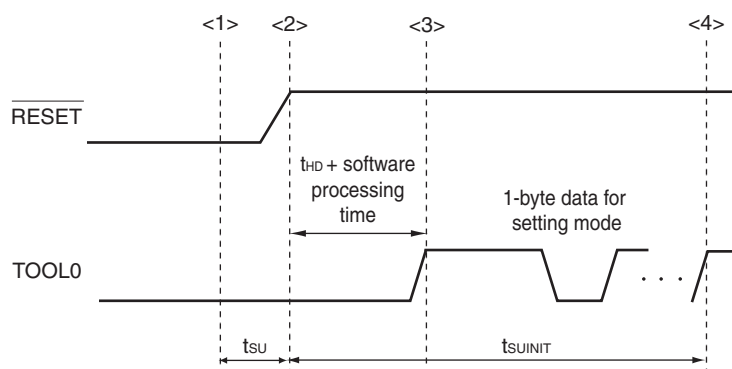
**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

## 3.10 Timing of Entry to Flash Memory Programming Modes

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	$t_{\text{SUNIT}}$	POR and LVD reset are released before external release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	$t_{\text{SU}}$	POR and LVD reset are released before external release	10			$\mu\text{s}$
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	$t_{\text{HD}}$	POR and LVD reset are released before external release	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark**  $t_{\text{SUNIT}}$ : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{\text{SU}}$ : Time to release the external reset after the TOOL0 pin is set to the low level

$t_{\text{HD}}$ : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)