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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f102aadsp-x0

1.3 Differences between the R5F102 Products and the R5F103 Products

The following are differences between the R5F102 products and the R5F103 products.

○ Whether the data flash memory is mounted or not

○ High-speed on-chip oscillator oscillation frequency accuracy

○ Number of channels in serial interface

○ Whether the DMA function is mounted or not

○ Whether a part of the safety functions are mounted or not

1.3.1 Data Flash

The data flash memory of 2 KB is mounted on the R5F102 products, but not on the R5F103 products.

Product	Data Flash
R5F102 products R5F1026A, R5F1027A, R5F102AA, R5F10269, R5F10279, R5F102A9, R5F10268, R5F10278, R5F102A8, R5F10267, R5F10277, R5F102A7, R5F10266 ^{Note}	2KB
R5F103 products R5F1036A, R5F1037A, R5F103AA, R5F10369, R5F10379, R5F103A9, R5F10368, R5F10378 R5F103A8, R5F10367, R5F10377, R5F103A7, R5F10366	Not mounted

Note The RAM in the R5F10266 has capacity as small as 256 bytes. Depending on the customer's program specification, the stack area to execute the data flash library may not be kept and data may not be written to or erased from the data flash memory.

Caution When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

1.5 Pin Identification

ANI0 to ANI3, ANI16 to ANI22:	Analog input	REGC: $\overline{\text{RESET}}$:	Regulator Capacitance Reset
AV$_{REFM}$:	Analog Reference Voltage Minus	RxD0 to RxD2:	Receive Data
AV$_{REFP}$:	Analog reference voltage plus	SCK00, SCK01, SCK11,	
EXCLK:	External Clock Input	SCK20:	Serial Clock Input/Output
	(Main System Clock)	SCL00, SCL01,	
INTP0 to INTP5	Interrupt Request From Peripheral	SCL11, SCL20, SCLA0:	Serial Clock Input/Output
KR0 to KR9:	Key Return	SDA00, SDA01, SDA11,	
P00 to P03:	Port 0	SDA20, SDAA0:	Serial Data Input/Output
P10 to P17:	Port 1	SI00, SI01, SI11, SI20:	Serial Data Input
P20 to P23:	Port 2	SO00, SO01, SO11,	
P30 to P31:	Port 3	SO20:	Serial Data Output
P40 to P42:	Port 4	TI00 to TI07:	Timer Input
P50, P51:	Port 5	TO00 to TO07:	Timer Output
P60, P61:	Port 6	TOOL0:	Data Input/Output for Tool
P120 to P122, P125:	Port 12	TOOLRxD, TOOLTxD:	Data Input/Output for External
P137:	Port 13		Device
P147:	Port 14	TxD0 to TxD2:	Transmit Data
PCLBUZ0, PCLBUZ1:	Programmable Clock Output/	V$_{DD}$:	Power supply
	Buzzer Output	V$_{SS}$:	Ground
		X1, X2:	Crystal Oscillator (Main System Clock)

(2/2)

Item		20-pin		24-pin		30-pin	
		R5F1026x	R5F1036x	R5F1027x	R5F1037x	R5F102Ax	R5F103Ax
Clock output/buzzer output		1				2	
		2.44 kHz to 10 MHz: (Peripheral hardware clock: f_{MAIN} = 20 MHz operation)					
8/10-bit resolution A/D converter		11 channels				8 channels	
Serial interface		[R5F1026x (20-pin), R5F1027x (24-pin)] · CSI: 2 channels/Simplified I^{2}C: 2 channels/UART: 1 channel [R5F102Ax (30-pin)] · CSI: 1 channel/Simplified I^{2}C: 1 channel/UART: 1 channel · CSI: 1 channel/Simplified I^{2}C: 1 channel/UART: 1 channel · CSI: 1 channel/Simplified I^{2}C: 1 channel/UART: 1 channel [R5F1036x (20-pin), R5F1037x (24-pin)] · CSI: 1 channel/Simplified I^{2}C: 0 channel/UART: 1 channel [R5F103Ax (30-pin)] · CSI: 1 channel/Simplified I^{2}C: 0 channel/UART: 1 channel					
	I^{2}C bus	1 channel					
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (unsigned or signed) • 32 bits × 32 bits = 32 bits (unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (unsigned or signed)					
DMA controller		2 channels	—	2 channels	—	2 channels	—
Vectored interrupt sources	Internal	18	16	18	16	26	19
	External	5				6	
Key interrupt		6		10		—	
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access					
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP) • Power-down-reset: 1.50 V (TYP)					
Voltage detector		• Rising edge : 1.88 to 4.06 V (12 stages) • Falling edge : 1.84 to 3.98 V (12 stages)					
On-chip debug function		Provided					
Power supply voltage		V_{DD} = 1.8 to 5.5 V					
Operating ambient temperature		T_A = −40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = −40 to +105°C (G: Industrial applications)					

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T$_A$ = 25°C)

Parameter	Symbols	Conditions			Ratings	Unit
Supply Voltage	V$_{DD}$				−0.5 to + 6.5	V
REGC terminal input voltage[Note1]	V$_{IREGC}$	REGC			−0.3 to +2.8 and −0.3 to V$_{DD}$ + 0.3 [Note 2]	V
Input Voltage	V$_{I1}$	Other than P60, P61			−0.3 to V$_{DD}$ + 0.3[Note 3]	V
	V$_{I2}$	P60, P61 (N-ch open drain)			−0.3 to 6.5	V
Output Voltage	V$_O$				−0.3 to V$_{DD}$ + 0.3[Note 3]	V
Analog input voltage	V$_{AI}$	20-, 24-pin products: ANI0 to ANI3, ANI16 to ANI22 30-pin products: ANI0 to ANI3, ANI16 to ANI19			−0.3 to V$_{DD}$ + 0.3 and −0.3 to AVREF(+)+0.3[Notes 3, 4]	V
Output current, high	I$_{OH1}$	Per pin	Other than P20 to P23		−40	mA
		Total of all pins	All the terminals other than P20 to P23		−170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120		−70	mA
			20-, 24-pin products: P00 to P03[Note 5], P10 to P14 30-pin products: P10 to P17, P30, P31, P50, P51, P147		−100	mA
	I$_{OH2}$	Per pin	P20 to P23		−0.5	mA
		Total of all pins			−2	mA
Output current, low	I$_{OL1}$	Per pin	Other than P20 to P23		40	mA
		Total of all pins	All the terminals other than P20 to P23		170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120		70	mA
			20-, 24-pin products: P00 to P03[Note 5], P10 to P14, P60, P61 30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147		100	mA
	I$_{OL2}$	Per pin	P20 to P23		1	mA
		Total of all pins			5	mA
Operating ambient temperature	T$_A$				−40 to +85	°C
Storage temperature	T$_{stg}$				−65 to +150	°C

Notes **1.**   30-pin product only.

2.   Connect the REGC pin to V$_{SS}$ via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.

3.   Must be 6.5 V or lower.

4.   Do not exceed AV$_{REF}$(+) + 0.3 V in case of A/D conversion target pin.

5.   24-pin products only.

Caution   Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1.   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.   AV$_{REF}$(+) : + side reference voltage of the A/D converter.

3.   V$_{SS}$: Reference voltage

## 2.4 AC Characteristics

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T$_{CY}$	Main system clock (f$_{MAIN}$) operation	HS (High-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.125		1	μs
		During self programming	HS (High-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.125		1	μs
External main system clock frequency	f$_{EX}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V$_{DD}$ < 2.4 V			1.0		8.0	MHz
External main system clock input high-level width, low-level width	t$_{EXH}$, t$_{EXL}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			24			ns
		2.4 V ≤ V$_{DD}$ < 2.7 V			30			ns
		1.8 V ≤ V$_{DD}$ < 2.4 V			60			ns
TI00 to TI07 input high-level width, low-level width	t$_{TIH}$, t$_{TIL}$				1/f$_{MCK}$ + 10			ns
TO00 to TO07 output frequency	f$_{TO}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V					12	MHz
		2.7 V ≤ V$_{DD}$ < 4.0 V					8	MHz
		1.8 V ≤ V$_{DD}$ < 2.7 V					4	MHz
PCLBUZ0, or PCLBUZ1 output frequency	f$_{PCL}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V					16	MHz
		2.7 V ≤ V$_{DD}$ < 4.0 V					8	MHz
		1.8 V ≤ V$_{DD}$ < 2.7 V					4	MHz
INTP0 to INTP5 input high-level width, low-level width	t$_{INTH}$, t$_{INTL}$				1			μs
KR0 to KR9 input available width	t$_{KR}$				250			ns
$\overline{RESET}$ low-level width	t$_{RSL}$				10			μs

Remark   f$_{MCK}$: Timer array unit operation clock frequency

(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

2.5 Peripheral Functions Characteristics

AC Timing Test Point
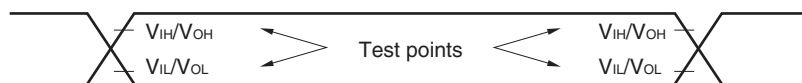
2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1				f$_{MCK}$/6		f$_{MCK}$/6	bps
		Theoretical value of the maximum transfer rate f$_{CLK}$ = f$_{MCK}$^{Note2}		4.0		1.3	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f$_{CLK}$) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ V$_{DD}$ ≤ 5.5 V)

16 MHz (2.4 V ≤ V$_{DD}$ ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ V$_{DD}$ ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)

UART mode bit width (during communication at same potential) (reference)

Remarks 1. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

2. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

RENESAS
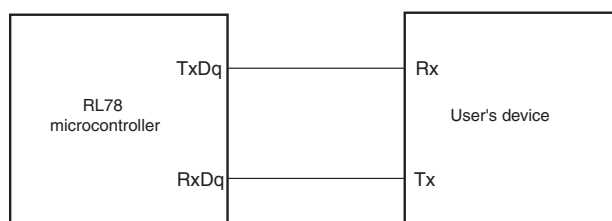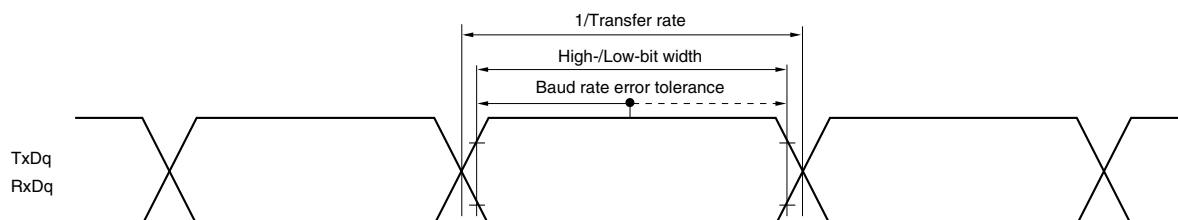
(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time [Note4]	t$_{KCY2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	20 MHz < f$_{MCK}$	8/f$_{MCK}$		−		ns
			f$_{MCK}$ ≤ 20 MHz	6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V	16 MHz < f$_{MCK}$	8/f$_{MCK}$		−		ns
			f$_{MCK}$ ≤ 16 MHz	6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		6/f$_{MCK}$ and 750		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2−7		t$_{KCY2}$/2−7		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2−8		t$_{KCY2}$/2−8		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2−18		t$_{KCY2}$/2−18		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		t$_{KCY2}$/2−18		ns
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK2}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$ + 20		1/f$_{MCK}$ + 30		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		1/f$_{MCK}$ + 30		ns
SIp hold time (from SCKp↑) [Note 2]	t$_{KSI2}$			1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns
Delay time from SCKp↓ to SOp output [Note 3]	t$_{KSO2}$	C = 30 pF [Note4]	2.7 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{MCK}$ + 44		2/f$_{MCK}$ + 110	ns
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{MCK}$ + 75		2/f$_{MCK}$ + 110	ns
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		2/f$_{MCK}$ + 110	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	81		479		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	177		479		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	479		479		ns
SIp hold time (from SCKp↑) [Note 1]	t$_{KSI1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	19		19		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	19		19		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	19		19		ns
Delay time from SCKp↓ to SOp output [Note 1]	t$_{KSO1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		100		100	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		195		195	ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		483		483	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

      2. Use it with V$_{DD}$ ≥ V$_b$.

(**Cautions** and **Remarks** are listed on the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	20 MHz < f$_{MCK}$ ≤ 24 MHz	12/f$_{MCK}$		−		ns
			8 MHz < f$_{MCK}$ ≤ 20 MHz	10/f$_{MCK}$		−		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/f$_{MCK}$		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	20 MHz < f$_{MCK}$ ≤ 24 MHz	16/f$_{MCK}$		−		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	14/f$_{MCK}$		−		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	12/f$_{MCK}$		−		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/f$_{MCK}$		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]	20 MHz < f$_{MCK}$ ≤ 24 MHz	36/f$_{MCK}$		−		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	32/f$_{MCK}$		−		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	26/f$_{MCK}$		−		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	10/f$_{MCK}$		10/f$_{MCK}$		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		t$_{KCY2}$/2 − 12		t$_{KCY2}$/2 − 50		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		t$_{KCY2}$/2 − 18		t$_{KCY2}$/2 − 50		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]		t$_{KCY2}$/2 − 50		t$_{KCY2}$/2 − 50		ns
SIp setup time (to SCKp↑) [Note 3]	t$_{SIK2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_{DD}$ ≤ 4.0 V		1/f$_{MCK}$ + 20		1/f$_{MCK}$ + 30		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		1/f$_{MCK}$ + 20		1/f$_{MCK}$ + 30		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_{DD}$ ≤ 2.0 V [Note 2]		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
SIp hold time (from SCKp↑) [Note 4]	t$_{KSI2}$			1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns
Delay time from SCKp↓ to SOp output [Note 5]	t$_{KSO2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ			2/f$_{MCK}$ + 120		2/f$_{MCK}$ + 573	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ			2/f$_{MCK}$ + 214		2/f$_{MCK}$ + 573	ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ			2/f$_{MCK}$ + 573		2/f$_{MCK}$ + 573	ns

Notes 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

2. Use it with V$_{DD}$ ≥ V$_b$.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Cautions 1. Select the TTL input buffer for the SIp and SCKp pins and the N-ch open drain output (V$_{DD}$ tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).
For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

2. CSI01 and CSI11 cannot communicate at different potential.

(3) When reference voltage (+) = V$_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (−) = V$_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = V$_{DD}$, Reference voltage (−) = V$_{SS}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution			1.2	±7.0	LSB
					1.2	±10.5 [Note 3]	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
				57		95	μs
Conversion time	t$_{CONV}$	10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution				±0.60	%FSR
						±0.85 [Note 3]	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution				±0.60	%FSR
						±0.85 [Note 3]	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution				±4.0	LSB
						±6.5 [Note 3]	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution				±2.0	LSB
						±2.5 [Note 3]	LSB
Analog input voltage	V$_{AIN}$	ANI0 to ANI3, ANI16 to ANI22		0		V$_{DD}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)		V$_{BGR}$ [Note 4]			V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)		V$_{TMPS25}$ [Note 4]			V

Notes 1. Excludes quantization error (±1/2 LSB).

    2. This value is indicated as a ratio (%FSR) to the full-scale value.

    3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

    4. Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) 30-pin products

$(T_A = -40$ to $+105°C$, 2.4 V $\leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)   (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS (High-speed main) mode[Note 4]	f_{IH} = 24 MHz[Note 3]	Basic operation	V_{DD} = 5.0 V		1.5		mA
						V_{DD} = 3.0 V		1.5		
					Normal operation	V_{DD} = 5.0 V		3.7	5.8	mA
						V_{DD} = 3.0 V		3.7	5.8	
				f_{IH} = 16 MHz[Note 3]		V_{DD} = 5.0 V		2.7	4.2	mA
						V_{DD} = 3.0 V		2.7	4.2	
				f_{MX} = 20 MHz[Note 2], V_{DD} = 5.0 V		Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	
				f_{MX} = 20 MHz[Note 2], V_{DD} = 3.0 V		Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 5.0 V		Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 3.0 V		Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

    2. When high-speed on-chip oscillator clock is stopped.

    3. When high-speed system clock is stopped

    4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

        HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz

                                      V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

    2. f_{IH}: high-speed on-chip oscillator clock frequency

    3. Temperature condition of the TYP. value is T_A = 25°C.

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(2) 30-pin products

(T_A = −40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)   (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I_{DD2} [Note 2]	HALT mode	HS (High-speed main) mode [Note 6]	f_{IH} = 24 MHz [Note 4]	V_{DD} = 5.0 V		440	2300	μA
					V_{DD} = 3.0 V		440	2300	
				f_{IH} = 16 MHz [Note 4]	V_{DD} = 5.0 V		400	1700	μA
					V_{DD} = 3.0 V		400	1700	
				f_{MX} = 20 MHz [Note 3], V_{DD} = 5.0 V	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				f_{MX} = 20 MHz [Note 3], V_{DD} = 3.0 V	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				f_{MX} = 10 MHz [Note 3], V_{DD} = 5.0 V	Square wave input		190	1020	μA
					Resonator connection		260	1100	
				f_{MX} = 10 MHz [Note 3], V_{DD} = 3.0 V	Square wave input		190	1020	μA
					Resonator connection		260	1100	
	I_{DD3} [Note 5]	STOP mode	T_A = −40°C				0.18	0.50	μA
			T_A = +25°C				0.23	0.50	
			T_A = +50°C				0.30	1.10	
			T_A = +70°C				0.46	1.90	
			T_A = +85°C				0.75	3.30	
			T_A = +105°C				2.94	15.30	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

    2. During HALT instruction execution by flash memory.

    3. When high-speed on-chip oscillator clock is stopped.

    4. When high-speed system clock is stopped.

    5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

    6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

    HS (High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz

                           V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

    2. f_{IH}: high-speed on-chip oscillator clock frequency

    3. Except STOP mode, temperature condition of the TYP. value is T_A = 25°C.

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3.4 AC Characteristics

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T$_{CY}$	Main system clock (f$_{MAIN}$) operation	HS (High-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
		During self programming	HS (High-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
External main system clock frequency	f$_{EX}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V			1.0		16.0	MHz
External main system clock input high-level width, low-level width	t$_{EXH}$, t$_{EXL}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			24			ns
		2.4 V ≤ V$_{DD}$ < 2.7 V			30			ns
TI00 to TI07 input high-level width, low-level width	t$_{TIH}$, t$_{TIL}$				1/f$_{MCK}$ + 10			ns
TO00 to TO07 output frequency	f$_{TO}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V					12	MHz
		2.7 V ≤ V$_{DD}$ < 4.0 V					8	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V					4	MHz
PCLBUZ0, or PCLBUZ1 output frequency	f$_{PCL}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V					16	MHz
		2.7 V ≤ V$_{DD}$ < 4.0 V					8	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V					4	MHz
INTP0 to INTP5 input high-level width, low-level width	t$_{INTH}$, t$_{INTL}$				1			μs
KR0 to KR9 input available width	t$_{KR}$				250			ns
$\overline{RESET}$ low-level width	t$_{RSL}$				10			μs

Remark   f$_{MCK}$: Timer array unit operation clock frequency

(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

3.5 Peripheral Functions Characteristics

AC Timing Test Point
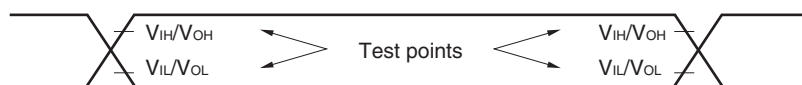
3.5.1 Serial array unit

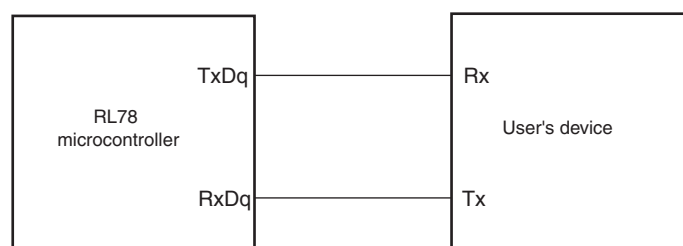**(1) During communication at same potential (UART mode)**

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate **Note 1**					f$_{MCK}$/12	bps
		Theoretical value of the maximum transfer rate f$_{CLK}$ = f$_{MCK}$**Note2**			2.0	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f$_{CLK}$) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ V$_{DD}$ ≤ 5.5 V)

16 MHz (2.4 V ≤ V$_{DD}$ ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)

UART mode bit width (during communication at same potential) (reference)
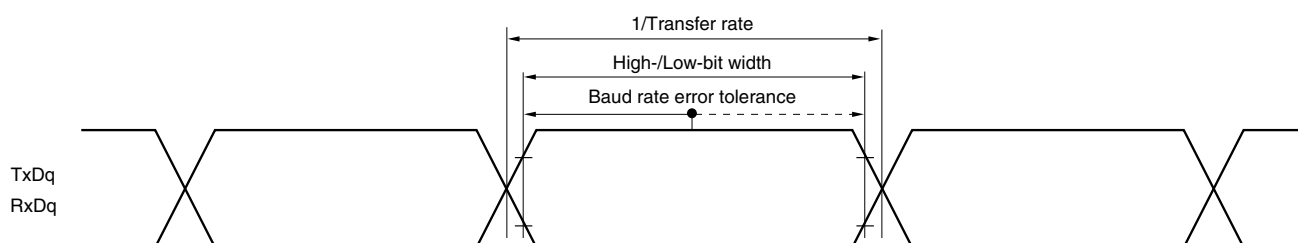
Remarks 1. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

2. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T$_A$ = $-$40 to +105°C, 2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ $\geq$ 4/f$_{CLK}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	334		ns
			2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	500		ns
SCKp high-/low-level width	t$_{KH1}$,	4.0 V $\leq$ V$_{DD}$ $\leq$ 5.5 V		t$_{KCY1}$/2$-$24		ns
	t$_{KL1}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V		t$_{KCY1}$/2$-$36		ns
		2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V		t$_{KCY1}$/2$-$76		ns
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK1}$	4.0 V $\leq$ V$_{DD}$ $\leq$ 5.5 V		66		ns
		2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V		66		ns
		2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V		113		ns
SIp hold time (from SCKp↑) [Note 2]	t$_{KSI1}$			38		ns
Delay time from SCKp↓ to SOp output [Note 3]	t$_{KSO1}$	C = 30 pF [Note4]			50	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)

2. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3))

$$\text{Baud rate error (theoretical value)} = \frac{\dfrac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \dfrac{2.2}{V_b})\}}{(\dfrac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

5. The smaller maximum transfer rate derived by using f$_{MCK}$/12 or the following expression is the valid maximum transfer rate.

   Expression for calculating the transfer rate when 2.7 V $\le$ V$_{DD}$ < 4.0 V and 2.3 V $\le$ V$_b$ $\le$ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln (1 - \dfrac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\dfrac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \dfrac{2.0}{V_b})\}}{(\dfrac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

7. The smaller maximum transfer rate derived by using f$_{MCK}$/12 or the following expression is the valid maximum transfer rate.

   Expression for calculating the transfer rate when 2.4 V $\le$ V$_{DD}$ < 3.3 V, 1.6 V $\le$ V$_b$ $\le$ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln (1 - \dfrac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\dfrac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \dfrac{1.5}{V_b})\}}{(\dfrac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

8. This value as an example is calculated when the conditions described in the "Conditions" column are   met. Refer to **Note 7** above to calculate the maximum transfer rate under conditions of the customer.

Caution   Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). **For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

(T_A = −40 to +105°C, 2.4 V ≤ V_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	600		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	1000		ns
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	2300		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 −150		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 −340		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 −916		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 −24		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 −36		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 −100		ns

Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

2. CSI01 and CSI11 cannot communicate at different potential.

Remarks 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSI number (p = 00, 20)

Simplified I²C mode connection diagram (during communication at different potential)
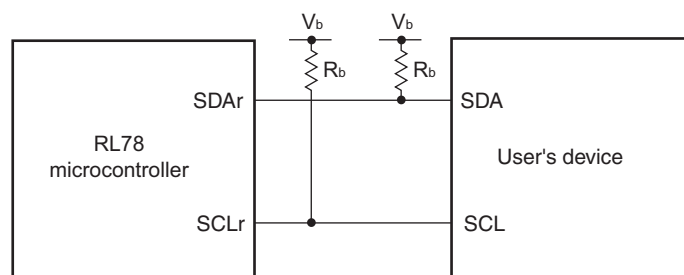
Simplified I²C mode serial transfer timing (during communication at different potential)
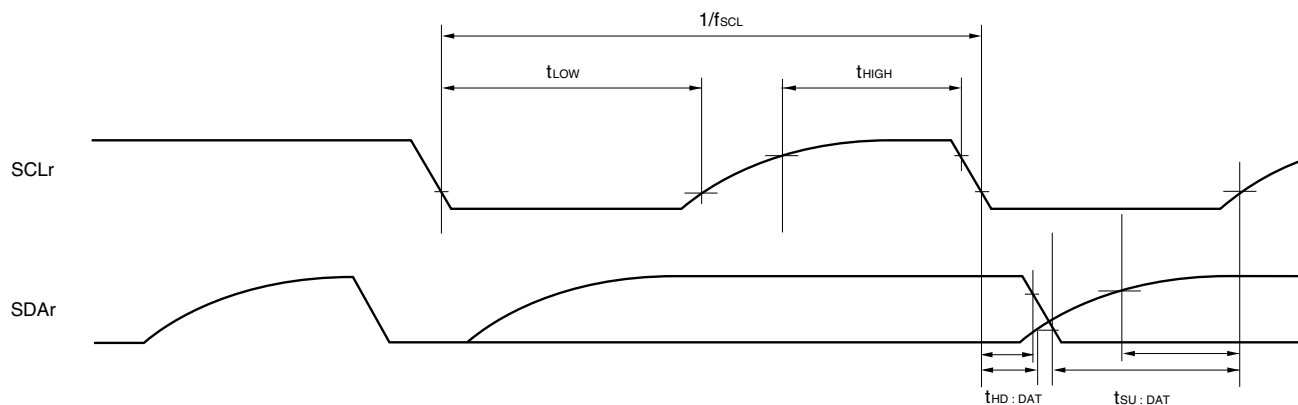
Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b [V]: Communication line voltage

    2. r: IIC Number (r = 00, 20)

    3. f_{MCK}: Serial array unit operation clock frequency

       (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

       m: Unit number (m = 0,1), n: Channel number (n = 0))

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV$_{REFP}$ Reference voltage (−) = AV$_{REFM}$	Reference voltage (+) = V$_{DD}$ Reference voltage (−) = V$_{SS}$	Reference voltage (+) = V$_{BGR}$ Reference voltage (−) = AV$_{REFM}$
ANI0 to ANI3	Refer to **29.6.1 (1)**.	Refer to **29.6.1 (3)**.	Refer to **29.6.1 (4)**.
ANI16 to ANI22	Refer to **29.6.1 (2)**.		
Internal reference voltage	Refer to **29.6.1 (1)**.		−
Temperature sensor output voltage			

(1) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage

(T$_A$ = −40 to +105°C, 2.4 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (−) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]			1.2	±3.5	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI2, ANI3	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]				±0.25	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]				±0.25	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]				±2.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]				±1.5	LSB
Analog input voltage	V$_{AIN}$	ANI2, ANI3		0		AV$_{REFP}$	V
		Internal reference voltage (HS (high-speed main) mode)			V$_{BGR}$[Note 4]		V
		Temperature sensor output voltage (HS (high-speed main) mode)			V$_{TMPS25}$[Note 4]		V

(**Notes** are listed on the next page.)

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.