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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10366asp-v5

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Code flash	Data flash	RAM	20 pins	24 pins	30 pins
16 KB	2 KB	2 KB	_	_	R5F102AA
	_		_	_	R5F103AA
	2 KB	1.5 KB	R5F1026A Note 1	R5F1027A ^{Note 1}	_
			R5F1036A Note 1	R5F1037A Note 1	_
12 KB	2KB	1 KB	R5F10269 Note 1	R5F10279 Note 1	R5F102A9
			R5F10369 Note 1	R5F10379 Note 1	R5F103A9
8 KB	2 KB	768 B	R5F10268 Note 1	R5F10278 Note 1	R5F102A8
			R5F10368 Note 1	R5F10378 Note 1	R5F103A8
4 KB	2KB	512 B	R5F10267	R5F10277	R5F102A7
	_		R5F10367	R5F10377	R5F103A7
2 KB	2 KB	256 B	R5F10266 Note 2		_
			R5F10366 Note 2		

O ROM, RAM capacities

Notes 1. This is 640 bytes when the self-programming function or data flash function is used. (For details, see CHAPTER 3 CPU ARCHITECTURE.)

2. The self-programming function cannot be used for R5F10266 and R5F10366.

Caution When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.



1.6 Block Diagram







1.6.2 24-pin products



Note Provided only in the R5F102 products.



1.6.3 30-pin products





Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR).



2.2 Oscillator Characteristics

2.2.1 X1 oscillator characteristics

$(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{V}_{DD} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{ V}_{SS} = 0 \text{ V})$

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation	Ceramic resonator /	$2.7~V \leq V_{\text{DD}} \leq 5.5~V$	1.0		20.0	MHz
frequency (fx) ^{Note}	crystal oscillator	$1.8~V \leq V_{\text{DD}} < 2.7~V$	1.0		8.0	

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

- Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.
- **Remark** When using the X1 oscillator, refer to **5.4 System Clock Oscillator**.

2.2.2 On-chip oscillator characteristics

$(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{ V}_{SS} = 0 \text{ V})$

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	fін			1		24	MHz
High-speed on-chip oscillator		R5F102 products	$T_A = -20 \text{ to } +85^{\circ}\text{C}$	-1.0		+1.0	%
clock frequency accuracy			$T_A = -40$ to $-20^{\circ}C$	-1.5		+1.5	%
		R5F103 products		-5.0		+5.0	%
Low-speed on-chip oscillator clock frequency	fı∟				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.



(TA = −40 to +85°C, 1	$1.8 V \le V$	$DD \leq 5.5 V, Vss = 0 V$					(2/4)
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	Iol1	20-, 24-pin products: Per pin for P00 to P03 ^{Note 4} , P10 to P14, P40 to P42				20.0 Note 2	mA
		30-pin products: Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147					
		Per pin for P60, P61				15.0 Note 2	mA
		20-, 24-pin products:	$4.0~V \leq V_{\text{DD}} \leq 5.5~V$			60.0	mA
		Total of P40 to P42	$2.7~V \leq V_{\text{DD}} < 4.0~V$			9.0	mA
		30-pin products: Total of P00, P01, P40, P120 (When duty $\leq 70\%^{\text{Note 3}}$)	$1.8~V \leq V_{\text{DD}} < 2.7~V$			1.8	mA
		20-, 24-pin products:	$4.0~V \leq V_{\text{DD}} \leq 5.5~V$			80.0	mA
		Total of P00 to P03 ^{Note 4} ,	$2.7~V \leq V_{\text{DD}} < 4.0~V$			27.0	mA
		30-pin products: Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147 (When duty \leq 70% ^{Note 3})	$1.8 \text{ V} \leq \text{V}_{\text{DD}} < 2.7 \text{ V}$			5.4	mA
		Total of all pins (When duty $\leq 70\%^{Note 3}$)				140	mA
	IOL2	Per pin for P20 to P23				0.4	mA
		Total of all pins				1.6	mA

(a (A)

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the Vss pin.

2. However, do not exceed the total current value.

3. The output current value under conditions where the duty factor \leq 70%.

If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

• Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where n = 80% and $I_{OL} = 10.0$ mA

Total output current of pins = $(10.0 \times 0.7)/(80 \times 0.01) \cong 8.7$ mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

- 4. 24-pin products only.
- Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



(T _A = −40 to +85°C,	1.8 V ≤ Vo	$d \leq 5.5 \text{ V}, \text{ Vss} = 0 \text{ V}$				(4/4)		
Parameter	Symbol		Conditic	ns	MIN.	TYP.	MAX.	Unit
Output voltage, low	V _{OL1}	20-, 24-pin product P00 to P03 ^{Note} , P10	s:) to P14,	$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL1}} = 20.0 \ mA \end{array} \label{eq:DD_eq}$			1.3	V
		P40 to P42 30-pin products: P0	00, P01,	$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL1}} = 8.5 \ mA \end{array} \end{array} \label{eq:DD}$			0.7	V
		P10 to P17, P30, F P50, P51, P120, P	P31, P40, 147	$\begin{array}{l} 2.7 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL1}} = 3.0 \ mA \end{array} \label{eq:DD}$			0.6	V
				$\begin{array}{l} 2.7 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL1}} = 1.5 \ mA \end{array} \end{array} \label{eq:DD}$			0.4	V
				$\label{eq:VDD} \begin{array}{l} 1.8 \mbox{ V} \leq \mbox{ V}_{\mbox{DD}} \leq 5.5 \mbox{ V}, \\ I_{\mbox{DL1}} = 0.6 \mbox{ mA} \end{array}$			0.4	V
	Vol2	P20 to P23		lol2 = 400 μA			0.4	V
	Vol3	P60, P61		$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL1}} = 15.0 \ mA \end{array} \end{array} \label{eq:VDD}$			2.0	V
				$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL1}} = 5.0 \ mA \end{array} \label{eq:DD}$			0.4	V
				$\begin{array}{l} 2.7 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL1}} = 3.0 \ mA \end{array} \label{eq:DD}$			0.4	V
				$\label{eq:VDD} \begin{array}{l} 1.8 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL1}} = 2.0 \ mA \end{array}$			0.4	V
Input leakage current, high	Ішні	Other than P121, P122	$V_{\text{I}} = V_{\text{DD}}$				1	μA
	Ілн2	P121, P122 (X1, X2/EXCLK)	VI = VDD	Input port or external clock input			1	μA
				When resonator connected			10	μA
Input leakage current, low	ILIL1	Other than P121, P122	VI = Vss				-1	μA
	ILIL2	P121, P122 (X1, X2/EXCLK)	VI = Vss	Input port or external clock input			-1	μA
				When resonator connected			-10	μA
On-chip pull-up resistance	Ru	20-, 24-pin product P00 to P03 ^{№™} , P10 P40 to P42, P125,	s:) to P14, RESET	VI = Vss, input port	10	20	100	kΩ
		30-pin products: P0 P10 to P17, P30, F P50, P51, P120, P	00, P01, P31, P40, 147					

$40 \text{ to } 185^{\circ}$ 18V < Vpp < 55 V Vcc -0 1/1

Note 24-pin products only.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



Minimum Instruction Execution Time during Main System Clock Operation



When the high-speed on-chip oscillator clock is selected During self programming When high-speed system clock is selected _ _ _

_ . _ .



TCY vs VDD (LS (low-speed main) mode)

When the high-speed on-chip oscillator clock is selected

--- During self programming ---. When high-speed system clock is selected



2.5 Peripheral Functions Characteristics

AC Timing Test Point



2.5.1 Serial array unit

LS (low-spee

(1) During communication at same potential (UART mode) ($T_A = -40$ to $+85^{\circ}$ C, 1.8 V \leq V_{DD} \leq 5.5 V, V_{SS} = 0 V)

Parameter	Symbol		Conditions	HS (hig main)	h-speed Mode	LS (low main)	/-speed Mode	Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate					fмск/6		fмск/6	bps
Note 1		Theoretical v fcLк = fмск ^{Note2}	alue of the maximum transfer rate		4.0		1.3	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (fcLk) are: HS (high-speed main) mode: 24 MHz (2.7 V \leq VDD \leq 5.5 V)

16 MHz (2.4 V
$$\leq$$
 VDD \leq 5.5 V)

d main) mode: 8 MHz (1.8 V
$$\leq$$
 VDD \leq 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

2. fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))



UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)





- **Remarks 1.** R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage
 - **2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)
 - fmck: Serial array unit operation clock frequency (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
 - m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))
 - **4.** UART0 of the 20- and 24-pin products supports communication at different potential only when the peripheral I/O redirection function is not used.



(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

Parameter	Symbol		Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t ксү1	$t_{KCY1} \geq 4/f_{CLK}$	$4.0~V \leq V_{\text{DD}} \leq 5.5~V,$	300		1150		ns
			$2.7~V \leq V_b \leq 4.0~V,$					
			C_b = 30 pF, R_b = 1.4 k Ω					
			$2.7~V \leq V_{\text{DD}} < 4.0~V,$	500		1150		ns
			$2.3~V \leq V_b \leq 2.7~V,$					
			C_b = 30 pF, R_b = 2.7 k Ω					
			$1.8~V \leq V_{\text{DD}} < 3.3~V,$	1150		1150		ns
			$1.6~V \leq V_{b} \leq 2.0~V^{\text{ Note}},$					
			C_b = 30 pF, R_b = 5.5 k Ω					
SCKp high-level width	tкнı	$4.0~V \leq V_{\text{DD}} \leq$	5.5 V, 2.7 V \leq V _b \leq 4.0 V,	tксү1/2-75		tксү1/2-75		ns
		$C_b = 30 \text{ pF}, \text{ F}$	lb = 1.4 kΩ					
		$2.7 \text{ V} \leq \text{V}_{\text{DD}}$ <	$4.0~V,~2.3~V \le V_b \le 2.7~V,~$	tксү1/2 –170		tксү1/2–170		ns
		$C_b = 30 \text{ pF}, \text{ R}$	$h_b = 2.7 \text{ k}\Omega$					
		$1.8 \text{ V} \leq \text{V}_{\text{DD}} <$	3.3 V, 1.6 V \leq V $_{b}$ \leq 2.0 V $^{\text{Note}},$	tксү1/2 –458		tксү1/2-458		ns
		$C_b = 30 \text{ pF}, \text{ F}$	$h_b = 5.5 \text{ k}\Omega$					
SCKp low-level width	tĸ∟1	$4.0~V \leq V_{\text{DD}} \leq$	$5.5~V,~2.7~V \le V_b \le 4.0~V,$	tксү1/2-12		tксү1/2–50		ns
		$C_{b} = 30 \text{ pF}, \text{ R}$	lb = 1.4 kΩ					
		$2.7 \text{ V} \leq \text{V}_{\text{DD}}$ <	$4.0~V,~2.3~V \le V_b \le 2.7~V,~$	tксү1/2 –18		tксү1/2–50		ns
		C _b = 30 pF, R	$h_b = 2.7 \text{ k}\Omega$					
		$1.8 \text{ V} \leq \text{V}_{\text{DD}} <$	$3.3 \text{ V}, \ 1.6 \text{ V} \le \text{V}_{b} \le 2.0 \text{ V}^{\text{Note}},$	tксү1/2 –50		tксү1/2–50		ns
		C _b = 30 pF, R	$h_b = 5.5 \text{ k}\Omega$					

 $(T_A = -40 \text{ to } +85^{\circ}C, 1.8 \text{ V} \le \text{V}_{DD} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{ V}_{SS} = 0 \text{ V})$

 $\label{eq:Note} \textbf{Note} \quad \textbf{Use it with } V_{\text{DD}} \geq V_{\text{b}}.$

- Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.
 - 2. CSI01 and CSI11 cannot communicate at different potential.
- **Remarks 1.** R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage
 - **2.** p: CSI number (p = 00, 20)



(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)

Parameter	Symbol	Conditions	HS (hig main)	h-speed Mode	LS (low main)	/-speed Mode	Unit
			MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) ^{Note 1}	tsıĸı	$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \ 2.7 \ V \leq V_b \leq 4.0 \ V, \\ C_b = 30 \ pF, \ R_b = 1.4 \ k\Omega \end{array}$	81		479		ns
		$\label{eq:VD} \begin{split} 2.7 \ V \leq V_{\text{DD}} < 4.0 \ V, \ 2.3 \ V \leq V_{b} \leq 2.7 \ V, \\ C_{b} = 30 \ pF, \ R_{b} = 2.7 \ k\Omega \end{split}$	177		479		ns
		$\label{eq:VDD} \begin{split} 1.8 \ V \leq V_{\text{DD}} < 3.3 \ V, \ 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 2}}, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{split}$	479		479		ns
SIp hold time (from SCKp↑) ^{Note 1}	tksii	$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \ 2.7 \ V \leq V_b \leq 4.0 \ V, \\ C_b = 30 \ pF, \ R_b = 1.4 \ k\Omega \end{array}$	19		19		ns
		$\label{eq:VD} \begin{array}{l} 2.7 \ V \leq V_{\text{DD}} < 4.0 \ V, \ 2.3 \ V \leq V_{b} \leq 2.7 \ V, \\ C_{b} = 30 \ pF, \ R_{b} = 2.7 \ k\Omega \end{array}$	19		19		ns
		$\label{eq:VDD} \begin{split} 1.8 \ V \leq V_{\text{DD}} < 3.3 \ V, \ 1.6 \ V \leq V_b \leq 2.0 \ V^{\text{Note 2}}, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{split}$	19		19		ns
Delay time from SCKp↓ to	tkso1	$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \ 2.7 \ V \leq V_b \leq 4.0 \ V, \\ C_b = 30 \ pF, \ R_b = 1.4 \ k\Omega \end{array}$		100		100	ns
SOp output Note 1		$\label{eq:VD} \begin{array}{l} 2.7 \ V \leq V_{\text{DD}} < 4.0 \ V, \ 2.3 \ V \leq V_{b} \leq 2.7 \ V, \\ C_{b} = 30 \ pF, \ R_{b} = 2.7 \ k\Omega \end{array}$		195		195	ns
		$\label{eq:VDD} \begin{array}{ c c c c c } \hline 1.8 \ V \leq V_{\text{DD}} < 3.3 \ V, \ 1.6 \ V \leq V_{b} \leq 2.0 \ V^{\text{Note 2}}, \\ \hline C_{b} = 30 \ pF, \ R_{b} = 5.5 \ k\Omega \end{array}$		483		483	ns

$(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{ V}_{SS} = 0 \text{ V})$

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. Use it with $V_{DD} \ge V_b$.

(Cautions and Remarks are listed on the next page.)



Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

- **2.** This value is indicated as a ratio (%FSR) to the full-scale value.
- 3. When AV_{REFP} < V_{DD}, the MAX. values are as follows. Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}. Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}. Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.
- 4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).
- 5. Refer to 28.6.2 Temperature sensor/internal reference voltage characteristics.
- (2) When reference voltage (+) = AVREFP/ANIO (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{AV}_{REFP} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{ V}_{SS} = 0 \text{ V}, \text{ Reference voltage (+)} = \text{AV}_{REFP}, \text{ Reference voltage (-)} = \text{AV}_{REFM} = 0 \text{ V})$

Parameter	Symbol	Conditio	ns	MIN.	TYP.	MAX.	Unit
Resolution	Res			8		10	bit
Overall error Note 1	AINL	10-bit resolution			1.2	±5.0	LSB
		$AV_{REFP} = V_{DD}^{Note 3}$			1.2	$\pm 8.5^{\text{Note 4}}$	LSB
Conversion time	t CONV	10-bit resolution	$3.6~V \leq V \text{DD} \leq 5.5~V$	2.125		39	μS
		Target ANI pin: ANI16 to ANI22	$2.7~V \leq V \text{DD} \leq 5.5~V$	3.1875		39	μS
			$1.8~V \leq V \text{DD} \leq 5.5~V$	17		39	μS
				57		95	μS
Zero-scale error Notes 1, 2	EZS	10-bit resolution				±0.35	%FSR
		$AV_{REFP} = V_{DD}^{Note 3}$				$\pm 0.60^{\text{Note 4}}$	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution				±0.35	%FSR
		$AV_{REFP} = V_{DD}^{Note 3}$				$\pm 0.60^{\text{Note 4}}$	%FSR
Integral linearity error Note 1	ILE	10-bit resolution				±3.5	LSB
		$AV_{REFP} = V_{DD}^{Note 3}$				$\pm 6.0^{\text{Note 4}}$	LSB
Differential linearity	DLE	10-bit resolution				±2.0	LSB
error Note 1		$AV_{REFP} = V_{DD}^{Note 3}$				±2.5 ^{Note 4}	LSB
Analog input voltage	VAIN	ANI16 to ANI22		0		AVREFP and VDD	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

- 2. This value is indicated as a ratio (%FSR) to the full-scale value.
- **3.** When AV_{REFP} \leq V_{DD}, the MAX. values are as follows. Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}. Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}. Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
- 4. When the conversion time is set to 57 μ s (min.) and 95 μ s (max.).



<R> 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

$(T_A = -40 \text{ to } +85^{\circ}\text{C}, \text{Vss} = 0 \text{ V})$						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 Note		5.5	V

<R> Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



2.8 Flash Memory Programming Characteristics

$(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.8 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}_{DD}$
--

<r></r>	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	System clock frequency	fclk		1		24	MHz
	Code flash memory rewritable times		Retained for 20 years	1,000			Times
	Notes 1, 2, 3		$T_A = 85^{\circ}C$				
	Data flash memory rewritable times		Retained for 1 year		1,000,000		
	Notes 1, 2, 3		T _A = 25°C				
			Retained for 5 years	100,000			
			T _A = 85°C				
			Retained for 20 years	10,000			
			T _A = 85°C				

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

- 2. When using flash memory programmer and Renesas Electronics self programming library
- 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.



Parameter	Symbol	Condition	s	MIN.	TYP.	MAX.	Unit
Input voltage, high	VIH1	Normal input buffer	0.8Vdd		Vdd	V	
		20-, 24-pin products: P00 to P0 P40 to P42					
		30-pin products: P00, P01, P1 P40, P50, P51, P120, P147	0 to P17, P30, P31,				
	VIH2	TTL input buffer	$4.0~V \leq V_{\text{DD}} \leq 5.5~V$	2.2		VDD	v
		20-, 24-pin products: P10, P11	$3.3~V \leq V_{\text{DD}} < 4.0~V$	2.0		VDD	V
		30-pin products: P01, P10, P11, P13 to P17	$2.4~V \leq V_{\text{DD}} < 3.3~V$	1.5		Vdd	V
	VIH3	Normal input buffer		0.7Vdd		Vdd	V
	Villa	P60 P61	0.71/00		6.0	V	
	VINE	P121 P122 P125 ^{Note 1} P137 F	0.81/pp		Voo	V	
Input voltage low	Vii 1	Normal input buffer	0.0100		0 2Vpp	v	
		20-, 24-pin products: P00 to P03 ^{Note 2} , P10 to P14, P40 to P42					
		30-pin products: P00, P01, P10 P40, P50, P51, P120, P147					
	VIL2	TTL input buffer	$4.0~V \leq V_{\text{DD}} \leq 5.5~V$	0		0.8	V
		20-, 24-pin products: P10, P11	$3.3~V \leq V_{\text{DD}} < 4.0~V$	0		0.5	V
		30-pin products: P01, P10, P11, P13 to P17	$2.4~V \leq V_{\text{DD}} < 3.3~V$	0		0.32	V
	VIL3	P20 to P23	0		0.3VDD	V	
	VIL4	P60, P61		0		0.3VDD	V
	VIL5	P121, P122, P125 ^{Note 1} , P137, I	EXCLK, RESET	0		0.2VDD	V
Output voltage, high	gh V _{OH1} 20-, 24-pin products: P00 to P03 ^{Note 2} , P10	20-, 24-pin products: P00 to P03 ^{Note 2} , P10 to P14,	$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OH1}} = -3.0 \ mA \end{array} \end{array} \label{eq:VDD}$	VDD-0.7			V
		P40 to P42 30-pin products:	$2.7 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V},$ Ioh1 = -2.0 mA	VDD-0.6			V
		P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	$\begin{array}{l} 2.4 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OH1}} = -1.5 \ mA \end{array}$	V _{DD} -0.5			V
	Vон2	P20 to P23	Іон2 = -100 <i>µ</i> А	VDD-0.5			V

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{V}_{SS} = 0 \text{ V})$

(3/4)

Notes 1. 20, 24-pin products only.

- **2.** 24-pin products only.
- CautionThe maximum value of VIH of pins P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-
pin products, and P00, P10 to P15, P17, and P50 for 30-pin products is VDD even in N-ch open-drain mode.High level is not output in the N-ch open-drain mode.
- Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



(2) 30-pin products

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{V}_{SS}$	s = 0 V)
---	----------

(T _A = -40 to	$\Lambda = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{ V}_{\text{SS}} = 0 \text{ V}$ (1/2)							(1/2)		
Parameter	Symbol			Conditions			MIN.	TYP.	MAX.	Unit
Supply	Idd1	Operating	HS (High-speed	$f_{H} = 24 \text{ MHz}^{Note 3}$	Basic	V _{DD} = 5.0 V		1.5		mA
current ^{Note 1}	current ^{Note 1} mode ma	main) mode ^{Note 4}	Note 4	operation	V _{DD} = 3.0 V		1.5			
				Normal	V _{DD} = 5.0 V		3.7	5.8	mA	
				operation	V _{DD} = 3.0 V		3.7	5.8		
				$f_{IH} = 16 \; MHz^{Note3}$		V _{DD} = 5.0 V		2.7	4.2	mA
				V _{DD} = 3.0 V		2.7	4.2			
			$\label{eq:masses} \begin{split} f_{\text{MX}} &= 20 \ \text{MHz}^{\text{Note 2}}, \\ V_{\text{DD}} &= 5.0 \ \text{V} \\ \\ \hline f_{\text{MX}} &= 20 \ \text{MHz}^{\text{Note 2}}, \end{split}$		Square wave input		3.0	4.9	mA	
					Resonator connection		3.2	5.0		
				$f_{MX} = 20 \text{ MHz}^{Note 2},$		Square wave input		3.0	4.9	mA
		$V_{DD} = 3.0 V$		Resonator connection		3.2	5.0			
		$f_{MX} = 10 \text{ MHz}^{Note 2},$		Square wave input		1.9	2.9	mA		
	Vo fmx	V _{DD} = 5.0 V		Resonator connection		1.9	2.9			
		$f_{MX} = 10 \text{ MHz}^{Note 2},$		Square wave input		1.9	2.9	mA		
				$V_{DD} = 3.0 V$		Resonator connection		1.9	2.9	

Notes 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or Vss. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

- 2. When high-speed on-chip oscillator clock is stopped.
- 3. When high-speed system clock is stopped
- 4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: VDD = 2.7 V to 5.5 V @1 MHz to 24 MHz VDD = 2.4 V to 5.5 V @1 MHz to 16 MHz

- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 - 2. fin: high-speed on-chip oscillator clock frequency
 - **3.** Temperature condition of the TYP. value is $T_A = 25^{\circ}C$.



Minimum Instruction Execution Time during Main System Clock Operation



AC Timing Test Point



External Main System Clock Timing





Rising reset release voltage

Falling interrupt voltage

MAX.

2.86

3.03

2.97

3.14

3.07

4.22

4.13

3.90

3.83

4.06

3.98

Unit

v

V

V

v

V

V

٧

LVD detection voltage of interrupt & reset mode

(T _A = -40 to +10	5°C, Vpd	$R \leq V D D$	$0 \le 5.5 \text{ V}, \text{ Vss} = 0 \text{ V}$				
Parameter	Symbol		Cond	itions	MIN.	TYP.	
Interrupt and reset	VLVDD0	VPOC2,	VPOC1, VPOC1 = 0, 1, 1, fall	ing reset voltage	2.64	2.75	
mode	VLVDD1		LVIS1, LVIS0 = 1, 0	Rising reset release voltage	2.81	2.92	
				Falling interrupt voltage	2.75	2.86	
	VLVDD2		LVIS1, LVIS0 = 0, 1	Rising reset release voltage	2.90	3.02	
				Falling interrupt voltage	2.85	2.96	

LVIS1, LVIS0 = 0, 0

3.6.5 Power supply voltage rising slope characteristics

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, \text{ Vss} = 0 \text{ V})$

VLVDD3

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 29.4 AC Characteristics.



<R>

4.3 30-pin products

R5F102AAASP, R5F102A9ASP, R5F102A8ASP, R5F102A7ASP R5F103AAASP, R5F103A9ASP, R5F103A8ASP, R5F103A7ASP R5F102AADSP, R5F102A9DSP, R5F102A8DSP, R5F102A7DSP R5F103AADSP, R5F103A9DSP, R5F103A8DSP, R5F103A7DSP R5F102AAGSP, R5F102A9GSP, R5F102A8GSP, R5F102A7GSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



NOTE

DI⊕

MM

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
А	9.85±0.15
В	0.45 MAX.
С	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
Е	0.1±0.05
F	1.3±0.1
G	1.2
Н	8.1±0.2
I	6.1±0.2
J	1.0±0.2
К	0.17±0.03
L	0.5
М	0.13
Ν	0.10
Р	3° ^{+5°} _3°
Т	0.25
U	0.6±0.15

J

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Revision History

RL78/G12 Data Sheet

			Description		
Rev.	Date	Page	Summary		
1.00	Dec 10, 2012	-	First Edition issued		
2.00	Sep 06, 2013	1	Modification of 1.1 Features		
			Modification of 1.2 List of Part Numbers		
		4	Modification of Table 1-1. List of Ordering Part Numbers, Note, and Caution		
		7 to 9	Modification of package name in 1.4.1 to 1.4.3		
		14	Modification of tables in 1.7 Outline of Functions		
		17	Modification of description of table in 2.1 Absolute Maximum Ratings (TA = 25° C)		
		18	Modification of table, Note, and Caution in 2.2.1 X1 oscillator characteristics		
		18	Modification of table in 2.2.2 On-chip oscillator characteristics		
		19	Modification of Note 3 in 2.3.1 Pin characteristics (1/4)		
		20	Modification of Note 3 in 2.3.1 Pin characteristics (2/4)		
		23	Modification of Notes 1 and 2 in (1) 20-, 24-pin products (1/2)		
		24	Modification of Notes 1 and 3 in (1) 20-, 24-pin products (2/2)		
		25	Modification of Notes 1 and 2 in (2) 30-pin products (1/2)		
		26	Modification of Notes 1 and 3 in (2) 30-pin products (2/2)		
		27	Modification of (3) Peripheral functions (Common to all products)		
		28	Modification of table in 2.4 AC Characteristics		
		29	Addition of Minimum Instruction Execution Time during Main System Clock Operation		
		30	Modification of figures of AC Timing Test Point and External Main System Clock Timing		
		31	Modification of figure of AC Timing Test Point		
		21	Modification of description and Note 2 in (1) During communication at same potential		
		51			
		20	Modification of description in (2) During communication at same potential (CSI mode)		
		00	Modification of description in (2) During communication at same potential (CSI mode)		
		33	Modification of description in (4) During communication at same potential (CSI mode)		
		00	Modification of table and Note 2 in (5) During communication at same potential (Combde)		
		30	(cimplified l^2 C mode)		
		00.00	(Simplified to Hode)		
		38, 39	$(1.8 \times 2.5 \times 2.1)$ (LAPT mode)		
		40	Modification of Romarko 1 to 2 in (6) Communication at different notantial (1.8.)		
		40	2.5 V 3 V) (LIART mode)		
		44	Modification of table in (7) Communication at different potential (2.5 V, 2.V) (CSI mode)		
		41	Modification of Courties in (7) Communication at different potential (2.5 V, 3 V) (CSI mode)		
		42	Medification of table in (0) Communication at different potential (2.5 V, 3 V) (CSI mode)		
		43	mode) (1/2)		
		4.4	Medification of table and Nates 1 and 0 in (0) Communication at different notantial (1.9		
		44	Nouncation of table and Notes 1 and 2 in (6) Communication at different potential (1.8 $V_{2} = V_{1} = 2 V_{1} = 2 V_{2}$		
			V, 2.5 V, 3 V) (CSI mode) (2/3)		
		45	(1.8.)(2.5.)(2.)) (CSL mode) (2(2)		
			$(1.8 \ V, 2.5 \ V, 3 \ V)$ (CSI mode) (3/3)		
		47	mode)		
			Medification of table. Note 1, and Ocution 1 in (10) Ocumentation of different at all		
		50	(1.8.) (2.5.) (2.1) (eimelified I ² C mode)		
			(1.0 v, 2.3 v, 3 v) (simplified 1.0 mode)		
		52	Noomication of Remark in 2.5.2 Serial Interface IICA		
		53	Addition of table to 2.6.1 A/D converter characteristics		
		53	Modification of description in 2.6.1 (1)		
		54	Modification of Notes 3 to 5 in 2.6.1 (1)		
		54	Modification of description and Notes 2 to 4 in 2.6.1 (2)		