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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

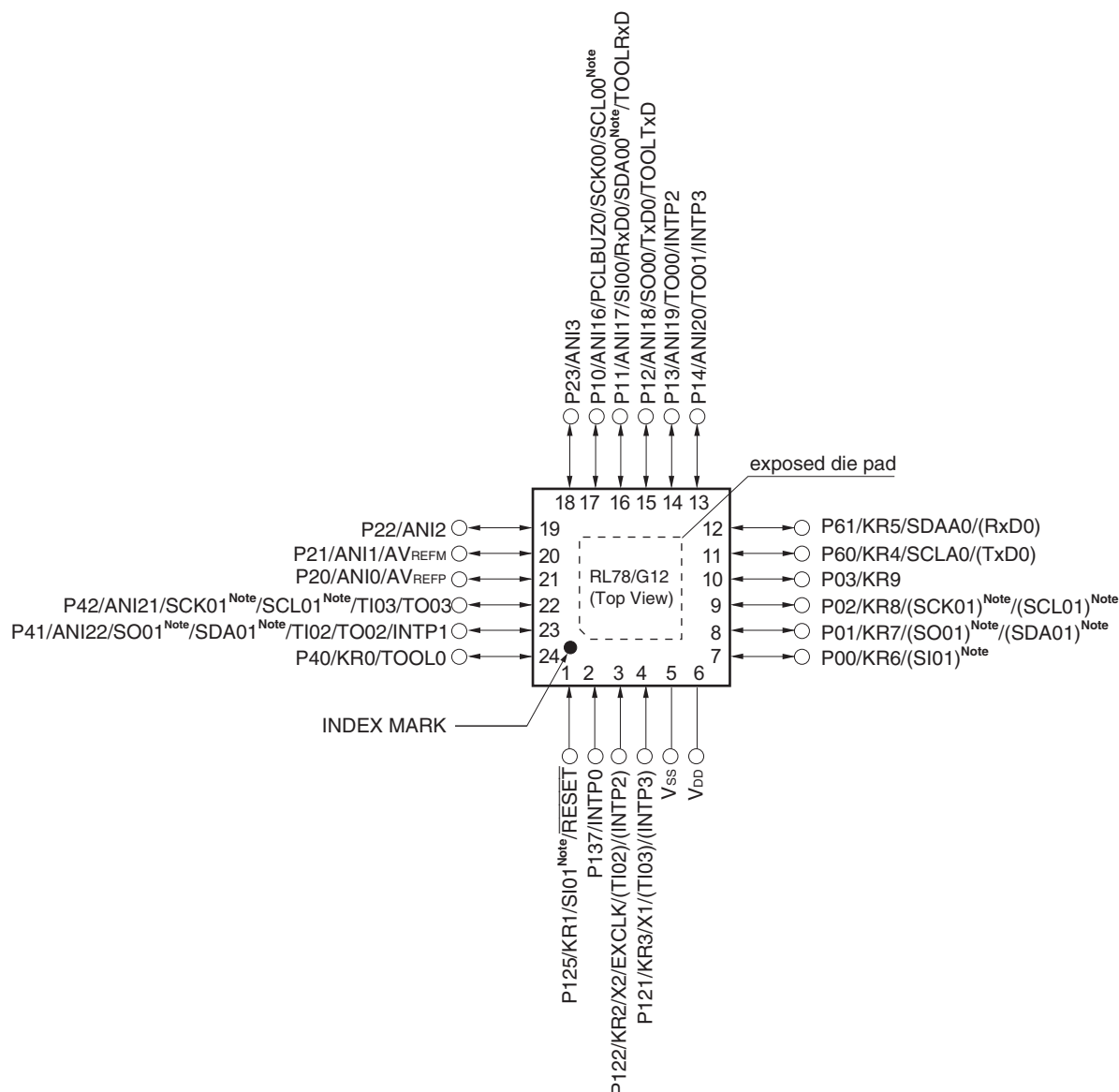
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10366dsp-v0

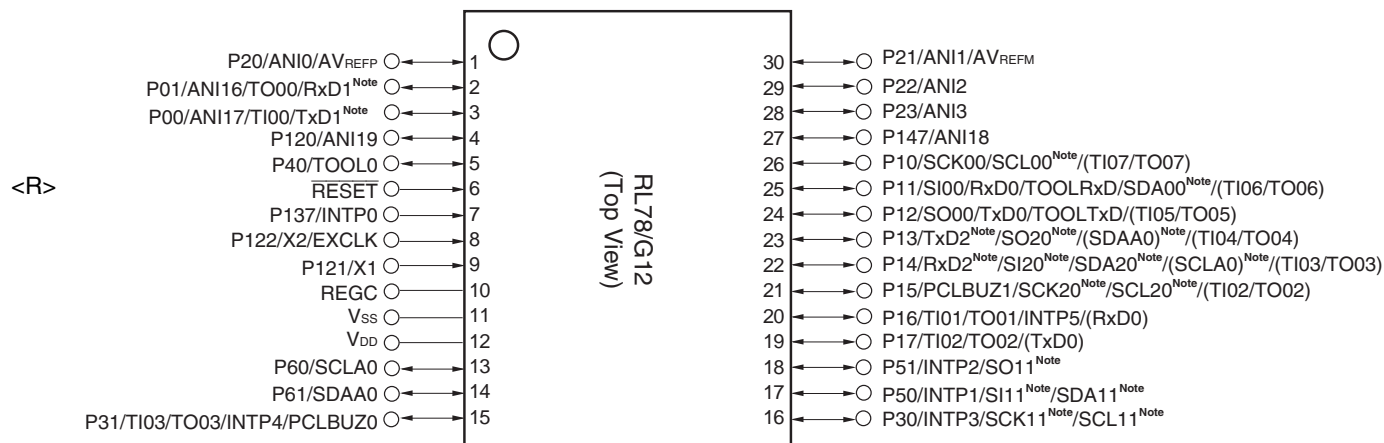
1.4.2 24-pin products

- <R> • 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)



1.4.3 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



Note Provided only in the R5F102 products.

Caution Connect the REGC pin to V_{SS} via capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.5 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V _{DD}			–0.5 to + 6.5	V
REGC terminal input voltage ^{Note 1}	V _{I REGC}	REGC		–0.3 to +2.8 and –0.3 to V _{DD} + 0.3 ^{Note 2}	V
Input Voltage	V _{I1}	Other than P60, P61		–0.3 to V _{DD} + 0.3 ^{Note 3}	V
	V _{I2}	P60, P61 (N-ch open drain)		–0.3 to 6.5	V
Output Voltage	V _O			–0.3 to V _{DD} + 0.3 ^{Note 3}	V
Analog input voltage	V _{AI}	20-, 24-pin products: ANI0 to ANI3, ANI16 to ANI22 30-pin products: ANI0 to ANI3, ANI16 to ANI19		–0.3 to V _{DD} + 0.3 and –0.3 to AVREF(+) + 0.3 ^{Notes 3, 4}	V
Output current, high	I _{OH1}	Per pin	Other than P20 to P23	–40	mA
		Total of all pins	All the terminals other than P20 to P23	–170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	–70	mA
			20-, 24-pin products: P00 to P03 ^{Note 5} , P10 to P14 30-pin products: P10 to P17, P30, P31, P50, P51, P147	–100	mA
	I _{OH2}	Per pin	P20 to P23	–0.5	mA
		Total of all pins		–2	mA
Output current, low	I _{OL1}	Per pin	Other than P20 to P23	40	mA
		Total of all pins	All the terminals other than P20 to P23	170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	70	mA
			20-, 24-pin products: P00 to P03 ^{Note 5} , P10 to P14, P60, P61 30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147	100	mA
	I _{OL2}	Per pin	P20 to P23	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T _A			–40 to +85	°C
Storage temperature	T _{stg}			–65 to +150	°C

Notes 1. 30-pin product only.

2. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.
3. Must be 6.5 V or lower.
4. Do not exceed AVREF(+) + 0.3 V in case of A/D conversion target pin.
5. 24-pin products only.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks** 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
2. AVREF(+) : + side reference voltage of the A/D converter.
 3. V_{SS} : Reference voltage

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

(1/4)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	20-, 24-pin products: Per pin for P00 to P03 ^{Note 4} , P10 to P14, P40 to P42 30-pin products: Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147			–10.0 ^{Note 2}	mA
		20-, 24-pin products: Total of P40 to P42	4.0 V ≤ V _{DD} ≤ 5.5 V		–30.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		–6.0	mA
		30-pin products: Total of P00, P01, P40, P120 (When duty ≤ 70% ^{Note 3})	1.8 V ≤ V _{DD} < 2.7 V		–4.5	mA
		20-, 24-pin products: Total of P00 to P03 ^{Note 4} , P10 to P14	4.0 V ≤ V _{DD} ≤ 5.5 V		–80.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		–18.0	mA
		30-pin products: Total of P10 to P17, P30, P31, P50, P51, P147 (When duty ≤ 70% ^{Note 3})	1.8 V ≤ V _{DD} < 2.7 V		–10.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})			–100	mA
	I _{OH2}	Per pin for P20 to P23			–0.1	mA
		Total of all pins			–0.4	mA

Notes 1. value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. The output current value under conditions where the duty factor ≤ 70%.

If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7) / (80 \times 0.01) \cong -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. 24-pin products only.

Caution P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**(2/4)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	20-, 24-pin products: Per pin for P00 to P03 ^{Note 4} , P10 to P14, P40 to P42			20.0 ^{Note 2}	mA
		30-pin products: Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147				
		Per pin for P60, P61			15.0 ^{Note 2}	mA
		20-, 24-pin products: Total of P40 to P42 30-pin products: Total of P00, P01, P40, P120 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		60.0	mA
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		9.0	mA
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		1.8	mA
		20-, 24-pin products: Total of P00 to P03 ^{Note 4} , P10 to P14, P60, P61 30-pin products: Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		80.0	mA
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		27.0	mA
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		5.4	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})			140	mA
	I _{OL2}	Per pin for P20 to P23			0.4	mA
		Total of all pins			1.6	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. The output current value under conditions where the duty factor $\leq 70\%$.

If duty factor $> 70\%$: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{OL} = 10.0\text{ mA}$

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. 24-pin products only.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(1) 20-, 24-pin products

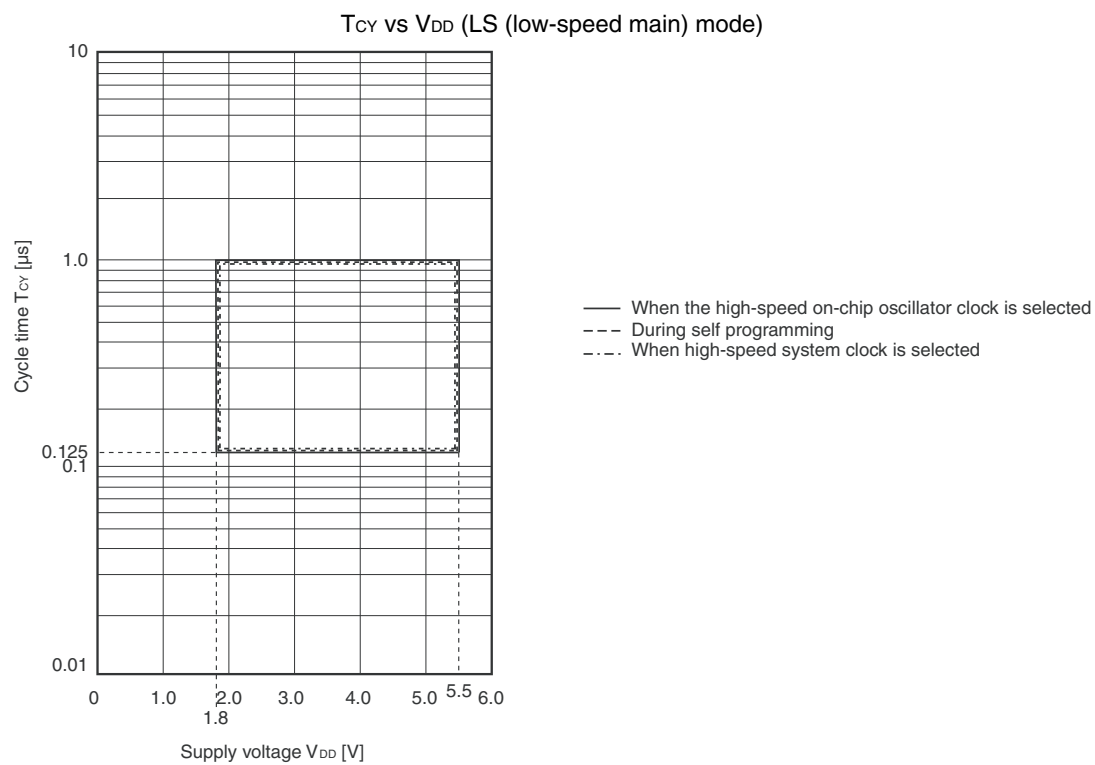
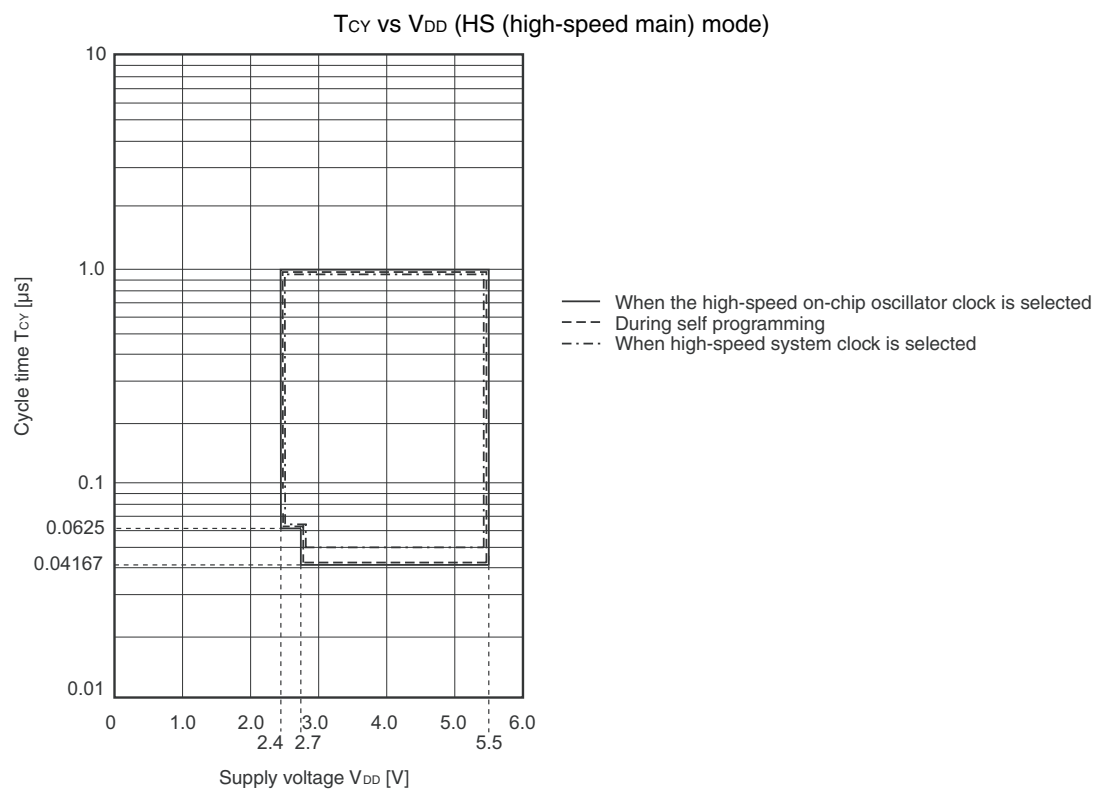
 $(T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	I _{DD2} ^{Note 2}	HALT mode	HS (High-speed main) mode ^{Note 6}	f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		440	1210	μA	
					V _{DD} = 3.0 V		440	1210		
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		400	950	μA	
					V _{DD} = 3.0 V		400	950		
			LS (Low-speed main) mode ^{Note 6}	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V		270	542	μA	
					V _{DD} = 2.0 V		270	542		
			HS (High-speed main) mode ^{Note 6}	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		280	1000	μA	
					Resonator connection		450	1170		
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		280	1000	μA	
					Resonator connection		450	1170		
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		190	590	μA	
					Resonator connection		260	660		
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		190	590	μA	
					Resonator connection		260	660		
			LS (Low-speed main) mode ^{Note 6}	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		110	360	μA	
					Resonator connection		150	416		
				f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input		110	360	μA	
					Resonator connection		150	416		
	I _{DD3} ^{Note 5}	STOP mode	T _A = −40°C					0.19	0.50	μA
			T _A = +25°C					0.24	0.50	
			T _A = +50°C					0.32	0.80	
			T _A = +70°C					0.48	1.20	
			T _A = +85°C					0.74	2.20	

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator clock is stopped.
 4. When high-speed system clock is stopped.
 5. Not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.
 HS(High speed main) mode: $V_{DD} = 2.7\text{ V}$ to 5.5 V @ 1 MHz to 24 MHz
 $V_{DD} = 2.4\text{ V}$ to 5.5 V @ 1 MHz to 16 MHz
 LS(Low speed main) mode: $V_{DD} = 1.8\text{ V}$ to 5.5 V @ 1 MHz to 8 MHz

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : high-speed on-chip oscillator clock frequency
 3. Except temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$, other than STOP mode

Minimum Instruction Execution Time during Main System Clock Operation

5. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 4** above to calculate the maximum transfer rate under conditions of the customer.

6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ and $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

8. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

9. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 8** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). **For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.**

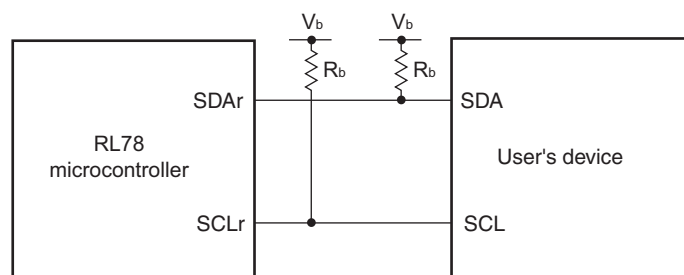
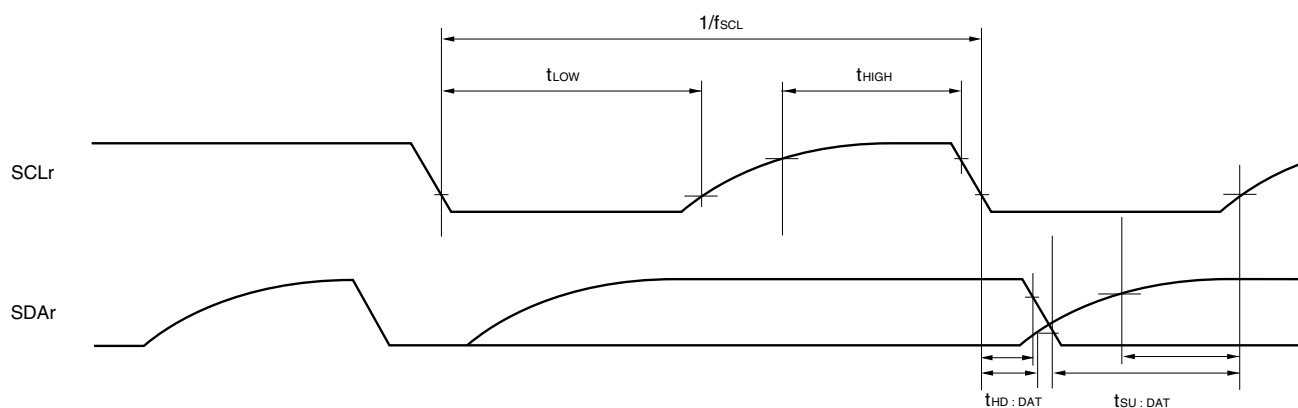
(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		400 ^{Note1}		300 ^{Note1}	kHz
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		400 ^{Note1}		300 ^{Note1}	kHz
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, ^{Note2} C _b = 100 pF, R _b = 5.5 kΩ		300 ^{Note1}		300 ^{Note1}	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1150		1550		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1150		1550		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, ^{Note2} C _b = 100 pF, R _b = 5.5 kΩ	1550		1550		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	675		610		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	600		610		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, ^{Note2} C _b = 100 pF, R _b = 5.5 kΩ	610		610		ns
Data setup time (reception)	t _{SU:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 190 ^{Note3}		1/f _{MCK} + 190 ^{Note3}		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 ^{Note3}		1/f _{MCK} + 190 ^{Note3}		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, ^{Note2} C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 ^{Note3}		1/f _{MCK} + 190 ^{Note3}		ns
Data hold time (transmission)	t _{HD:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	355	0	355	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	0	355	ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, ^{Note2} C _b = 100 pF, R _b = 5.5 kΩ	0	405	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.2. Use it with V_{DD} ≥ V_b.3. Set t_{SU:DAT} so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".**Cautions** 1. Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

2. IIC01 and IIC11 cannot communicate at different potential.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

- Remarks**
1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b [V]: Communication line voltage
 2. r : IIC Number ($r = 00, 20$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPS m) and the CKS mn bit of serial mode register mn (SMR mn).
 m : Unit number ($m = 0, 1$), n : Channel number ($n = 0$))
 4. Simplified I²C mode is supported only by the R5F102 products.

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution			1.2	± 7.0	LSB
					1.2	± 10.5 ^{Note 3}	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
				57		95	μs
Conversion time	t_{CONV}	10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZX	10-bit resolution				± 0.60	%FSR
						± 0.85 ^{Note 3}	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution				± 0.60	%FSR
						± 0.85 ^{Note 3}	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution				± 4.0	LSB
						± 6.5 ^{Note 3}	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution				± 2.0	LSB
						± 2.5 ^{Note 3}	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI3, ANI16 to ANI22		0		V_{DD}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} ^{Note 4}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TSP25} ^{Note 4}			V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV_{REFM} (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR}^{Note 3}, Reference voltage (-) = AV_{REFM}
^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8			bit
Conversion time	t _{CONV}	8-bit resolution	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	8-bit resolution			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution			±1.0	LSB
Analog input voltage	V _{AIN}		0		V _{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

2.9 Dedicated Flash Memory Programmer Communication (UART)

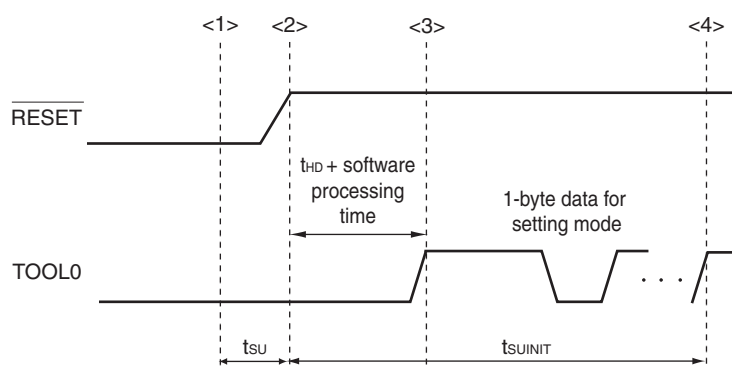
($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUNIT}	POR and LVD reset are released before external reset release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset are released before external reset release	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset are released before external reset release	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUNIT} : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

(1) 20-, 24-pin products

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V})$

(2/2)

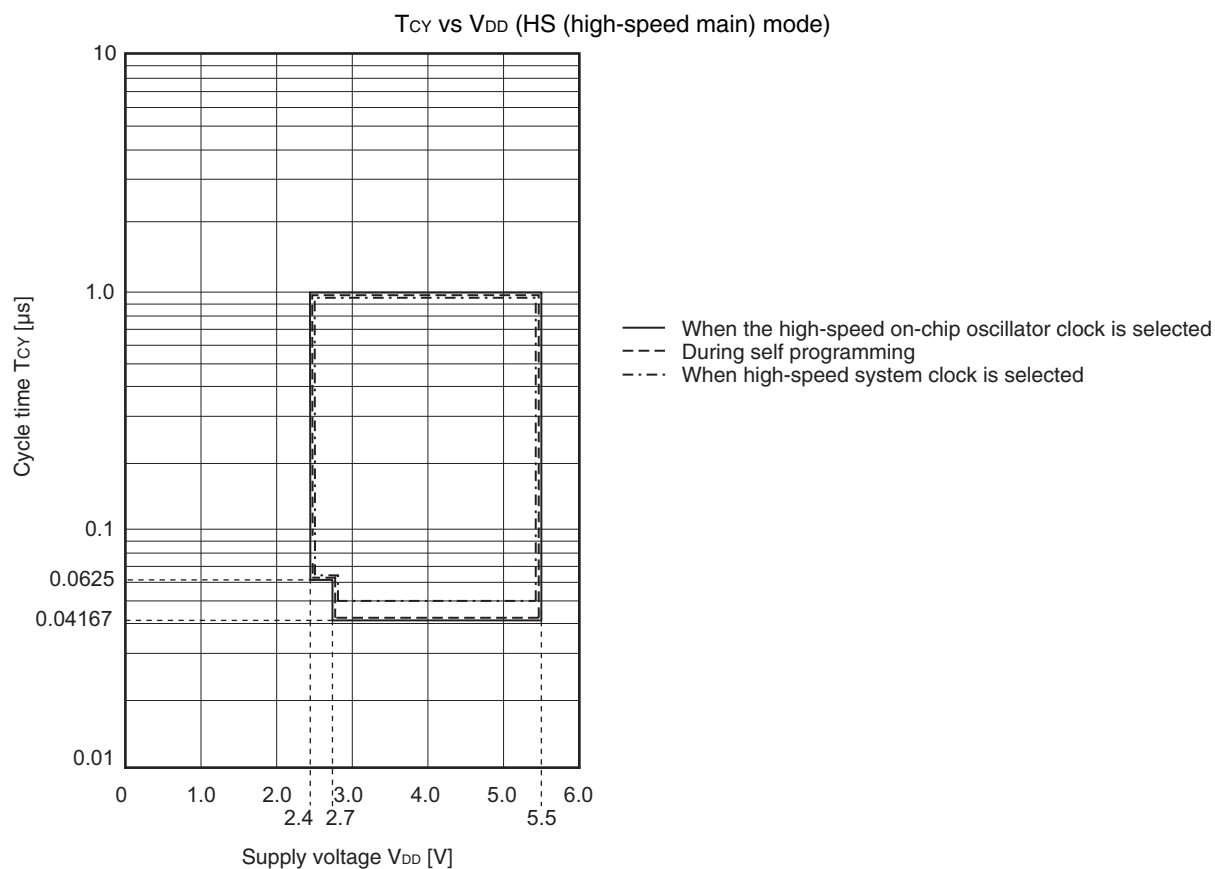
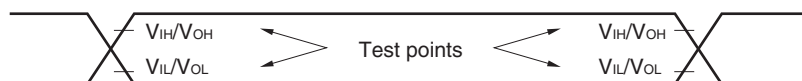
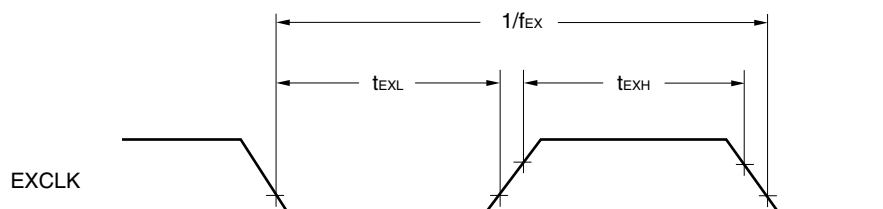
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	I _{DD2} ^{Note 2}	HALT mode	HS (High-speed main) mode ^{Note 6}	f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		440	2230	μA	
					V _{DD} = 3.0 V		440	2230		
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		400	1650	μA	
					V _{DD} = 3.0 V		400	1650		
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		280	1900	μA	
					Resonator connection		450	2000		
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		280	1900	μA	
					Resonator connection		450	2000		
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		190	1010	μA	
					Resonator connection		260	1090		
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		190	1010	μA	
					Resonator connection		260	1090		
	I _{DD3} ^{Note 5}	STOP mode	T _A = −40°C					0.19	0.50	μA
			T _A = +25°C					0.24	0.50	
T _A = +50°C					0.32	0.80				
T _A = +70°C					0.48	1.20				
T _A = +85°C					0.74	2.20				
T _A = +105°C					1.50	10.20				

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator clock is stopped.
 4. When high-speed system clock is stopped.
 5. Not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD} = 2.7\text{ V}$ to 5.5 V @ 1 MHz to 24 MHz

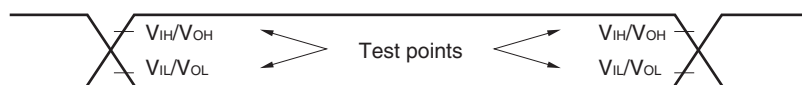
$V_{DD} = 2.4\text{ V}$ to 5.5 V @ 1 MHz to 16 MHz

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : high-speed on-chip oscillator clock frequency
 3. Except temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$, other than STOP mode

Minimum Instruction Execution Time during Main System Clock Operation**AC Timing Test Point****External Main System Clock Timing**

3.5 Peripheral Functions Characteristics

AC Timing Test Point



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

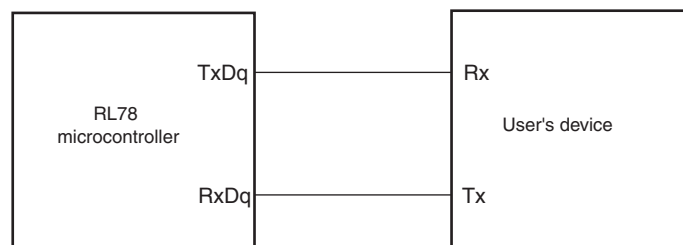
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate <small>Note 1</small>		Theoretical value of the maximum transfer rate $f_{CLK} = f_{MCK}$ <small>Note2</small>		$f_{MCK}/12$	bps
				2.0	Mbps

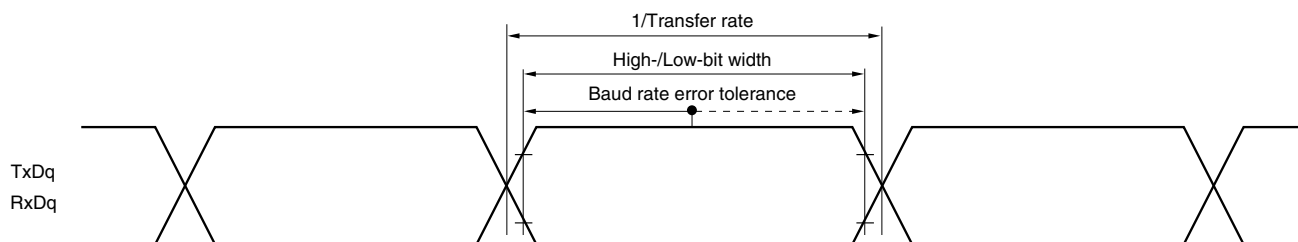
- Notes**
1. Transfer rate in the SNOOZE mode is 4800 bps only.
 2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
 HS (high-speed main) mode: 24 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)
 16 MHz ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

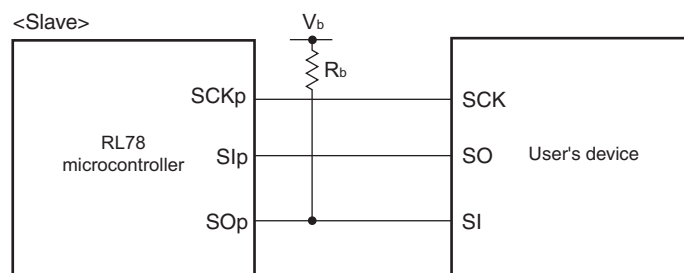
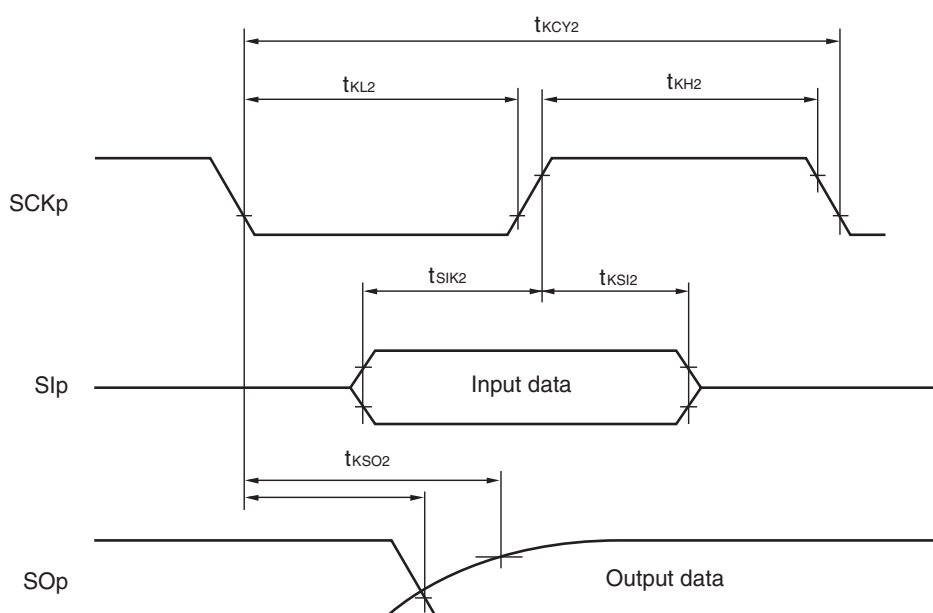
UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



- Remarks**
1. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)
 2. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

CSI mode connection diagram (during communication at different potential)
CSI mode serial transfer timing (slave mode) (during communication at different potential)
 (When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$.)


- Remarks**
1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage
 2. p : CSI number ($p = 00, 20$), m : Unit number ($m = 0, 1$), n : Channel number ($n = 0$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m ($SPSm$) and the $CKSmn$ bit of serial mode register mn ($SMRmn$))

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM} (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{BGR} ^{Note 3}, Reference voltage (–) = AV_{REFM}
^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8			bit
Conversion time	t_{CONV}	8-bit resolution	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	8-bit resolution			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution			± 2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution			± 1.0	LSB
Analog input voltage	V_{AIN}		0		V_{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (–) = AV_{REFM} .

Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

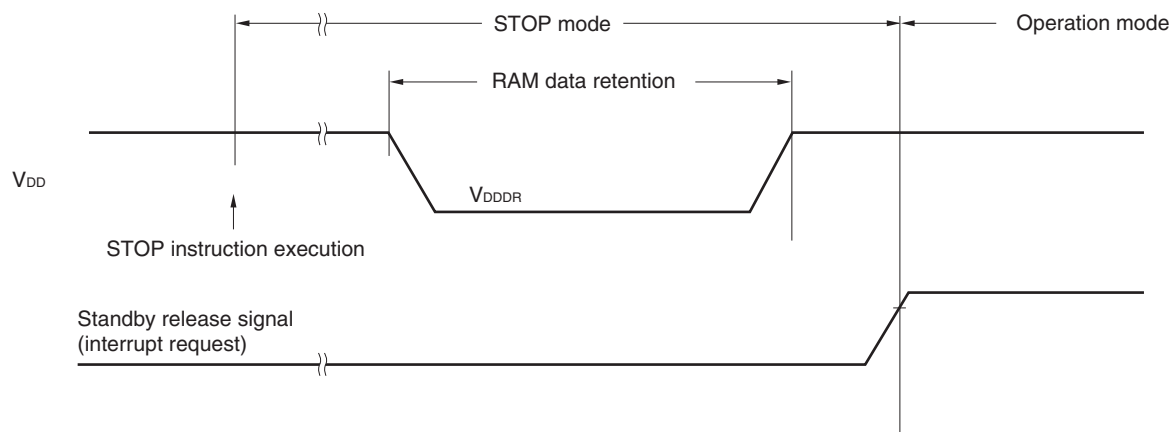
Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

<R> 3.7 RAM Data Retention Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 ^{Note}		5.5	V

<R> Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, 2.4 V $\leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		1		24	MHz
Code flash memory rewritable times <small>Notes 1, 2, 3</small>	C_{erwr}	Retained for 20 years $T_A = 85^\circ\text{C}$ <small>Notes 4</small>	1,000			Times
Data flash memory rewritable times <small>Notes 1, 2, 3</small>		Retained for 1 year $T_A = 25^\circ\text{C}$ <small>Notes 4</small>		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$ <small>Notes 4</small>	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$ <small>Notes 4</small>	10,000			

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library
 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
 4. This temperature is the average value at which data are retained.

NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.