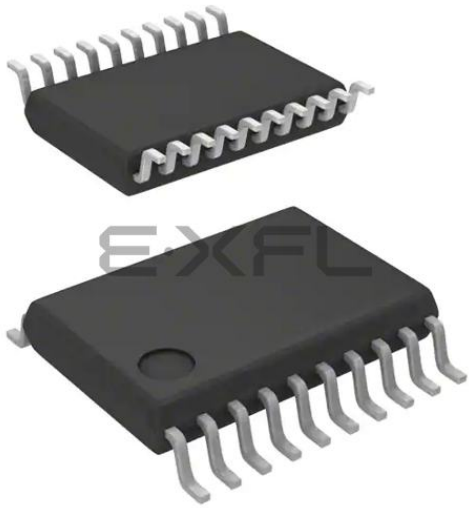


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CSI, I²C, UART/USART |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 14 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 11x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-LSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10367asp-v0 |

○ ROM, RAM capacities

| Code flash | Data flash | RAM | 20 pins | 24 pins | 30 pins |
|---|---|---|---|---|---|
| 16 KB | 2 KB | 2 KB | — | — | R5F102AA |
| | — | | — | — | R5F103AA |
| | 2 KB | 1.5 KB | R5F1026A Note 1 | R5F1027A Note 1 | — |
| | — | | R5F1036A Note 1 | R5F1037A Note 1 | — |
| 12 KB | 2KB | 1 KB | R5F10269 Note 1 | R5F10279 Note 1 | R5F102A9 |
| | — | | R5F10369 Note 1 | R5F10379 Note 1 | R5F103A9 |
| 8 KB | 2 KB | 768 B | R5F10268 Note 1 | R5F10278 Note 1 | R5F102A8 |
| | — | | R5F10368 Note 1 | R5F10378 Note 1 | R5F103A8 |
| 4 KB | 2KB | 512 B | R5F10267 | R5F10277 | R5F102A7 |
| | — | | R5F10367 | R5F10377 | R5F103A7 |
| 2 KB | 2 KB | 256 B | R5F10266 Note 2 | — | — |
| | — | | R5F10366 Note 2 | — | — |

**Notes 1.** This is 640 bytes when the self-programming function or data flash function is used. (For details, see **CHAPTER 3 CPU ARCHITECTURE**.)

**2.** The self-programming function cannot be used for R5F10266 and R5F10366.

**Caution** When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

**Table 1-1. List of Ordering Part Numbers**

| Pin count | Package | Data flash | Fields of Application | Part Number |
|---|---|---|---|---|
| <R> 20 pins | 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch) | Mounted | A | R5F1026AASP#V5, R5F10269ASP#V5, R5F10268ASP#V5, R5F10267ASP#V5, R5F10266ASP#V5<br>R5F1026AASP#X5, R5F10269ASP#X5, R5F10268ASP#X5, R5F10267ASP#X5, R5F10266ASP#X5 |
| | | | D | R5F1026ADSP#V5, R5F10269DSP#V5, R5F10268DSP#V5, R5F10267DSP#V5, R5F10266DSP#V5<br>R5F1026ADSP#X5, R5F10269DSP#X5, R5F10268DSP#X5, R5F10267DSP#X5, R5F10266DSP#X5 |
| | | | G | R5F1026AGSP#V5, R5F10269GSP#V5, R5F10268GSP#V5, R5F10267GSP#V5, R5F10266GSP#V5<br>R5F1026AGSP#X5, R5F10269GSP#X5, R5F10268GSP#X5, R5F10267GSP#X5, R5F10266GSP#X5 |
| | | Not mounted | A | R5F1036AASP#V5, R5F10369ASP#V5, R5F10368ASP#V5, R5F10367ASP#V5, R5F10366ASP#V5<br>R5F1036AASP#X5, R5F10369ASP#X5, R5F10368ASP#X5, R5F10367ASP#X5, R5F10366ASP#X5 |
| | | | D | R5F1036ADSP#V5, R5F10369DSP#V5, R5F10368DSP#V5, R5F10367DSP#V5, R5F10366DSP#V5<br>R5F1036ADSP#X5, R5F10369DSP#X5, R5F10368DSP#X5, R5F10367DSP#X5, R5F10366DSP#X5 |
| <R> 24 pins | 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch) | Mounted | A | R5F1027AANA#U5, R5F10279ANA#U5, R5F10278ANA#U5, R5F10277ANA#U5<br>R5F1027AANA#W5, R5F10279ANA#W5, R5F10278ANA#W5, R5F10277ANA#W5 |
| | | | D | R5F1027ADNA#U5, R5F10279DNA#U5, R5F10278DNA#U5, R5F10277DNA#U5<br>R5F1027ADNA#W5, R5F10279DNA#W5, R5F10278DNA#W5, R5F10277DNA#W5 |
| | | | G | R5F1027AGNA#U5, R5F10279GNA#U5, R5F10278GNA#U5, R5F10277GNA#U5<br>R5F1027AGNA#W5, R5F10279GNA#W5, R5F10278GNA#W5, R5F10277GNA#W5 |
| | | Not mounted | A | R5F1037AANA#V5, R5F10379ANA#V5, R5F10378ANA#V5, R5F10377ANA#V5<br>R5F1037AANA#X5, R5F10379ANA#X5, R5F10378ANA#X5, R5F10377ANA#X5 |
| | | | D | R5F1037ADNA#V5, R5F10379DNA#V5, R5F10378DNA#V5, R5F10377DNA#V5<br>R5F1037ADNA#X5, R5F10379DNA#X5, R5F10378DNA#X5, R5F10377DNA#X5 |
| 30 pins | 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch ) | Mounted | A | R5F102AAASP#V0, R5F102A9ASP#V0, R5F102A8ASP#V0, R5F102A7ASP#V0<br>R5F102AAASP#X0, R5F102A9ASP#X0, R5F102A8ASP#X0, R5F102A7ASP#X0 |
| | | | D | R5F102AADSP#V0, R5F102A9DSP#V0, R5F102A8DSP#V0, R5F102A7DSP#V0<br>R5F102AADSP#X0, R5F102A9DSP#X0, R5F102A8DSP#X0, R5F102A7DSP#X0 |
| | | | G | R5F102AAGSP#V0, R5F102A9GSP#V0, R5F102A8GSP#V0, R5F102A7GSP#V0<br>R5F102AAGSP#X0, R5F102A9GSP#X0, R5F102A8GSP#X0, R5F102A7GSP#X0 |
| | | Not mounted | A | R5F103AAASP#V0, R5F103A9ASP#V0, R5F103A8ASP#V0, R5F103A7ASP#V0<br>R5F103AAASP#X0, R5F103A9ASP#X0, R5F103A8ASP#X0, R5F103A7ASP#X0 |
| | | | D | R5F103AADSP#V0, R5F103A9DSP#V0, R5F103A8DSP#V0, R5F103A7DSP#V0<br>R5F103AADSP#X0, R5F103A9DSP#X0, R5F103A8DSP#X0, R5F103A7DSP#X0 |

**Note** For fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G12**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

## 2.4 AC Characteristics

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (High-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.04167 | | 1 | μs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | μs |
| | | | LS (Low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | μs |
| | | During self programming | HS (High-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.04167 | | 1 | μs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | μs |
| | | | LS (Low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | μs |
| External main system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 1.0 | | 8.0 | MHz |
| External main system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 30 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 60 | | | ns |
| TI00 to TI07 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 | | | ns |
| TO00 to TO07 output frequency | $f_{TO}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | | | 12 | MHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | | | 8 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | | | 4 | MHz |
| PCLBUZ0, or PCLBUZ1 output frequency | $f_{PCL}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | | | 16 | MHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | | | 8 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | | | 4 | MHz |
| INTP0 to INTP5 input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | | | | 1 | | | μs |
| KR0 to KR9 input available width | $t_{KR}$ | | | | 250 | | | ns |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | | 10 | | | μs |

**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

### (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note4 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 500 | | 6/$f_{MCK}$ and 500 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | 6/$f_{MCK}$ and 750 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2−7 | | $t_{KCY2}$/2−7 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2−8 | | $t_{KCY2}$/2−8 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2−18 | | $t_{KCY2}$/2−18 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | $t_{KCY2}$/2−18 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note4 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 44 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 75 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | 2/$f_{MCK}$ + 110 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

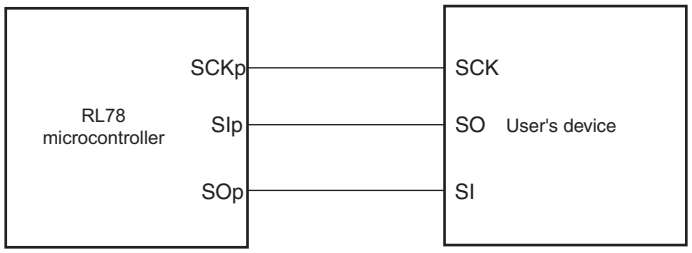
**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SOp output lines.

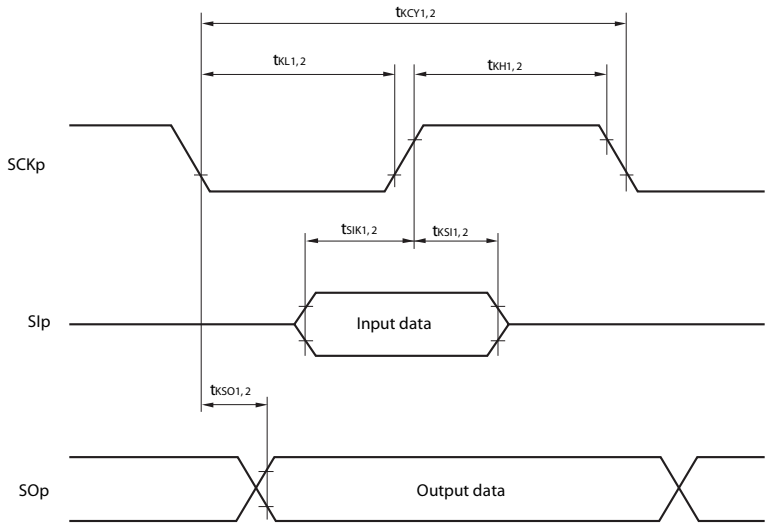
**5.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Caution** Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

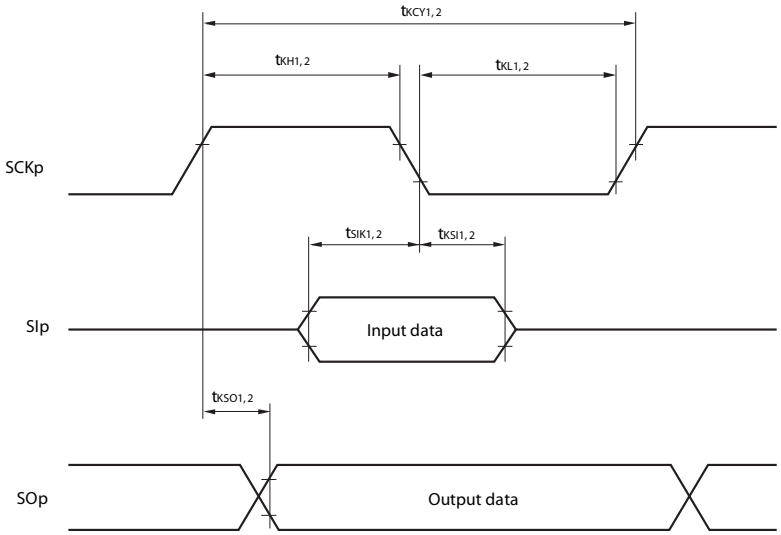
**CSI mode connection diagram (during communication at same potential)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




(**Remarks** are listed on the next page.)

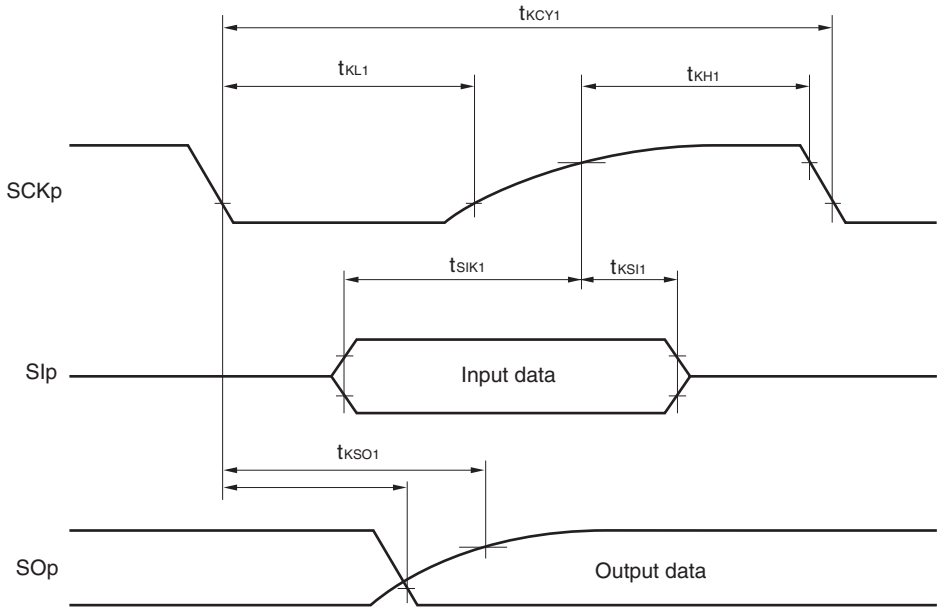
**(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

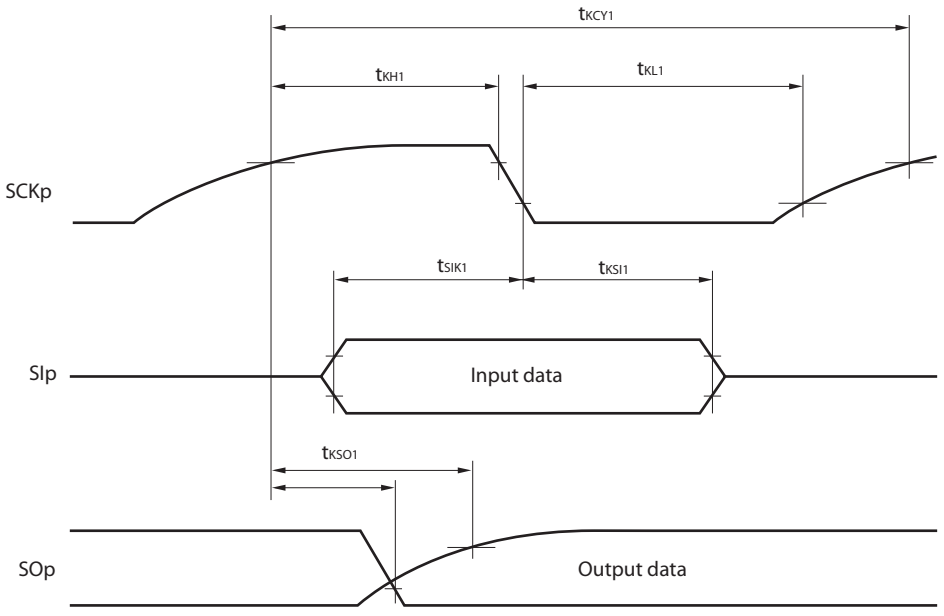
| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCK00 cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 2/f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 200 | | 1150 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 300 | | 1150 | | ns |
| SCK00 high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2– 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 120 | | $t_{KCY1}$/2 – 120 | | ns |
| SCK00 low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 7 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 10 | | $t_{KCY1}$/2 – 50 | | ns |
| SI00 setup time (to SCK00↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 58 | | 479 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 121 | | 479 | | ns |
| SI00 hold time (from SCK00↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | ns |
| Delay time from SCK00↓ to SO00 output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 60 | | 60 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 130 | | 130 | ns |
| SI00 setup time (to SCK00↓) Note 2 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 23 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 33 | | 110 | | ns |
| SI00 hold time (from SCK00↓) Note 2 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | ns |
| Delay time from SCK00↑ to SO00 output Note 2 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 10 | | 10 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 10 | | 10 | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



**(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 12/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 10/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 − 12 | | $t_{KCY2}$/2 − 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 − 18 | | $t_{KCY2}$/2 − 50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | $t_{KCY2}$/2 − 50 | | $t_{KCY2}$/2 − 50 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_{DD}$ ≤ 4.0 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_{DD}$ ≤ 2.0 V Note 2 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 5 | $t_{KSO2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 120 | | 2/$f_{MCK}$ + 573 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

**Notes 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**2.** Use it with $V_{DD} \geq V_b$.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Cautions 1.** Select the TTL input buffer for the SIp and SCKp pins and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**2.** CSI01 and CSI11 cannot communicate at different potential.

## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | | |
|---|---|---|---|
| | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (–) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$<br>Reference voltage (–) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$<br>Reference voltage (–) = $AV_{REFM}$ |
| ANI0 to ANI3 | Refer to **28.6.1 (1)**. | Refer to **28.6.1 (3)**. | Refer to **28.6.1 (4)**. |
| ANI16 to ANI22 | Refer to **28.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **28.6.1 (1)**. | | – |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | 1.2 | ±3.5 | LSB |
| | | | | | 1.2 | ±7.0 [Note 4] | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI2, ANI3 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | | | 57 | | 95 | μs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage<br>(HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error[Notes 1, 2] | EZS | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | | ±0.25 | %FSR |
| | | | | | | ±0.50 [Note 4] | %FSR |
| Full-scale error[Notes 1, 2] | EFS | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | | ±0.25 | %FSR |
| | | | | | | ±0.50 [Note 4] | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | | ±2.5 | LSB |
| | | | | | | ±5.0 [Note 4] | LSB |
| Differential linearity error [Note 1] | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | | ±1.5 | LSB |
| | | | | | | ±2.0 [Note 4] | LSB |
| Analog input voltage | $V_{AIN}$ | ANI2, ANI3 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ [Note 5] | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ [Note 5] | | | V |

(**Notes** are listed on the next page.)

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

**4.** Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

**5.** Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | 1.2 | ±5.0 | LSB |
| | | | | | 1.2 | ±8.5 Note 4 | LSB |
| Conversion time | tCONV | 10-bit resolution<br>Target ANI pin: ANI16 to ANI22 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | | | 57 | | 95 | μs |
| Zero-scale error Notes 1, 2 | EZS | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±0.35 | %FSR |
| | | | | | | ±0.60 Note 4 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±0.35 | %FSR |
| | | | | | | ±0.60 Note 4 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±3.5 | LSB |
| | | | | | | ±6.0 Note 4 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±2.0 | LSB |
| | | | | | | ±2.5 Note 4 | LSB |
| Analog input voltage | VAIN | ANI16 to ANI22 | | 0 | | $AV_{REFP}$ and $V_{DD}$ | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

**4.** When the conversion time is set to 57 μs (min.) and 95 μs (max.).

### 2.6.2 Temperature sensor/internal reference voltage characteristics

**($T_A$ = –40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, HS (high-speed main) mode**

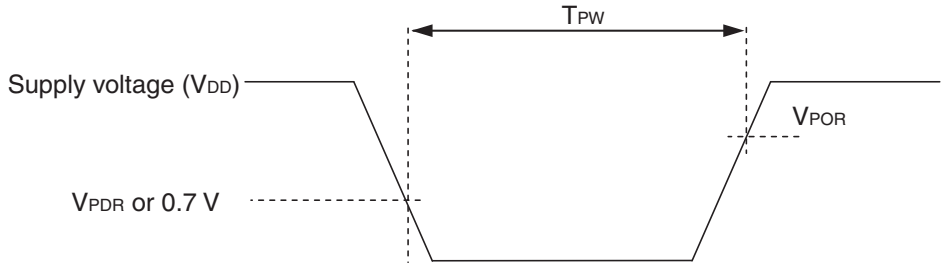
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.50 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor output voltage that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 2.6.3 POR circuit characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Power supply rise time | 1.47 | 1.51 | 1.55 | V |
| | $V_{PDR}$ | Power supply fall time | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width Note | $T_{PW}$ | | 300 | | | μs |

**Note** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).

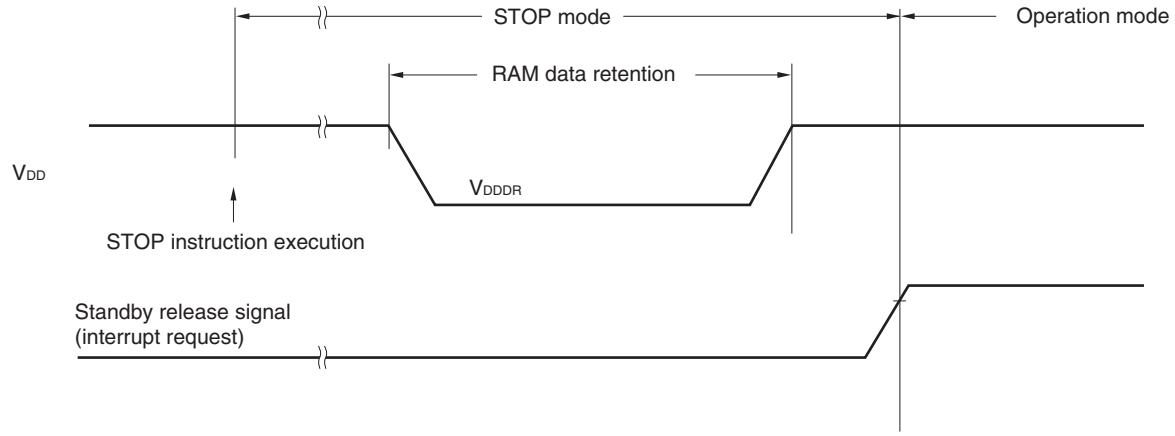


## <R> 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

**($T_A$ = −40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.46 Note | | 5.5 | V |

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.




## 2.8 Flash Memory Programming Characteristics

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

<R>

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| System clock frequency | $f_{CLK}$ | | 1 | | 24 | MHz |
| Code flash memory rewritable times Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years $T_A$ = 85°C | 1,000 | | | Times |
| Data flash memory rewritable times Notes 1, 2, 3 | | Retained for 1 year $T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years $T_A$ = 85°C | 100,000 | | | |
| | | Retained for 20 years $T_A$ = 85°C | 10,000 | | | |

**Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**2.** When using flash memory programmer and Renesas Electronics self programming library

**3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 3.1 Absolute Maximum Ratings

**Absolute Maximum Ratings ($T_A$ = 25°C)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | | −0.5 to + 6.5 | V |
| REGC terminal input voltage[Note1] | $V_{IREGC}$ | REGC | | −0.3 to +2.8 and −0.3 to $V_{DD}$ + 0.3 [Note 2] | V |
| Input Voltage | $V_{I1}$ | Other than P60, P61 | | −0.3 to $V_{DD}$ + 0.3[Note 3] | V |
| | $V_{I2}$ | P60, P61 (N-ch open drain) | | −0.3 to 6.5 | V |
| Output Voltage | $V_O$ | | | −0.3 to $V_{DD}$ + 0.3[Note 3] | V |
| Analog input voltage | $V_{AI}$ | 20, 24-pin products: ANI0 to ANI3, ANI16 to ANI22<br>30-pin products: ANI0 to ANI3, ANI16 to ANI19 | | −0.3 to $V_{DD}$ + 0.3 and −0.3 to AVREF(+)+0.3 [Notes 3, 4] | V |
| Output current, high | $I_{OH1}$ | Per pin | Other than P20 to P23 | −40 | mA |
| | | Total of all pins | All the terminals other than P20 to P23 | −170 | mA |
| | | | 20-, 24-pin products: P40 to P42<br>30-pin products: P00, P01, P40, P120 | −70 | mA |
| | | | 20-, 24-pin products: P00 to P03[Note 5], P10 to P14<br>30-pin products: P10 to P17, P30, P31, P50, P51, P147 | −100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P23 | −0.5 | mA |
| | | Total of all pins | | −2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | Other than P20 to P23 | 40 | mA |
| | | Total of all pins | All the terminals other than P20 to P23 | 170 | mA |
| | | | 20-, 24-pin products: P40 to P42<br>30-pin products: P00, P01, P40, P120 | 70 | mA |
| | | | 20-, 24-pin products: P00 to P03 [Note 5], P10 to P14, P60, P61<br>30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P23 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | | | −40 to +105 | °C |
| Storage temperature | $T_{stg}$ | | | −65 to +150 | °C |

**Notes 1.** 30-pin product only.

**2.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.

**3.** Must be 6.5 V or lower.

**4.** Do not exceed $AV_{REF}(+)$ + 0.3 V in case of A/D conversion target pin.

**5.** 24-pin products only.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** $AV_{REF}(+)$ : + side reference voltage of the A/D converter.

**3.** $V_{SS}$ : Reference voltage

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (3/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | Normal input buffer<br>20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | TTL input buffer<br>20-, 24-pin products: P10, P11<br>30-pin products: P01, P10, P11, P13 to P17 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 2.2 | | $V_{DD}$ | V |
| | | | 3.3 V ≤ $V_{DD}$ < 4.0 V | 2.0 | | $V_{DD}$ | V |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V | 1.5 | | $V_{DD}$ | V |
| | $V_{IH3}$ | Normal input buffer<br>P20 to P23 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60, P61 | | 0.7$V_{DD}$ | | 6.0 | V |
| | $V_{IH5}$ | P121, P122, P125[Note 1], P137, EXCLK, $\overline{\text{RESET}}$ | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | Normal input buffer<br>20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | 0 | | 0.2$V_{DD}$ | V |
| | $V_{IL2}$ | TTL input buffer<br>20-, 24-pin products: P10, P11<br>30-pin products: P01, P10, P11, P13 to P17 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | 3.3 V ≤ $V_{DD}$ < 4.0 V | 0 | | 0.5 | V |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P23 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL4}$ | P60, P61 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL5}$ | P121, P122, P125[Note 1], P137, EXCLK, $\overline{\text{RESET}}$ | | 0 | | 0.2$V_{DD}$ | V |
| Output voltage, high | $V_{OH1}$ | 20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –3.0 mA | $V_{DD}$–0.7 | | | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –2.0 mA | $V_{DD}$–0.6 | | | V |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –1.5 mA | $V_{DD}$–0.5 | | | V |
| | $V_{OH2}$ | P20 to P23 | $I_{OH2}$ = –100 μA | $V_{DD}$–0.5 | | | V |

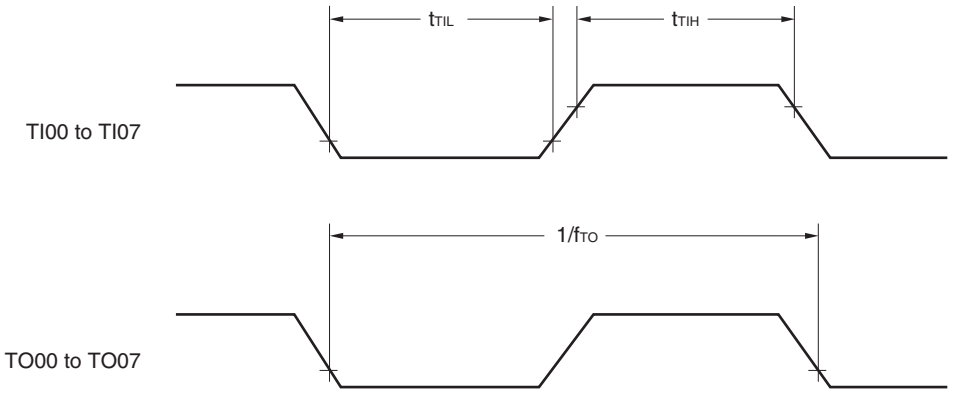
**Notes 1.** 20, 24-pin products only.

**2.** 24-pin products only.

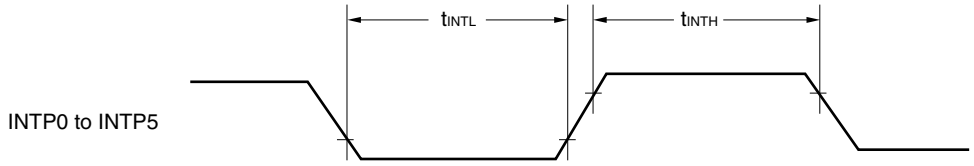
**Caution** The maximum value of $V_{IH}$ of pins P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products is $V_{DD}$ even in N-ch open-drain mode. High level is not output in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

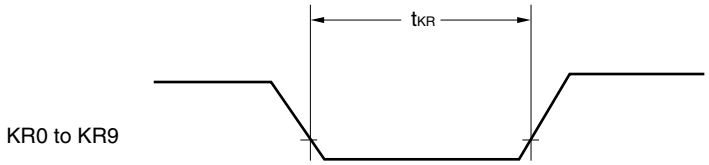
**TI/TO Timing**



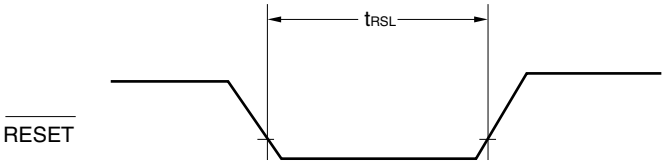

**Interrupt Request Input Timing**




**Key Interrupt Input Timing**




**$\overline{\text{RESET}}$ Input Timing**



**(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 24/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 20/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 32/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 28/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 24/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 72/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 64/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 52/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 32/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 20/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 – 24 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 – 36 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $t_{KCY2}$/2 – 100 | | ns |
| SIp setup time (to SCKp↑) Note 2 | $t_{SIK2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_{DD}$ ≤ 4.0 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_{DD}$ ≤ 2.0 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 240 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 1146 | ns |

**Notes 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

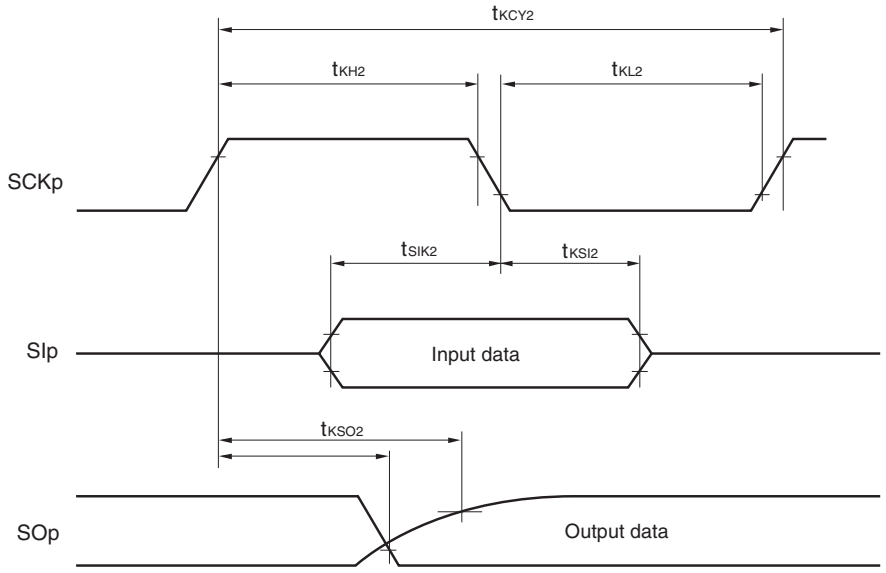
**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Cautions 1.** Select the TTL input buffer for the SIp and SCKp pins and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**2.** CSI01 and CSI11 cannot communicate at different potential.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

### 3.6.2 Temperature sensor/internal reference voltage characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, HS (high-speed main) mode**

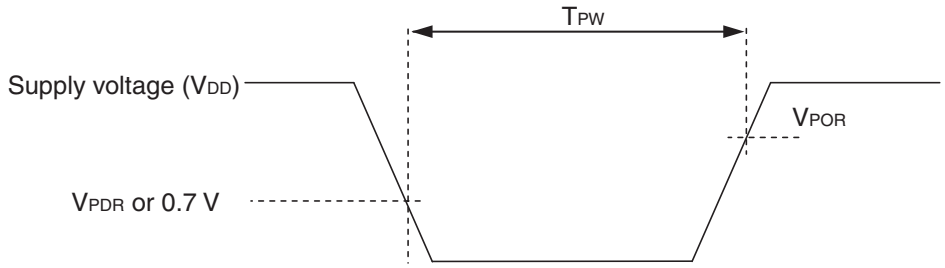
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.50 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor output voltage that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 3.6.3 POR circuit characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Power supply rise time | 1.45 | 1.51 | 1.57 | V |
| | $V_{PDR}$ | Power supply fall time | 1.44 | 1.50 | 1.56 | V |
| Minimum pulse width Note | $T_{PW}$ | | 300 | | | μs |

**Note** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



**LVD detection voltage of interrupt & reset mode**

**($T_A$ = –40 to +105°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC1}$ = 0, 1, 1, falling reset voltage | | | 2.64 | 2.75 | 2.86 | V |
| | $V_{LVDD1}$ | | LVIS1, LVIS0 = 1, 0 | Rising reset release voltage | 2.81 | 2.92 | 3.03 | V |
| | | | | Falling interrupt voltage | 2.75 | 2.86 | 2.97 | V |
| | $V_{LVDD2}$ | | LVIS1, LVIS0 = 0, 1 | Rising reset release voltage | 2.90 | 3.02 | 3.14 | V |
| | | | | Falling interrupt voltage | 2.85 | 2.96 | 3.07 | V |
| | $V_{LVDD3}$ | | LVIS1, LVIS0 = 0, 0 | Rising reset release voltage | 3.90 | 4.06 | 4.22 | V |
| | | | | Falling interrupt voltage | 3.83 | 3.98 | 4.13 | V |

### 3.6.5 Power supply voltage rising slope characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

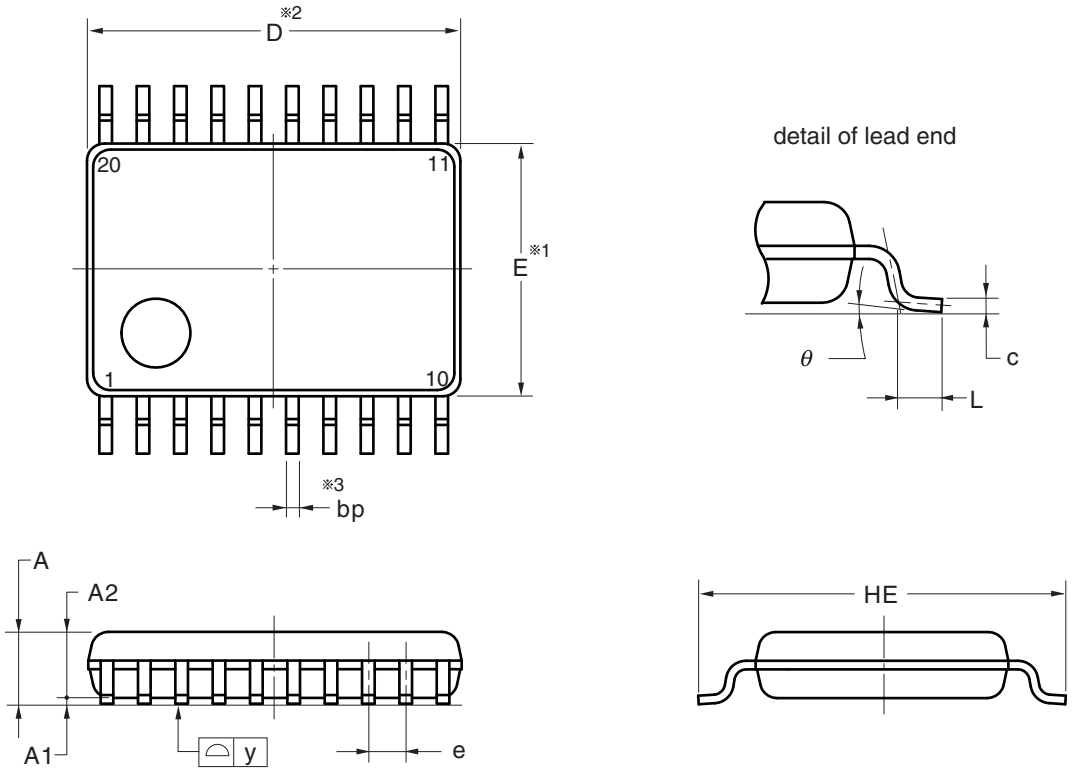
**Caution** Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 29.4 AC Characteristics.

# 4. PACKAGE DRAWINGS

## 4.1 20-pin products

R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP
R5F1036AASP, R5F10369ASP, R5F10368ASP, R5F10367ASP, R5F10366ASP
R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP
R5F1036ADSP, R5F10369DSP, R5F10368DSP, R5F10367DSP, R5F10366DSP
<R> R5F1026AGSP, R5F10269GSP, R5F10268GSP, R5F10267GSP, R5F10266GSP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LSSOP20-4.4x6.5-0.65 | PLSP0020JB-A | P20MA-65-NAA-1 | 0.1 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 6.50±0.10 |
| E | 4.40±0.10 |
| HE | 6.40±0.20 |
| A | 1.45 MAX. |
| A1 | 0.10±0.10 |
| A2 | 1.15 |
| e | 0.65±0.12 |
| bp | $0.22^{+0.10}_{-0.05}$ |
| c | $0.15^{+0.05}_{-0.02}$ |
| L | 0.50±0.20 |
| y | 0.10 |
| θ | 0° to 10° |

**NOTE**

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

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