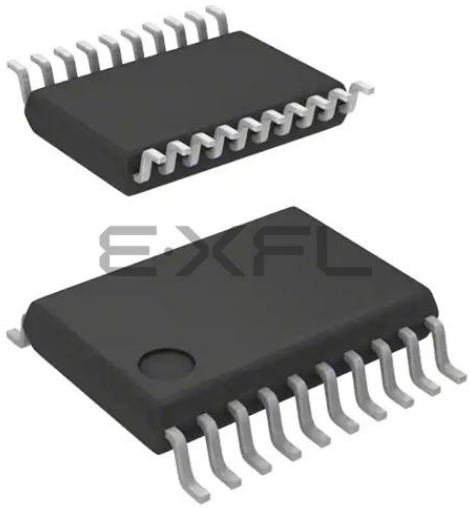

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10367asp-x5

1.3 Differences between the R5F102 Products and the R5F103 Products

The following are differences between the R5F102 products and the R5F103 products.

- Whether the data flash memory is mounted or not
- High-speed on-chip oscillator oscillation frequency accuracy
- Number of channels in serial interface
- Whether the DMA function is mounted or not
- Whether a part of the safety functions are mounted or not

1.3.1 Data Flash

The data flash memory of 2 KB is mounted on the R5F102 products, but not on the R5F103 products.

Product	Data Flash
R5F102 products R5F1026A, R5F1027A, R5F102AA, R5F10269, R5F10279, R5F102A9, R5F10268, R5F10278, R5F102A8, R5F10267, R5F10277, R5F102A7, R5F10266 Note	2KB
R5F103 products R5F1036A, R5F1037A, R5F103AA, R5F10369, R5F10379, R5F103A9, R5F10368, R5F10378 R5F103A8, R5F10367, R5F10377, R5F103A7, R5F10366	Not mounted

Note The RAM in the R5F10266 has capacity as small as 256 bytes. Depending on the customer's program specification, the stack area to execute the data flash library may not be kept and data may not be written to or erased from the data flash memory.

Caution When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

1.3.2 On-chip oscillator characteristics

(1) High-speed on-chip oscillator oscillation frequency of the R5F102 products

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = -20 to +85 °C	-1.0	+1.0	%
	T_A = -40 to -20 °C	-1.5	+1.5	
	T_A = +85 to +105 °C	-2.0	+2.0	

(2) High-speed on-chip oscillator oscillation frequency of the R5F103 products

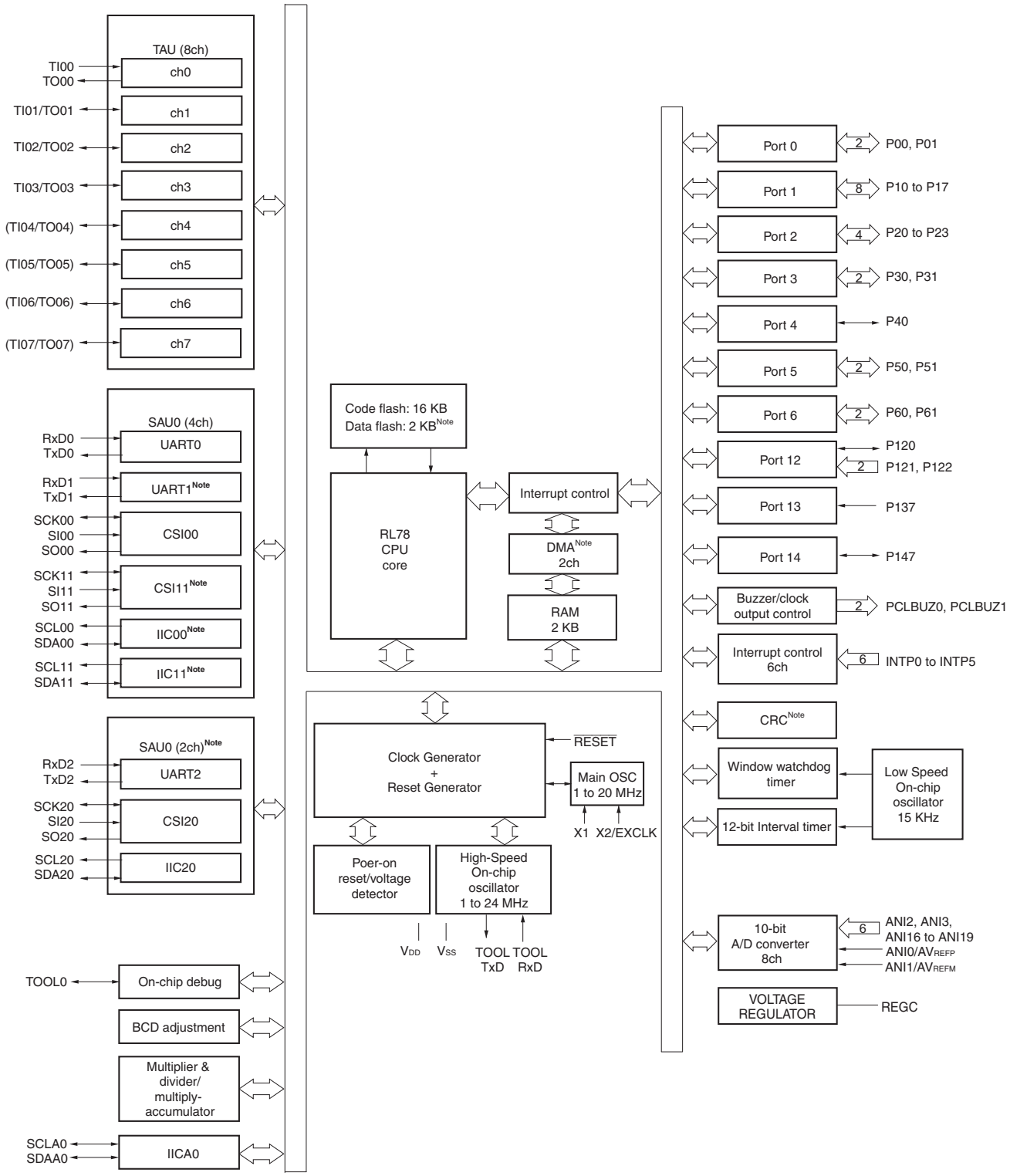
Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = -40 to + 85 °C	-5.0	+5.0	%

1.3.3 Peripheral Functions

The following are differences in peripheral functions between the R5F102 products and the R5F103 products.

RL78/G12		R5F102 product		R5F103 product	
		20, 24 pin product	30 pin product	20, 24 pin product	30 pin product
Serial interface	UART	1 channel	3 channels	1 channel	
	CSI	2 channels	3 channels	1 channel	
	Simplified I^2C	2 channels	3 channels	None	
DMA function		2 channels		None	
Safety function	CRC operation	Yes		None	
	RAM guard	Yes		None	
	SFR guard	Yes		None	

1.6.3 30-pin products



Note Provided only in the R5F102 products.

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

(2) 30-pin products

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (High-speed main) mode Note 4	f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.5		mA
						V_{DD} = 3.0 V		1.5		
					Normal operation	V_{DD} = 5.0 V		3.7	5.5	mA
						V_{DD} = 3.0 V		3.7	5.5	
				f_{IH} = 16 MHz Note 3		V_{DD} = 5.0 V		2.7	4.0	mA
						V_{DD} = 3.0 V		2.7	4.0	
			LS (Low-speed main) mode Note 4	f_{IH} = 8 MHz Note 3		V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	
			HS (High-speed main) mode Note 4	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V		Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V		Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V		Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V		Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
			LS (Low-speed main) mode Note 4	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.

3. When high-speed system clock is stopped

4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

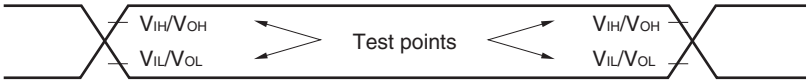
LS(Low speed main) mode: V_{DD} = 1.8 V to 5.5 V @1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

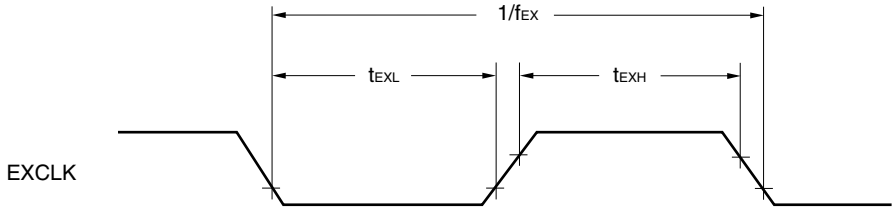
2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C.

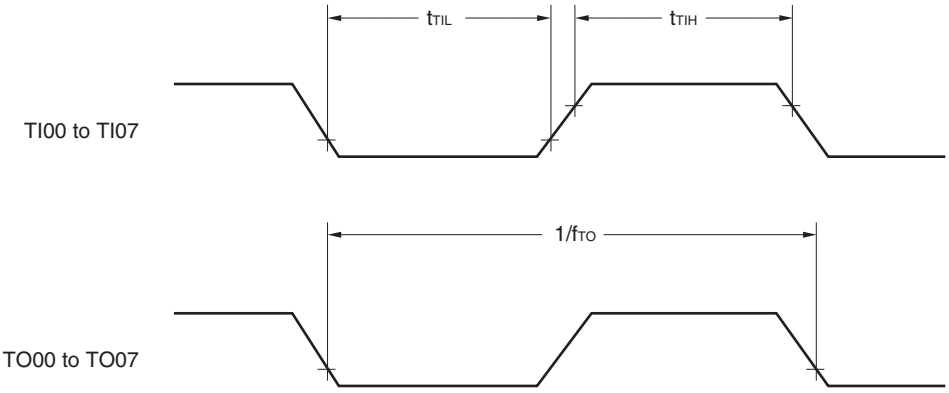
AC Timing Test Point



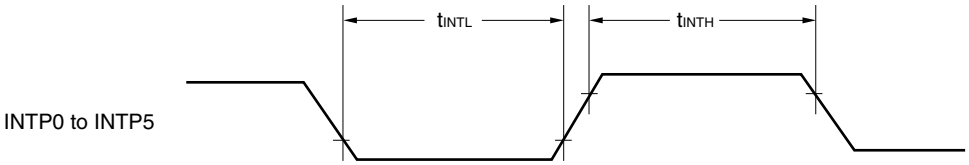
External Main System Clock Timing



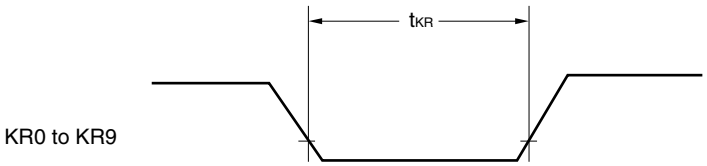
TI/TO Timing



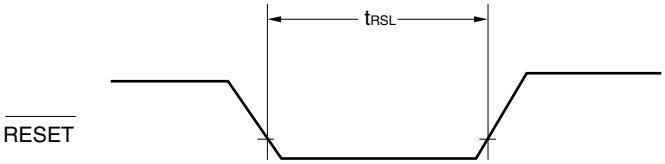
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	167		500		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	250		500		ns
			1.8 V ≤ V_{DD} ≤ 5.5 V	–		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2−12		t_{KCY1}/2−50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2−18		t_{KCY1}/2−50		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2−38		t_{KCY1}/2−50		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		–		t_{KCY1}/2−50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		44		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		44		110		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		75		110		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		–		110		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note4			25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products.))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate Note4		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/6 Note1		f_{MCK}/6 Note1	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note3		4.0		1.3	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/6 Note1		f_{MCK}/6 Note1	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note3		4.0		1.3	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/6 Notes1, 2		f_{MCK}/6 Notes1, 2	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note3		4.0		1.3	Mbps
		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		**Note4**		**Note4**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note5		2.8 Note5	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V,		**Note6**		**Note6**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note7		1.2 Note7	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		**Notes 2, 8**		**Notes 2, 8**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note9		0.43 Note9	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. Use it with $V_{DD} \geq V_b$.

3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

4. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2.5.2 Serial interface IICA

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode / LS (low-speed main) mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz			0	400	kHz
		Normal mode: f_{CLK} ≥ 1 MHz	0	100			kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		0.6		μs
Hold time[Note 1]	$t_{HD:STA}$		4.0		0.6		μs
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		μs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		μs
Bus-free time	t_{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

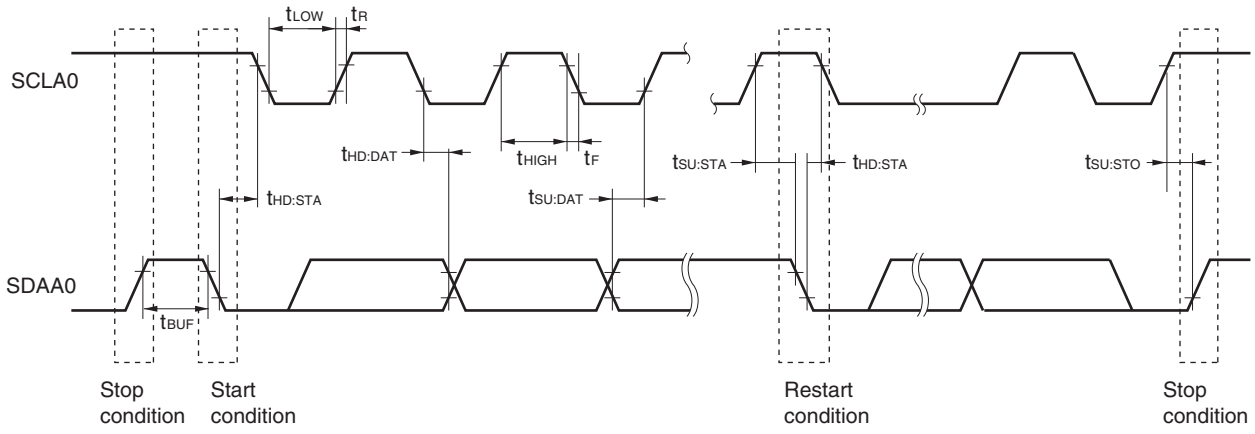
<R> **2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: C_b = 400 pF, Rb = 2.7 kΩ
Fast mode: C_b = 320 pF, Rb = 1.1 kΩ

IICA serial transfer timing



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (–) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (–) = AV_{REFM}
ANI0 to ANI3	Refer to **28.6.1 (1)**.	Refer to **28.6.1 (3)**.	Refer to **28.6.1 (4)**.
ANI16 to ANI22	Refer to **28.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **28.6.1 (1)**.		–

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +85°C, 1.8 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD} [Note 3]			1.2	±3.5	LSB
					1.2	±7.0 [Note 4]	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2, ANI3	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
				57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±0.25	%FSR
						±0.50 [Note 4]	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±0.25	%FSR
						±0.50 [Note 4]	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±2.5	LSB
						±5.0 [Note 4]	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±1.5	LSB
						±2.0 [Note 4]	LSB
Analog input voltage	V_{AIN}	ANI2, ANI3		0		AV_{REFP}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} [Note 5]			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} [Note 5]			V

(**Notes** are listed on the next page.)

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (−) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (−) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution			1.2	±7.0	LSB
					1.2	±10.5 Note 3	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
				57		95	μs
Conversion time	tCONV	10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution				±0.60	%FSR
						±0.85 Note 3	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution				±0.60	%FSR
						±0.85 Note 3	%FSR
Integral linearity error Note 1	ILE	10-bit resolution				±4.0	LSB
						±6.5 Note 3	LSB
Differential linearity error Note 1	DLE	10-bit resolution				±2.0	LSB
						±2.5 Note 3	LSB
Analog input voltage	VAIN	ANI0 to ANI3, ANI16 to ANI22		0		V_{DD}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} Note 4			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} Note 4			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

2.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode

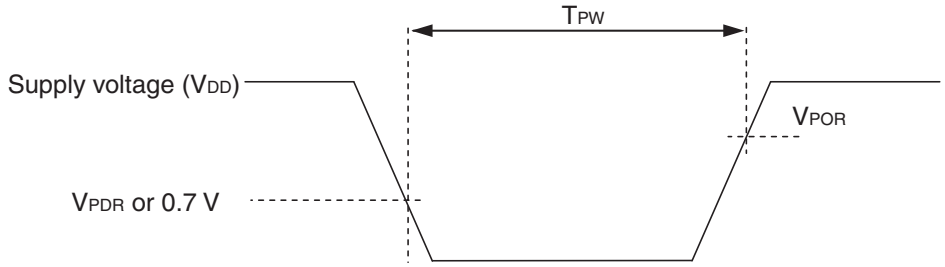
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

2.6.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width Note	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			−0.5 to + 6.5	V
REGC terminal input voltage[Note1]	V_{IREGC}	REGC		−0.3 to +2.8 and −0.3 to V_{DD} + 0.3 [Note 2]	V
Input Voltage	V_{I1}	Other than P60, P61		−0.3 to V_{DD} + 0.3[Note 3]	V
	V_{I2}	P60, P61 (N-ch open drain)		−0.3 to 6.5	V
Output Voltage	V_O			−0.3 to V_{DD} + 0.3[Note 3]	V
Analog input voltage	V_{AI}	20, 24-pin products: ANI0 to ANI3, ANI16 to ANI22 30-pin products: ANI0 to ANI3, ANI16 to ANI19		−0.3 to V_{DD} + 0.3 and −0.3 to AVREF(+)+0.3 [Notes 3, 4]	V
Output current, high	I_{OH1}	Per pin	Other than P20 to P23	−40	mA
		Total of all pins	All the terminals other than P20 to P23	−170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	−70	mA
			20-, 24-pin products: P00 to P03[Note 5], P10 to P14 30-pin products: P10 to P17, P30, P31, P50, P51, P147	−100	mA
	I_{OH2}	Per pin	P20 to P23	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	Other than P20 to P23	40	mA
		Total of all pins	All the terminals other than P20 to P23	170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	70	mA
			20-, 24-pin products: P00 to P03 [Note 5], P10 to P14, P60, P61 30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147	100	mA
	I_{OL2}	Per pin	P20 to P23	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A			−40 to +105	°C
Storage temperature	T_{stg}			−65 to +150	°C

Notes 1. 30-pin product only.

2. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.

3. Must be 6.5 V or lower.

4. Do not exceed $AV_{REF}(+)$ + 0.3 V in case of A/D conversion target pin.

5. 24-pin products only.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF}(+)$: + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

(2) 30-pin products

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS (High-speed main) mode[Note 4]	f_{IH} = 24 MHz[Note 3]	Basic operation	V_{DD} = 5.0 V		1.5		mA
						V_{DD} = 3.0 V		1.5		
					Normal operation	V_{DD} = 5.0 V		3.7	5.8	mA
						V_{DD} = 3.0 V		3.7	5.8	
				f_{IH} = 16 MHz[Note 3]		V_{DD} = 5.0 V		2.7	4.2	mA
						V_{DD} = 3.0 V		2.7	4.2	
				f_{MX} = 20 MHz[Note 2], V_{DD} = 5.0 V		Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	
				f_{MX} = 20 MHz[Note 2], V_{DD} = 3.0 V		Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 5.0 V		Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	
				f_{MX} = 10 MHz[Note 2], V_{DD} = 3.0 V		Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.

3. When high-speed system clock is stopped

4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @1 MHz to 24 MHz
V_{DD} = 2.4 V to 5.5 V @1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C.

(3) Peripheral functions (Common to all products)

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed onchip oscillator operating current	I_{FIL} Note 1				0.20		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 2, 3				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 4	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 5	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.30	1.70	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.50	0.70	mA
A/D converter reference voltage operating current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVD} Notes 1, 6				0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 8				2.00	12.20	mA
BGO operating current	I_{BGO} Notes 1, 7				2.00	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 9		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	2.04	mA
		CSI/UART operation			0.70	1.54	mA

Notes 1. Current flowing to the V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{FIL} and I_{TMKA} when the 12-bit interval timer operates.

4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

6. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.

7. Current flowing only during data flash rewrite.

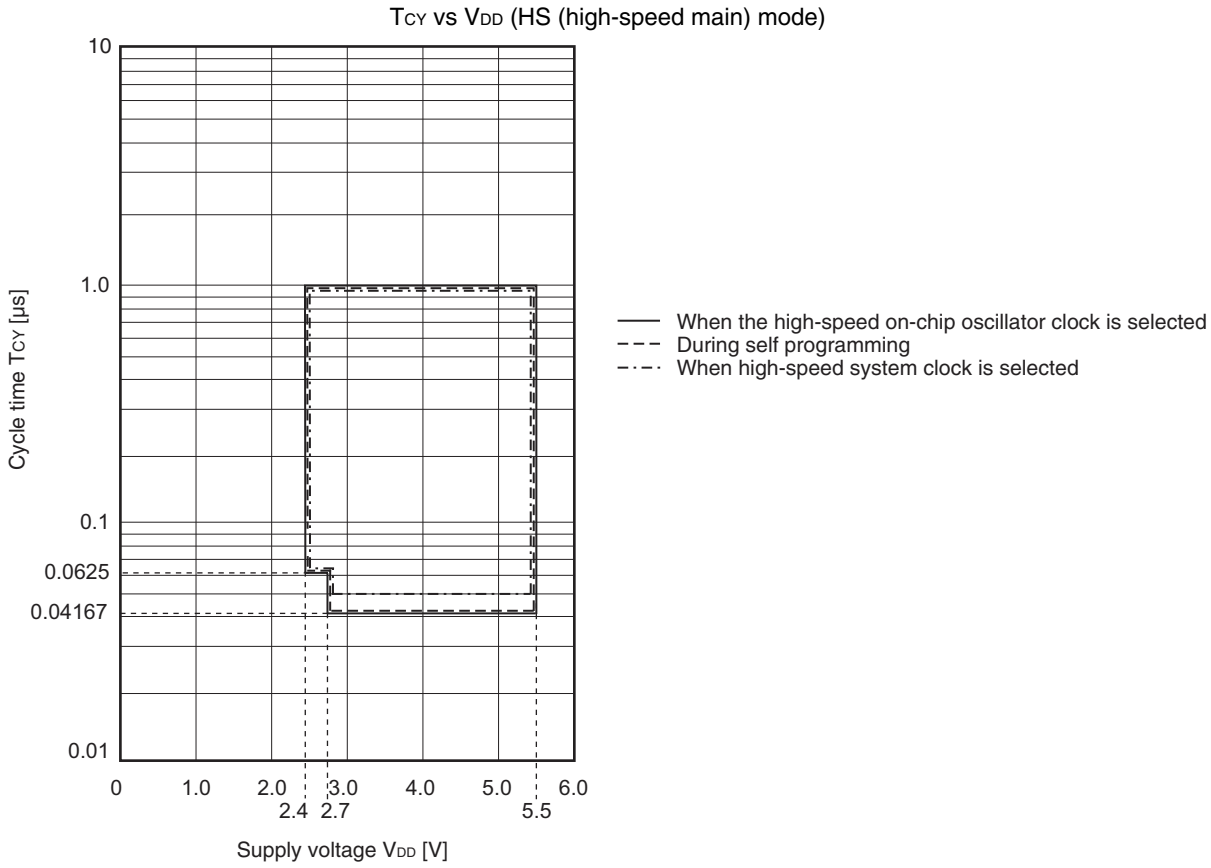
8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.

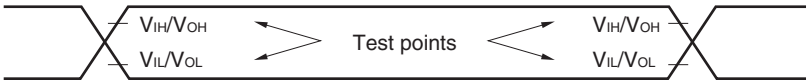
Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. Temperature condition of the TYP. value is T_A = 25°C

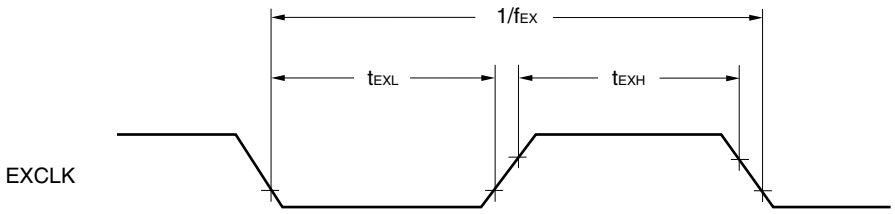
Minimum Instruction Execution Time during Main System Clock Operation



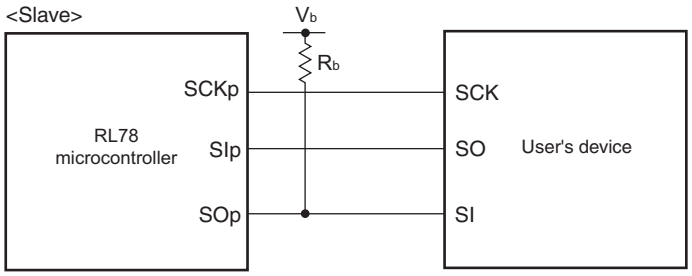
AC Timing Test Point



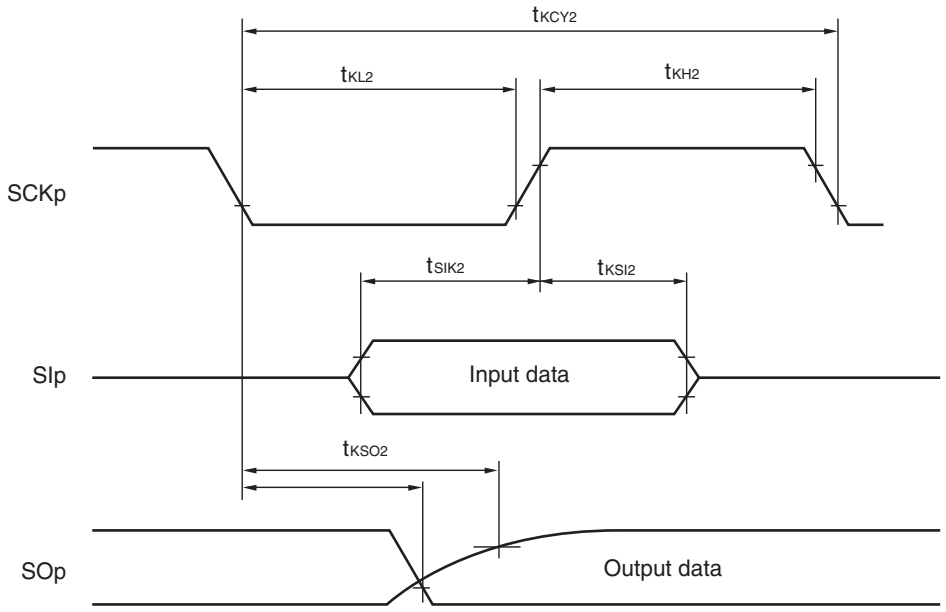
External Main System Clock Timing



CSI mode connection diagram (during communication at different potential)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



Remarks 1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn))

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode)

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		100 Note1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		100 Note1	kHz
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ		100 Note1	kHz
Hold time when SCLr = "L"	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	4600		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	4600		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	2700		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	2400		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	1830		ns
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 760 Note3		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 760 Note3		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 570 Note3		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	1420	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	0	1215	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

2. Set $t_{SU:DAT}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

Cautions 1. Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

2. IIC01 and IIC11 cannot communicate at different potential.

(**Remarks** are listed on the next page.)

3.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

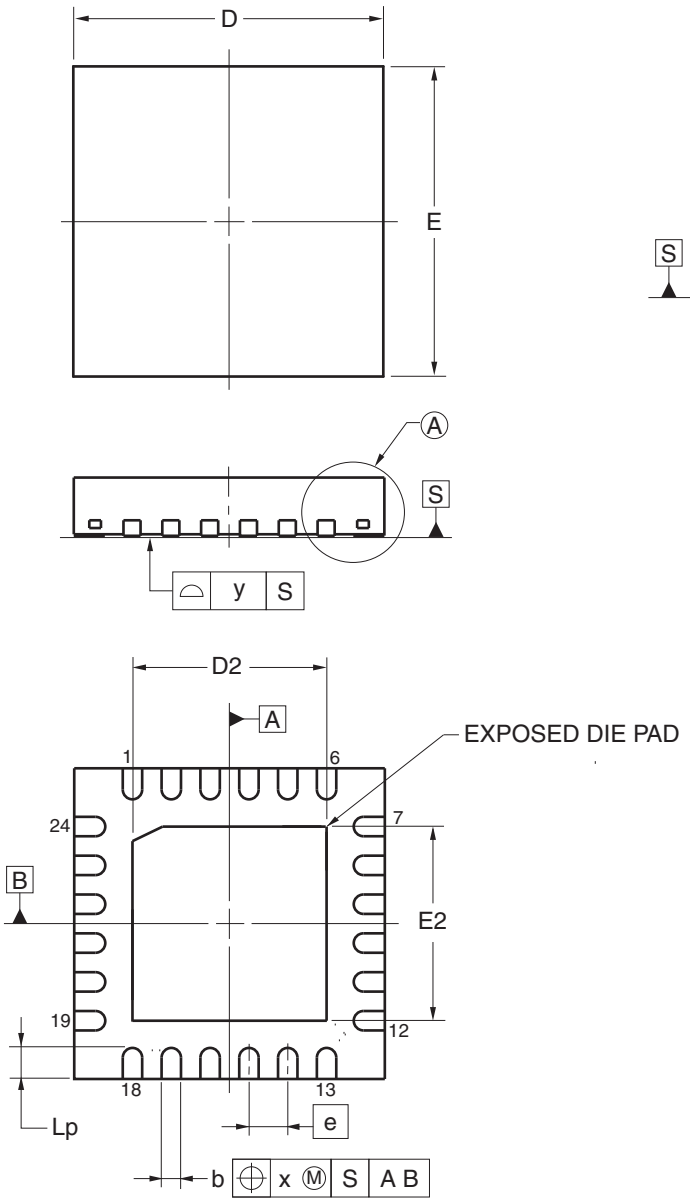
(T_A = –40 to +105°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

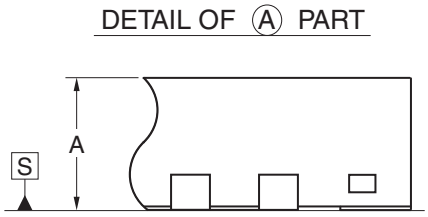
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	V_{LVD0}	Power supply rise time	3.90	4.06	4.22	V
		Power supply fall time	3.83	3.98	4.13	V
	V_{LVD1}	Power supply rise time	3.60	3.75	3.90	V
		Power supply fall time	3.53	3.67	3.81	V
	V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
		Power supply fall time	2.94	3.06	3.18	V
	V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
		Power supply fall time	2.85	2.96	3.07	V
	V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
		Power supply fall time	2.75	2.86	2.97	V
	V_{LVD5}	Power supply rise time	2.70	2.81	2.92	V
		Power supply fall time	2.64	2.75	2.86	V
	V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
		Power supply fall time	2.55	2.65	2.75	V
	V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
		Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width	t_{LW}		300			μs
Detection delay time					300	μs

4.2 24-pin products

R5F1027AANA, R5F10279ANA, R5F10278ANA, R5F10277ANA
R5F1037AANA, R5F10379ANA, R5F10378ANA, R5F10377ANA
R5F1027ADNA, R5F10279DNA, R5F10278DNA, R5F10277DNA
R5F1037ADNA, R5F10379DNA, R5F10378DNA, R5F10377DNA
<R> R5F1027AGNA, R5F10279GNA, R5F10278GNA, R5F10277GNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN24-4x4-0.50	PWQN0024KE-A	P24K8-50-CAB-1	0.04





(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.05
E	4.00±0.05
A	0.75±0.05
b	$0.25^{+0.05}_{-0.07}$
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	2.45	2.50	2.55	2.45	2.50	2.55

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