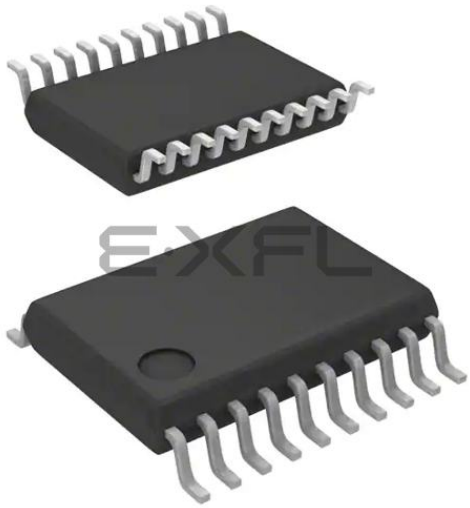

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CSI, I²C, UART/USART |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 14 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 768 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 11x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-LSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10368asp-x5 |

## 1.7 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

| Item | | 20-pin | | 24-pin | | 30-pin | |
|---|---|---|---|---|---|---|---|
| | | R5F1026x | R5F1036x | R5F1027x | R5F1037x | R5F102Ax | R5F103Ax |
| Code flash memory | | 2 to 16 KB Note 1 | | 4 to 16 KB | | | |
| Data flash memory | | 2 KB | – | 2 KB | – | 2 KB | – |
| RAM | | 256 B to 1.5 KB | | 512 B to 1.5 KB | | 512 B to 2KB | |
| Address space | | 1 MB | | | | | |
| <R> Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (High-speed main) mode : 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode : 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode : 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V) | | | | | |
| | High-speed on-chip oscillator clock | HS (High-speed main) mode : 1 to 24 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode : 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode : 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V) | | | | | |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP) | | | | | |
| General-purpose register | | (8-bit register × 8) × 4 banks | | | | | |
| Minimum instruction execution time | | 0.04167 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 24 MHz operation) | | | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits)<br>• Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc. | | | | | |
| I/O port | Total | 18 | | 22 | | 26 | |
| | CMOS I/O | 12<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 4) | | 16<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 5) | | 21<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 9) | |
| | CMOS input | 4 | | 4 | | 3 | |
| | N-ch open-drain I/O (6 V tolerance) | 2 | | | | | |
| Timer | 16-bit timer | 4 channels | | | | 8 channels | |
| | Watchdog timer | 1 channel | | | | | |
| | 12-bit Interval timer | 1 channel | | | | | |
| | Timer output | 4 channels<br>(PWM outputs: 3 Note 3) | | | | 8 channels<br>(PWM outputs: 7 Note 3) Note 2 | |

**Notes 1.** The self-programming function cannot be used in the R5F10266 and R5F10366.

**2.** The maximum number of channels when PIOR0 is set to 1.

**3.** The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). (See **6.9.3 Operation as multiple PWM output function**.)

**Caution** When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

# <R> 2. ELECTRICAL SPECIFICATIONS ($T_A$ = –40 to +85°C)

<R> This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A$ = -40 to +85°C

<R> R5F102xxAxx, R5F103xxAxx

D: Industrial applications $T_A$ = -40 to +85°C

<R> R5F102xxDxx, R5F103xxDxx

G: Industrial applications when $T_A$ = -40 to +105°C products is used in the range of $T_A$ = -40 to +85°C

<R> R5F102xxGxx

**Cautions 1.** The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

**2.** The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product.

**(1) 20-, 24-pin products**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 6 | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 440 | 1210 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 1210 | |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 400 | 950 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 950 | |
| | | | LS (Low-speed main) mode Note 6 | $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 270 | 542 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 270 | 542 | |
| | | | HS (High-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1000 | μA |
| | | | | | Resonator connection | | 450 | 1170 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1000 | μA |
| | | | | | Resonator connection | | 450 | 1170 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 190 | 590 | μA |
| | | | | | Resonator connection | | 260 | 660 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 190 | 590 | μA |
| | | | | | Resonator connection | | 260 | 660 | |
| | | | LS (Low-speed main) mode Note 6 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 360 | μA |
| | | | | | Resonator connection | | 150 | 416 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 360 | μA |
| | | | | | Resonator connection | | 150 | 416 | |
| | $I_{DD3}$ Note 5 | STOP mode | $T_A$ = –40°C | | | | 0.19 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.32 | 0.80 | |
| | | | $T_A$ = +70°C | | | | 0.48 | 1.20 | |
| | | | $T_A$ = +85°C | | | | 0.74 | 2.20 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS(Low speed main) mode: $V_{DD}$ = 1.8 V to 5.5 V @1 MHz to 8 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except temperature condition of the TYP. value is $T_A$ = 25°C, other than STOP mode

**(2) 30-pin products**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 6 | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 440 | 1280 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 1280 | |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 400 | 1000 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 1000 | |
| | | | LS (Low-speed main) mode Note 6 | $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 260 | 530 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 260 | 530 | |
| | | | HS (High-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1000 | μA |
| | | | | | Resonator connection | | 450 | 1170 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1000 | μA |
| | | | | | Resonator connection | | 450 | 1170 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 190 | 600 | μA |
| | | | | | Resonator connection | | 260 | 670 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 190 | 600 | μA |
| | | | | | Resonator connection | | 260 | 670 | |
| | | | LS (Low-speed main) mode Note 6 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | |
| | | | | $f_{MX}$ = 8 MHz Note 3 $V_{DD}$ = 2.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | |
| | $I_{DD3}$ Note 5 | STOP mode | $T_A$ = –40°C | | | | 0.18 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.30 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.46 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.75 | 3.30 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS (Low speed main) mode: $V_{DD}$ = 1.8 V to 5.5 V @1 MHz to 8 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C.

### (3) Peripheral functions (Common to all products)

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed onchip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | μA |
| 12-bit interval timer operating current | $I_{TMKA}$ Notes 1, 2, 3 | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 4 | $f_{IL}$ = 15 kHz | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 5 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | 1.30 | 1.70 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.50 | 0.70 | mA |
| A/D converter reference voltage operating current | $I_{ADREF}$ Note 1 | | | | 75.0 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | 75.0 | | μA |
| LVD operating current | $I_{LVD}$ Notes 1, 6 | | | | 0.08 | | μA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 8 | | | | 2.00 | 12.20 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 7 | | | | 2.00 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 9 | | 0.50 | 0.60 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 1.44 | mA |
| | | CSI/UART operation | | | 0.70 | 0.84 | mA |

**Notes 1.** Current flowing to the $V_{DD}$.

**2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**3.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$, and $I_{FIL}$ and $I_{TMKA}$ when the 12-bit interval timer operates.

**4.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer operates.

**5.** Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**6.** Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit operates.

**7.** Current flowing only during data flash rewrite.

**8.** Current flowing only during self programming.

**9.** For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.

**Remarks 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**2.** Temperature condition of the TYP. value is $T_A$ = 25°C

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 300 | | 1150 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 500 | | 1150 | | ns |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 −75 | | $t_{KCY1}$/2−75 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 −170 | | $t_{KCY1}$/2−170 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 −458 | | $t_{KCY1}$/2−458 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 −12 | | $t_{KCY1}$/2−50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 −18 | | $t_{KCY1}$/2−50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 −50 | | $t_{KCY1}$/2−50 | | ns |

**Note** Use it with $V_{DD} \geq V_b$.

**Cautions 1.** Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.

**2.** CSI01 and CSI11 cannot communicate at different potential.

**Remarks 1.** $R_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$ [F]: Communication line (SCKp, SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20)

**(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 12/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 10/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 − 12 | | $t_{KCY2}$/2 − 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 − 18 | | $t_{KCY2}$/2 − 50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | $t_{KCY2}$/2 − 50 | | $t_{KCY2}$/2 − 50 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_{DD}$ ≤ 4.0 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_{DD}$ ≤ 2.0 V Note 2 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 5 | $t_{KSO2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 120 | | 2/$f_{MCK}$ + 573 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

**Notes 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**2.** Use it with $V_{DD} \geq V_b$.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Cautions 1.** Select the TTL input buffer for the SIp and SCKp pins and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**2.** CSI01 and CSI11 cannot communicate at different potential.

### 2.5.2 Serial interface IICA

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode / LS (low-speed main) mode | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Standard Mode | | Fast Mode | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | | | 0 | 400 | kHz |
| | | Normal mode: $f_{CLK}$ ≥ 1 MHz | 0 | 100 | | | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | | 4.7 | | 0.6 | | μs |
| Hold time[Note 1] | $t_{HD:STA}$ | | 4.0 | | 0.6 | | μs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | | 4.7 | | 1.3 | | μs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | | 4.0 | | 0.6 | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | | 250 | | 100 | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | | 0 | 3.45 | 0 | 0.9 | μs |
| Setup time of stop condition | $t_{SU:STO}$ | | 4.0 | | 0.6 | | μs |
| Bus-free time | $t_{BUF}$ | | 4.7 | | 1.3 | | μs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

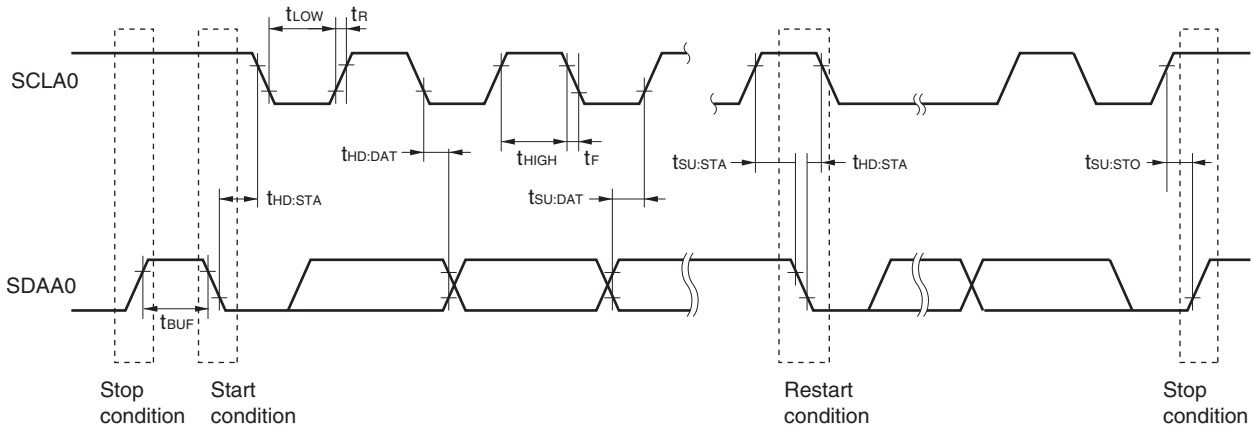
<R> **2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: $C_b$ = 400 pF, Rb = 2.7 kΩ
Fast mode: $C_b$ = 320 pF, Rb = 1.1 kΩ

IICA serial transfer timing



### 2.6.2 Temperature sensor/internal reference voltage characteristics

**($T_A$ = –40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, HS (high-speed main) mode**

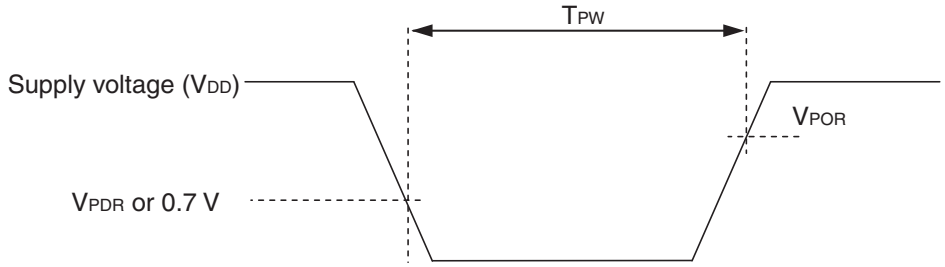
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.50 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor output voltage that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 2.6.3 POR circuit characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Power supply rise time | 1.47 | 1.51 | 1.55 | V |
| | $V_{PDR}$ | Power supply fall time | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width Note | $T_{PW}$ | | 300 | | | μs |

**Note** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).

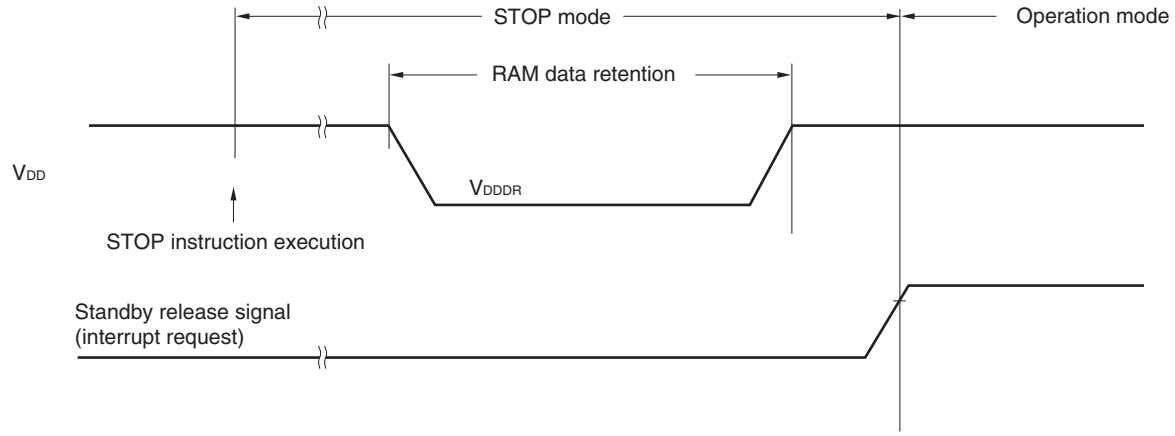


## <R> 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

**($T_A$ = −40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.46 Note | | 5.5 | V |

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.




## 2.8 Flash Memory Programming Characteristics

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

<R>

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| System clock frequency | $f_{CLK}$ | | 1 | | 24 | MHz |
| Code flash memory rewritable times Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years $T_A$ = 85°C | 1,000 | | | Times |
| Data flash memory rewritable times Notes 1, 2, 3 | | Retained for 1 year $T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years $T_A$ = 85°C | 100,000 | | | |
| | | Retained for 20 years $T_A$ = 85°C | 10,000 | | | |

**Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**2.** When using flash memory programmer and Renesas Electronics self programming library

**3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

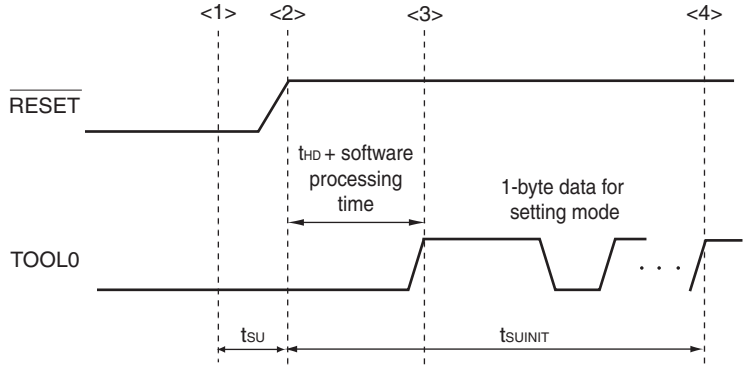
**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 2.10 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Time to complete the communication for the initial setting after the external reset is released | $t_{SUINIT}$ | POR and LVD reset are released before external reset release | | | 100 | ms |
| Time to release the external reset after the TOOL0 pin is set to the low level | $t_{SU}$ | POR and LVD reset are released before external reset release | 10 | | | μs |
| Time to hold the TOOL0 pin at the low level after the external reset is released<br>(excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset are released before external reset release | 1 | | | ms |




<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{SU}$: Time to release the external reset after the TOOL0 pin is set to the low level

$t_{HD}$: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

# <R> 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A$ = –40 to +105°C)

<R> This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A$ = -40 to +105°C

<R> R5F102xxGxx

**Cautions 1.** The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

**2.** The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product.

**3.** Please contact Renesas Electronics sales office for derating of operation under $T_A$ = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

**Remark When the RL78 microcontroller is used in the range of $T_A$ = -40 to +85 °C, see CHAPTER 28**

<R> **ELECTRICAL SPECIFICATIONS (A: $T_A$ = -40 to +85 °C).**

There are following differences between the products "G: Industrial applications ($T_A$ = -40 to +105°C)" and the products “A: Consumer applications, and D: Industrial applications”.

| Parameter | Application | |
|---|---|---|
| | A: Consumer applications, D: Industrial applications | G: Industrial applications |
| Operating ambient temperature | $T_A$ = -40 to +85°C | $T_A$ = -40 to +105°C |
| Operating mode<br>Operating voltage range | HS (high-speed main) mode:<br>2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz<br>2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz<br>LS (low-speed main) mode:<br>1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz | HS (high-speed main) mode only:<br>2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz<br>2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz |
| High-speed on-chip oscillator clock accuracy | R5F102 products, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V:<br>±1.0%@ $T_A$ = -20 to +85°C<br>±1.5%@ $T_A$ = -40 to -20°C<br>R5F103 products, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V:<br>±5.0%@ $T_A$ = -40 to +85°C | R5F102 products, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V:<br>±2.0%@ $T_A$ = +85 to +105°C<br>±1.0%@ $T_A$ = -20 to +85°C<br>±1.5%@ $T_A$ = -40 to -20°C |
| Serial array unit | UART<br>CSI: $f_{CLK}$/2 (supporting 12 Mbps), $f_{CLK}$/4<br>Simplified $I^2C$ communication | UART<br>CSI: $f_{CLK}$/4<br>Simplified $I^2C$ communication |
| Voltage detector | Rise detection voltage: 1.88 V to 4.06 V (12 levels)<br>Fall detection voltage: 1.84 V to 3.98 V (12 levels) | Rise detection voltage: 2.61 V to 4.06 V (8 levels)<br>Fall detection voltage: 2.55 V to 3.98 V (8 levels) |

**Remark** The electrical characteristics of the products G: Industrial applications ($T_A$ = -40 to +105°C) are different from those of the products “A: Consumer applications, and D: Industrial applications”. For details, refer to **29.1** to **29.10**.

## 3.3.2 Supply current characteristics

**(1) 20-, 24-pin products**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD1}$ | Operating mode | HS (High-speed main) mode[Note 4] | $f_{IH}$ = 24 MHz[Note 3] | Basic operation | $V_{DD}$ = 5.0 V | | 1.5 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.5 | | |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.3 | 5.3 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.3 | 5.3 | |
| | | | | $f_{IH}$ = 16 MHz[Note 3] | | $V_{DD}$ = 5.0 V | | 2.5 | 3.9 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.5 | 3.9 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 2.8 | 4.7 | mA |
| | | | | | | Resonator connection | | 3.0 | 4.8 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 2.8 | 4.7 | mA |
| | | | | | | Resonator connection | | 3.0 | 4.8 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 1.8 | 2.8 | mA |
| | | | | | | Resonator connection | | 1.8 | 2.8 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 1.8 | 2.8 | mA |
| | | | | | | Resonator connection | | 1.8 | 2.8 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator clock is stopped.

**3.** When high-speed system clock is stopped

**4.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Temperature condition of the TYP. value is $T_A$ = 25°C.

### (2) 30-pin products

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 6 | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 440 | 2300 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 2300 | |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 400 | 1700 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 1700 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 190 | 1020 | μA |
| | | | | | Resonator connection | | 260 | 1100 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 190 | 1020 | μA |
| | | | | | Resonator connection | | 260 | 1100 | |
| | $I_{DD3}$ Note 5 | STOP mode | $T_A$ = –40°C | | | | 0.18 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.30 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.46 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.75 | 3.30 | |
| | | | $T_A$ = +105°C | | | | 2.94 | 15.30 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C.

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**4.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**5.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ $V_{DD}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3}\ [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**6.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

**7.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3}\ [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**8.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 7** above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). **For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 600 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 1000 | | ns |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 2300 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 –150 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 –340 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 –916 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 –24 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 –36 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 –100 | | ns |

**Cautions 1.** Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.

**2.** CSI01 and CSI11 cannot communicate at different potential.

**Remarks 1.** $R_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$ [F]: Communication line (SCKp, SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20)

## 3.6 Analog Characteristics

### 3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | | |
|---|---|---|---|
| | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (–) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$<br>Reference voltage (–) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$<br>Reference voltage (–) = $AV_{REFM}$ |
| ANI0 to ANI3 | Refer to **29.6.1 (1)**. | Refer to **29.6.1 (3)**. | Refer to **29.6.1 (4)**. |
| ANI16 to ANI22 | Refer to **29.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **29.6.1 (1)**. | | – |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | 1.2 | ±3.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI2, ANI3 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage<br>(HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error[Notes 1, 2] | EZS | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | | ±0.25 | %FSR |
| Full-scale error[Notes 1, 2] | EFS | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | | ±0.25 | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | | ±2.5 | LSB |
| Differential linearity error [Note 1] | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | | ±1.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI2, ANI3 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage<br>(HS (high-speed main) mode) | | $V_{BGR}$ [Note 4] | | | V |
| | | Temperature sensor output voltage<br>(HS (high-speed main) mode) | | $V_{TMPS25}$ [Note 4] | | | V |

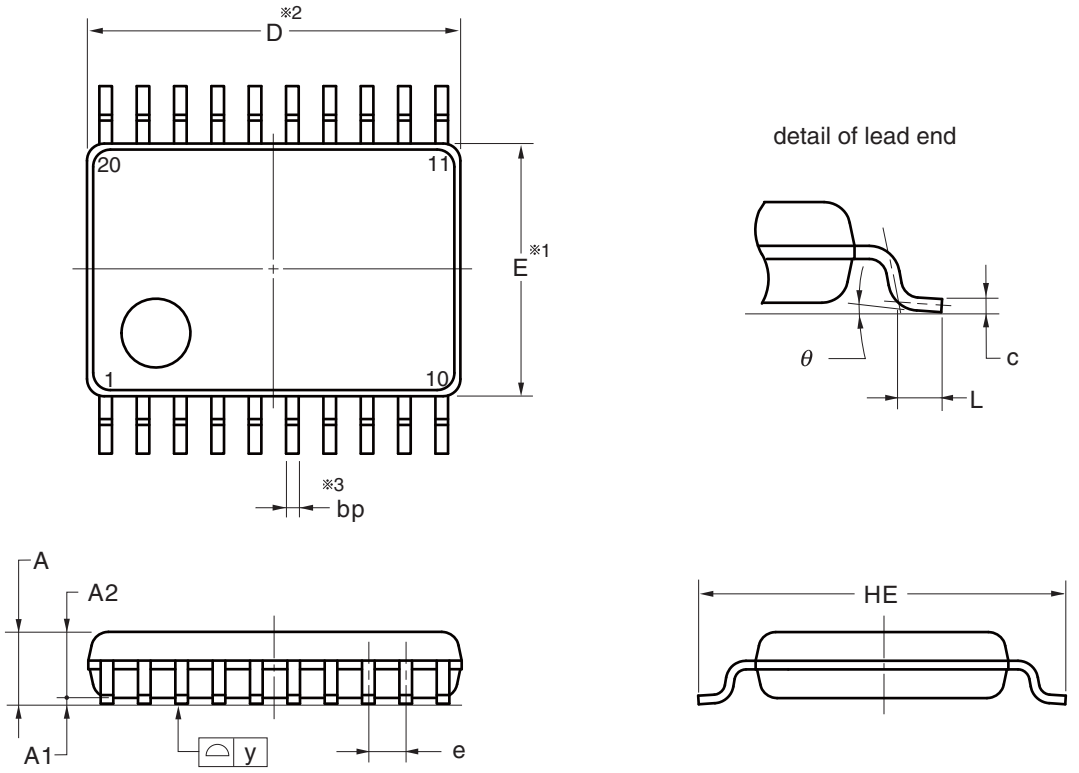
(**Notes** are listed on the next page.)

# 4. PACKAGE DRAWINGS

## 4.1 20-pin products

R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP
R5F1036AASP, R5F10369ASP, R5F10368ASP, R5F10367ASP, R5F10366ASP
R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP
R5F1036ADSP, R5F10369DSP, R5F10368DSP, R5F10367DSP, R5F10366DSP
<R> R5F1026AGSP, R5F10269GSP, R5F10268GSP, R5F10267GSP, R5F10266GSP

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LSSOP20-4.4x6.5-0.65 | PLSP0020JB-A | P20MA-65-NAA-1 | 0.1 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 6.50±0.10 |
| E | 4.40±0.10 |
| HE | 6.40±0.20 |
| A | 1.45 MAX. |
| A1 | 0.10±0.10 |
| A2 | 1.15 |
| e | 0.65±0.12 |
| bp | $0.22^{+0.10}_{-0.05}$ |
| c | $0.15^{+0.05}_{-0.02}$ |
| L | 0.50±0.20 |
| y | 0.10 |
| θ | 0° to 10° |

**NOTE**

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

## NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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**California Eastern Laboratories, Inc.**
4590 Patrick Henry Drive, Santa Clara, California 95054-1817, U.S.A.
Tel: +1-408-919-2500, Fax: +1-408-988-0279

**Renesas Electronics Europe Limited**
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

**Renesas Electronics Hong Kong Limited**
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

**Renesas Electronics Taiwan Co., Ltd.**
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

**Renesas Electronics Malaysia Sdn.Bhd.**
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics India Pvt. Ltd.**
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

**Renesas Electronics Korea Co., Ltd.**
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141





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