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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
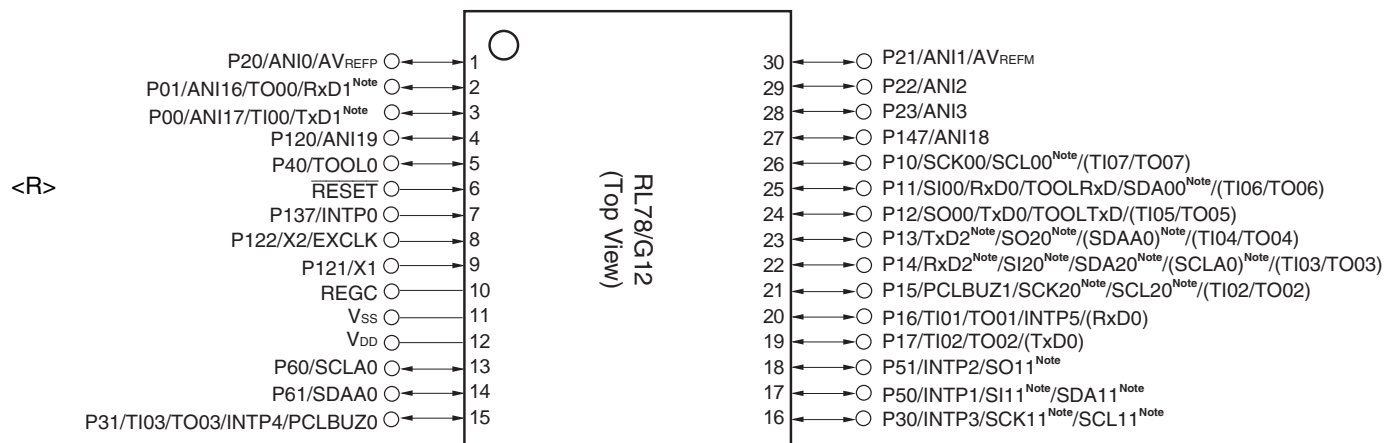
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1036aasp-x0

1.4.3 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)

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Pin assignments (Top View), RL78/G12:

Left side:
- 1 P20/ANI0/AV$_{REFP}$
- 2 P01/ANI16/TO00/RxD1[Note]
- 3 P00/ANI17/TI00/TxD1[Note]
- 4 P120/ANI19
- 5 P40/TOOL0
- 6 $\overline{RESET}$
- 7 P137/INTP0
- 8 P122/X2/EXCLK
- 9 P121/X1
- 10 REGC
- 11 V$_{SS}$
- 12 V$_{DD}$
- 13 P60/SCLA0
- 14 P61/SDAA0
- 15 P31/TI03/TO03/INTP4/PCLBUZ0

Right side:
- 30 P21/ANI1/AV$_{REFM}$
- 29 P22/ANI2
- 28 P23/ANI3
- 27 P147/ANI18
- 26 P10/SCK00/SCL00[Note]/(TI07/TO07)
- 25 P11/SI00/RxD0/TOOLRxD/SDA00[Note]/(TI06/TO06)
- 24 P12/SO00/TxD0/TOOLTxD/(TI05/TO05)
- 23 P13/TxD2[Note]/SO20[Note]/(SDAA0)[Note]/(TI04/TO04)
- 22 P14/RxD2[Note]/SI20[Note]/SDA20[Note]/(SCLA0)[Note]/(TI03/TO03)
- 21 P15/PCLBUZ1/SCK20[Note]/SCL20[Note]/(TI02/TO02)
- 20 P16/TI01/TO01/INTP5/(RxD0)
- 19 P17/TI02/TO02/(TxD0)
- 18 P51/INTP2/SO11[Note]
- 17 P50/INTP1/SI11[Note]/SDA11[Note]
- 16 P30/INTP3/SCK11[Note]/SCL11[Note]

Note Provided only in the R5F102 products.

Caution Connect the REGC pin to Vss via capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.5 Pin Identification**.
   2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR).**
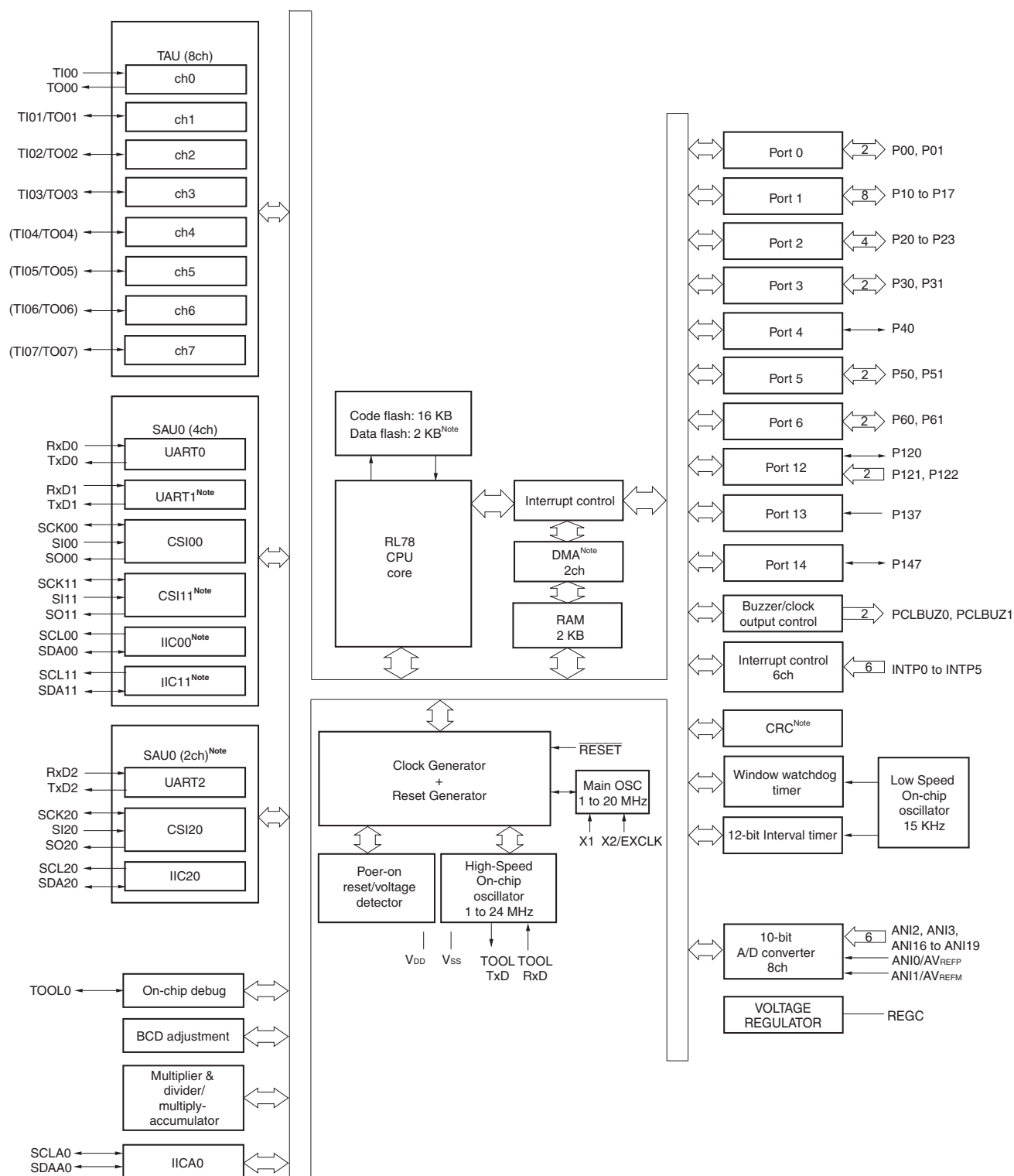
1.6 Block Diagram

1.6.1 20-pin products
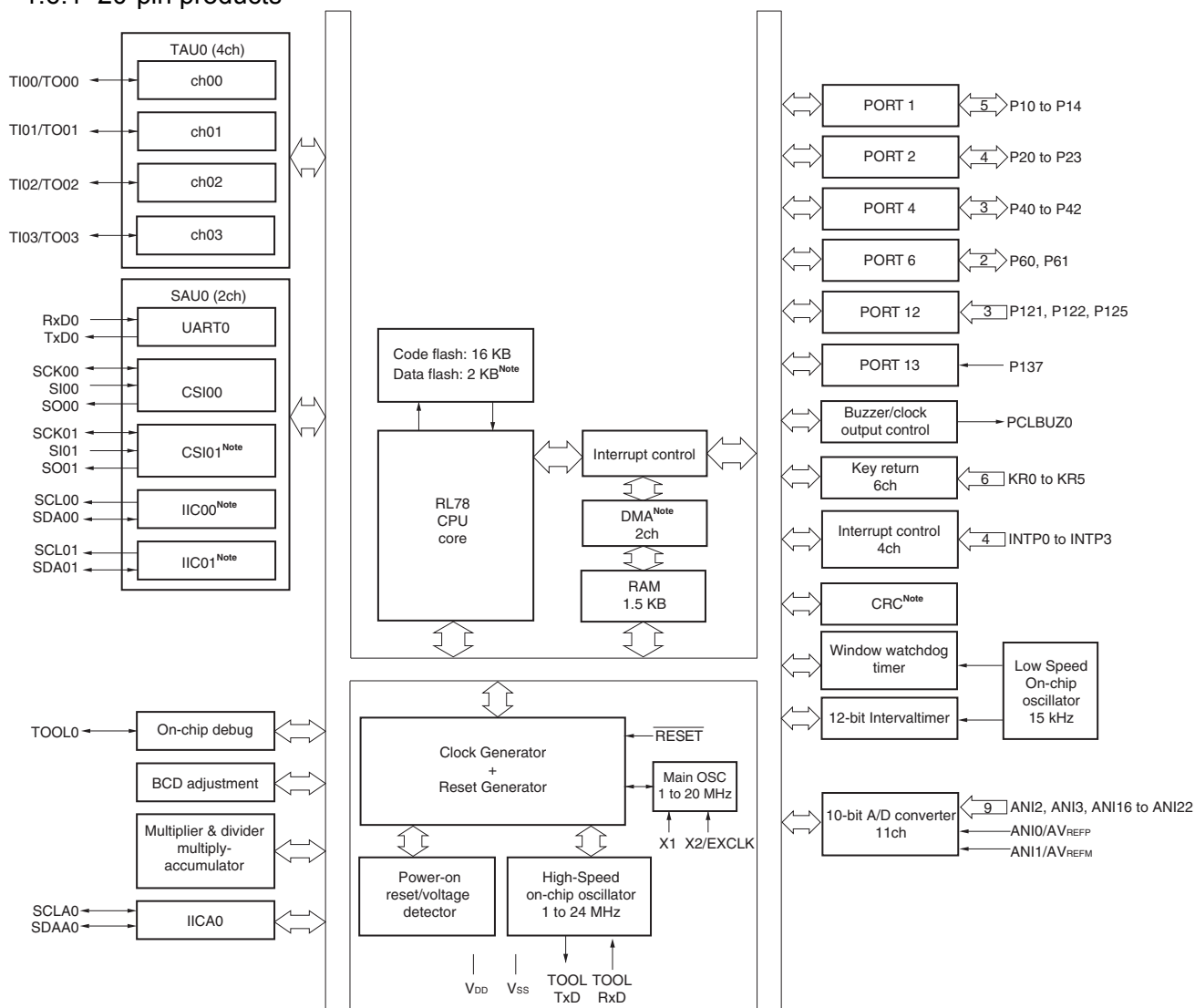
Note   Provided only in the R5F102 products.

1.6.3 30-pin products

TAU (8ch)
TI00 / TO00 — ch0
TI01/TO01 — ch1
TI02/TO02 — ch2
TI03/TO03 — ch3
(TI04/TO04) — ch4
(TI05/TO05) — ch5
(TI06/TO06) — ch6
(TI07/TO07) — ch7

SAU0 (4ch)
RxD0 / TxD0 — UART0
RxD1 / TxD1 — UART1[Note]
SCK00 / SI00 / SO00 — CSI00
SCK11 / SI11 / SO11 — CSI11[Note]
SCL00 / SDA00 — IIC00[Note]
SCL11 / SDA11 — IIC11[Note]

SAU0 (2ch)[Note]
RxD2 / TxD2 — UART2
SCK20 / SI20 / SO20 — CSI20
SCL20 / SDA20 — IIC20

TOOL0 — On-chip debug

BCD adjustment

Multiplier & divider/ multiply-accumulator

SCLA0 / SDAA0 — IICA0

Code flash: 16 KB
Data flash: 2 KB[Note]

RL78 CPU core

Interrupt control

DMA[Note] 2ch

RAM 2 KB

Clock Generator + Reset Generator — RESET

Main OSC 1 to 20 MHz — X1 X2/EXCLK

Poer-on reset/voltage detector

High-Speed On-chip oscillator 1 to 24 MHz

V_{DD} V_{SS} TOOL TxD TOOL RxD

Port 0 — 2 — P00, P01
Port 1 — 8 — P10 to P17
Port 2 — 4 — P20 to P23
Port 3 — 2 — P30, P31
Port 4 — P40
Port 5 — 2 — P50, P51
Port 6 — 2 — P60, P61
Port 12 — P120, 2 — P121, P122
Port 13 — P137
Port 14 — P147
Buzzer/clock output control — 2 — PCLBUZ0, PCLBUZ1
Interrupt control 6ch — 6 — INTP0 to INTP5
CRC[Note]
Window watchdog timer
12-bit Interval timer
Low Speed On-chip oscillator 15 KHz
10-bit A/D converter 8ch — 6 — ANI2, ANI3, ANI16 to ANI19, ANI0/AV$_{REFP}$, ANI1/AV$_{REFM}$
VOLTAGE REGULATOR — REGC

Note Provided only in the R5F102 products.

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

(T_A = −40 to +85°C, 1.8 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V) **(4/4)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL1}	20-, 24-pin products: P00 to P03**Note**, P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	4.0 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 20.0 mA			1.3	V
			4.0 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P23	I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60, P61	4.0 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 15.0 mA			2.0	V
			4.0 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 5.0 mA			0.4	V
			2.7 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 3.0 mA			0.4	V
			1.8 V $\leq$ V_{DD} $\leq$ 5.5 V, I_{OL1} = 2.0 mA			0.4	V
Input leakage current, high	I_{LIH1}	Other than P121, P122	V_I = V_{DD}			1	μA
	I_{LIH2}	P121, P122 (X1, X2/EXCLK)	V_I = V_{DD} / Input port or external clock input			1	μA
			When resonator connected			10	μA
Input leakage current, low	I_{LIL1}	Other than P121, P122	V_I = V_{SS}			−1	μA
	I_{LIL2}	P121, P122 (X1, X2/EXCLK)	V_I = V_{SS} / Input port or external clock input			−1	μA
			When resonator connected			−10	μA
On-chip pull-up resistance	R_U	20-, 24-pin products: P00 to P03**Note**, P10 to P14, P40 to P42, P125, $\overline{\text{RESET}}$ 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	V_I = V_{SS}, input port	10	20	100	kΩ

Note   24-pin products only.

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3) Peripheral functions (Common to all products)

(TA = −40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed onchip oscillator operating current	I_{FIL} [Note 1]				0.20		μA
12-bit interval timer operating current	I_{TMKA} [Notes 1, 2, 3]				0.02		μA
Watchdog timer operating current	I_{WDT} [Notes 1, 2, 4]	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} [Notes 1, 5]	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.30	1.70	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.50	0.70	mA
A/D converter reference voltage operating current	I_{ADREF} [Note 1]				75.0		μA
Temperature sensor operating current	I_{TMPS} [Note 1]				75.0		μA
LVD operating current	I_{LVD} [Notes 1, 6]				0.08		μA
Self-programming operating current	I_{FSP} [Notes 1, 8]				2.00	12.20	mA
BGO operating current	I_{BGO} [Notes 1, 7]				2.00	12.20	mA
SNOOZE operating current	I_{SNOZ} [Note 1]	ADC operation	The mode is performed [Note 9]		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to the V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{FIL} and I_{TMKA} when the 12-bit interval timer operates.

4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

6. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.

7. Current flowing only during data flash rewrite.

8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.

Remarks 1. f_{IL}:   Low-speed on-chip oscillator clock frequency

2. Temperature condition of the TYP. value is TA = 25°C

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time [Note4]	t$_{KCY2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	20 MHz < f$_{MCK}$	8/f$_{MCK}$		−		ns
			f$_{MCK}$ ≤ 20 MHz	6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V	16 MHz < f$_{MCK}$	8/f$_{MCK}$		−		ns
			f$_{MCK}$ ≤ 16 MHz	6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		6/f$_{MCK}$ and 750		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2−7		t$_{KCY2}$/2−7		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2−8		t$_{KCY2}$/2−8		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2−18		t$_{KCY2}$/2−18		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		t$_{KCY2}$/2−18		ns
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK2}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$ + 20		1/f$_{MCK}$ + 30		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		1/f$_{MCK}$ + 30		ns
SIp hold time (from SCKp↑) [Note 2]	t$_{KSI2}$			1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns
Delay time from SCKp↓ to SOp output [Note 3]	t$_{KSO2}$	C = 30 pF [Note4]	2.7 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{MCK}$ + 44		2/f$_{MCK}$ + 110	ns
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{MCK}$ + 75		2/f$_{MCK}$ + 110	ns
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		2/f$_{MCK}$ + 110	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

RENESAS

Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products.)

2. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products.))

(5) During communication at same potential (simplified I²C mode)
(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode LS (low-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ		400 [Note 1]	kHz
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ		300 [Note 1]	kHz
Hold time when SCLr = "L"	t$_{LOW}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1150		ns
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1550		ns
Hold time when SCLr = "H"	t$_{HIGH}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1150		ns
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1550		ns
Data setup time (reception)	t$_{SU:DAT}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1/f$_{MCK}$ + 145 [Note 2]		ns
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1/f$_{MCK}$ + 230 [Note 2]		ns
Data hold time (transmission)	t$_{HD:DAT}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	0	355	ns
		1.8 V ≤ V$_{DD}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	0	405	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

2. Set t$_{SU:DAT}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

Caution Select the N-ch open drain output (V$_{DD}$ tolerance) mode for SDAr by using port output mode register h (POMh).

(**Remarks** are listed on the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(TA = −40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time [Note 1]	t_{KCY2}	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	20 MHz < fMCK ≤ 24 MHz	12/fMCK		–		ns
			8 MHz < fMCK ≤ 20 MHz	10/fMCK		–		ns
			4 MHz < fMCK ≤ 8 MHz	8/fMCK		16/fMCK		ns
			fMCK ≤ 4 MHz	6/fMCK		10/fMCK		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	20 MHz < fMCK ≤ 24 MHz	16/fMCK		–		ns
			16 MHz < fMCK ≤ 20 MHz	14/fMCK		–		ns
			8 MHz < fMCK ≤ 16 MHz	12/fMCK		–		ns
			4 MHz < fMCK ≤ 8 MHz	8/fMCK		16/fMCK		ns
			fMCK ≤ 4 MHz	6/fMCK		10/fMCK		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V [Note 2]	20 MHz < fMCK ≤ 24 MHz	36/fMCK		–		ns
			16 MHz < fMCK ≤ 20 MHz	32/fMCK		–		ns
			8 MHz < fMCK ≤ 16 MHz	26/fMCK		–		ns
			4 MHz < fMCK ≤ 8 MHz	16/fMCK		16/fMCK		ns
			fMCK ≤ 4 MHz	10/fMCK		10/fMCK		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		t_{KCY2}/2 − 12		t_{KCY2}/2 − 50		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		t_{KCY2}/2 − 18		t_{KCY2}/2 − 50		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V [Note 2]		t_{KCY2}/2 − 50		t_{KCY2}/2 − 50		ns
SIp setup time (to SCKp↑) [Note 3]	t_{SIK2}	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ VDD ≤ 4.0 V		1/fMCK + 20		1/fMCK + 30		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		1/fMCK + 20		1/fMCK + 30		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ VDD ≤ 2.0 V [Note 2]		1/fMCK + 30		1/fMCK + 30		ns
SIp hold time (from SCKp↑) [Note 4]	t_{KSI2}			1/fMCK + 31		1/fMCK + 31		ns
Delay time from SCKp↓ to SOp output [Note 5]	t_{KSO2}	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ			2/fMCK + 120		2/fMCK + 573	ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ			2/fMCK + 214		2/fMCK + 573	ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V [Note 2], Cb = 30 pF, Rb = 5.5 kΩ			2/fMCK + 573		2/fMCK + 573	ns

Notes 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

    2. Use it with VDD ≥ Vb.

    3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Cautions 1. Select the TTL input buffer for the SIp and SCKp pins and the N-ch open drain output (VDD tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For VIH and VIL, see the DC characteristics with TTL input buffer selected.**

    2. CSI01 and CSI11 cannot communicate at different potential.

2.5.2 Serial interface IICA

(TA = −40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode LS (low-speed main) mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: $f_{CLK} \geq 3.5$ MHz			0	400	kHz
		Normal mode: $f_{CLK} \geq 1$ MHz	0	100			kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		0.6		μs
Hold time[Note 1]	$t_{HD:STA}$		4.0		0.6		μs
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		μs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		μs
Bus-free time	t_{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

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2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

　　　Normal mode:　　$C_b = 400$ pF, $R_b = 2.7$ kΩ
　　　Fast mode:　　　$C_b = 320$ pF, $R_b = 1.1$ kΩ

IICA serial transfer timing
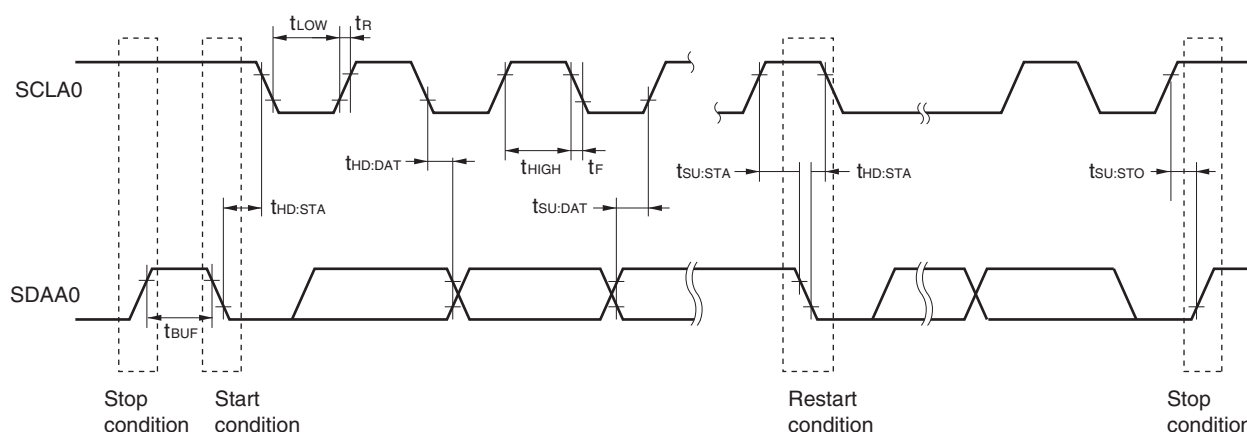
(3) When reference voltage (+) = V$_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (−) = V$_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = V$_{DD}$, Reference voltage (−) = V$_{SS}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution			1.2	±7.0	LSB
					1.2	±10.5 [Note 3]	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
				57		95	μs
Conversion time	t$_{CONV}$	10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution				±0.60	%FSR
						±0.85 [Note 3]	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution				±0.60	%FSR
						±0.85 [Note 3]	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution				±4.0	LSB
						±6.5 [Note 3]	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution				±2.0	LSB
						±2.5 [Note 3]	LSB
Analog input voltage	V$_{AIN}$	ANI0 to ANI3, ANI16 to ANI22		0		V$_{DD}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)		V$_{BGR}$ [Note 4]			V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)		V$_{TMPS25}$ [Note 4]			V

Notes 1. Excludes quantization error (±1/2 LSB).

    2. This value is indicated as a ratio (%FSR) to the full-scale value.

    3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

    4. Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (−) = AV$_{REFM}$ (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22

(T$_A$ = −40 to +85°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = V$_{BGR}$ $^{Note\ 3}$, Reference voltage (−) = AV$_{REFM}$ $^{Note\ 4}$= 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$			8		bit
Conversion time	t$_{CONV}$	8-bit resolution	17		39	μs
Zero-scale error[1,2]	EZS	8-bit resolution			±0.60	%FSR
Integral linearity error[1]	ILE	8-bit resolution			±2.0	LSB
Differential linearity error[1]	DLE	8-bit resolution			±1.0	LSB
Analog input voltage	V$_{AIN}$		0		V$_{BGR}$ [3]	V

Notes 1. Excludes quantization error (±1/2 LSB).
      2. This value is indicated as a ratio (%FSR) to the full-scale value.
      3. Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.
      4. When reference voltage (−) = V$_{SS}$, the MAX. values are as follows.
           Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AV$_{REFM}$.
           Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.
           Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

2.6.2 Temperature sensor/internal reference voltage characteristics

(T$_A$ = −40 to +85°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V$_{TMPS25}$	Setting ADS register = 80H, T$_A$ = +25°C		1.05		V
Internal reference voltage	V$_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F$_{VTMPS}$	Temperature sensor output voltage that depends on the temperature		−3.6		mV/°C
Operation stabilization wait time	t$_{AMP}$		5			μs

2.6.3 POR circuit characteristics

(T$_A$ = −40 to +85°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V$_{POR}$	Power supply rise time	1.47	1.51	1.55	V
	V$_{PDR}$	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width [Note]	T$_{PW}$		300			μs

Note Minimum time required for a POR reset when V$_{DD}$ exceeds below V$_{PDR}$. This is also the minimum time required for a POR reset from when V$_{DD}$ exceeds below 0.7 V to when V$_{DD}$ exceeds V$_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).

TI/TO Timing

TI00 to TI07

t_{TIL} t_{TIH}

TO00 to TO07

$1/f_{TO}$
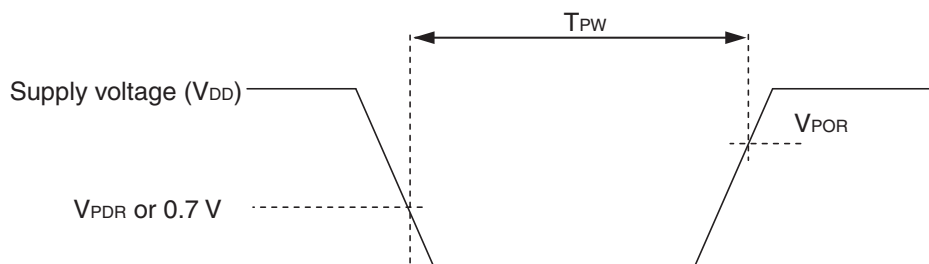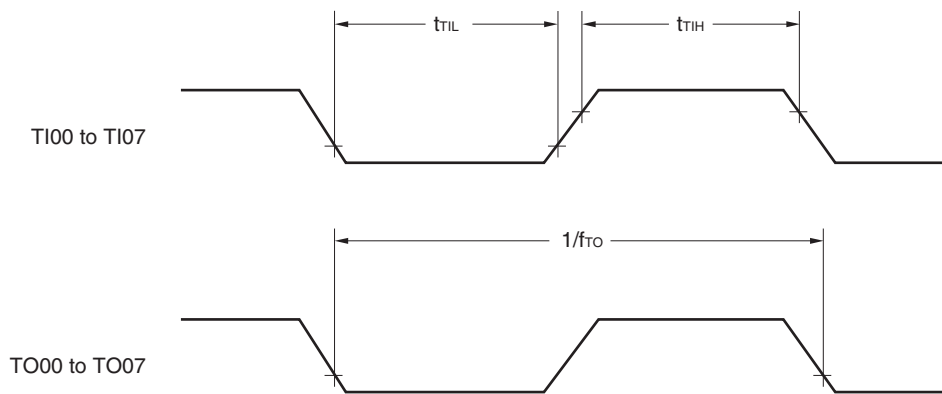
Interrupt Request Input Timing

INTP0 to INTP5

t_{INTL} t_{INTH}
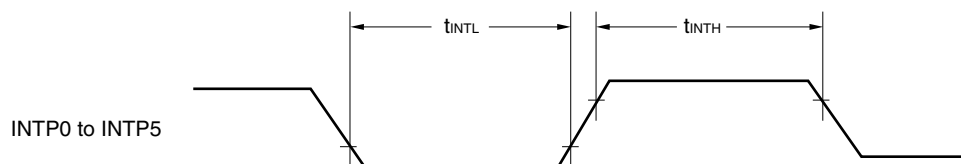
Key Interrupt Input Timing

KR0 to KR9

t_{KR}
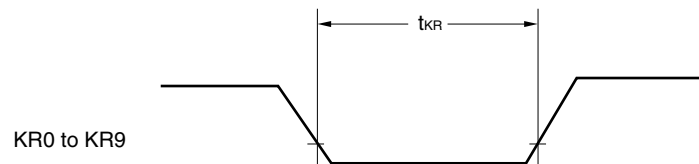
$\overline{\text{RESET}}$ Input Timing

$\overline{\text{RESET}}$

t_{RSL}
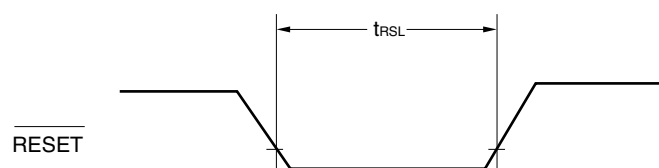
(4) During communication at same potential (simplified I^{2}C mode)
(T_A = −40 to +105°C, 2.4 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	C_b = 100 pF, R_b = 3 kΩ		100 $^{Note\ 1}$	kHz
Hold time when SCLr = "L"	t_{LOW}	C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 580 $^{Note\ 2}$		ns
Data hold time (transmission)	$t_{HD:DAT}$	C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.
2. Set $t_{SU:DAT}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

Caution Select the N-ch open drain output (V_{DD} tolerance) mode for SDAr by using port output mode register h (POMh).

Simplified I^{2}C mode connection diagram (during communication at same potential)
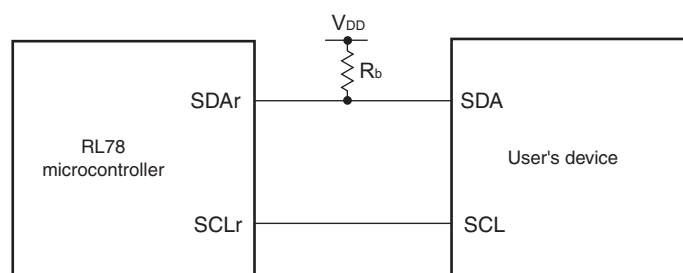
Simplified I^{2}C mode serial transfer timing (during communication at same potential)
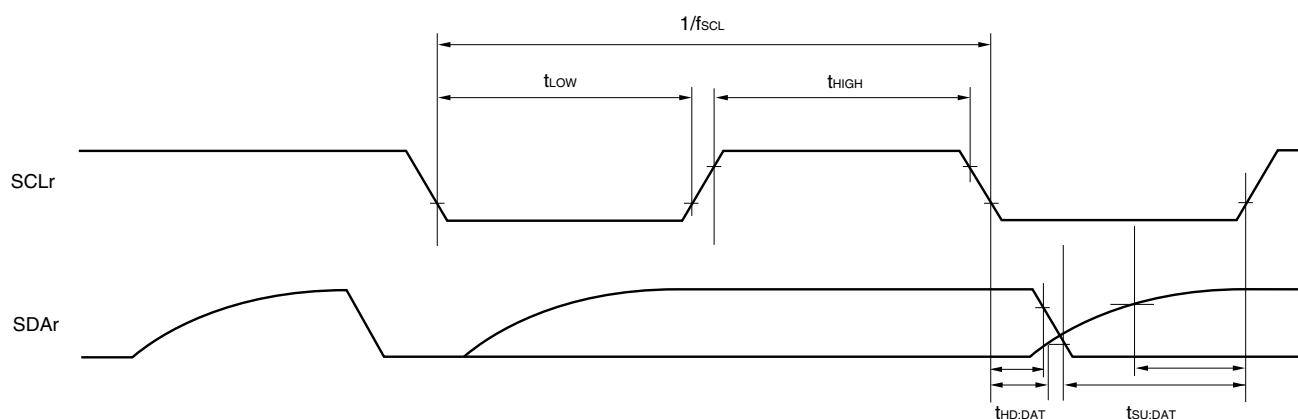
Remarks 1. R_b [Ω]:Communication line (SDAr) pull-up resistance
C_b [F]: Communication line (SCLr, SDAr) load capacitance
2. r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1, 4, 5)
3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0, 1), n: Channel number (0, 1, 3))

CSI mode connection diagram (during communication at different potential)
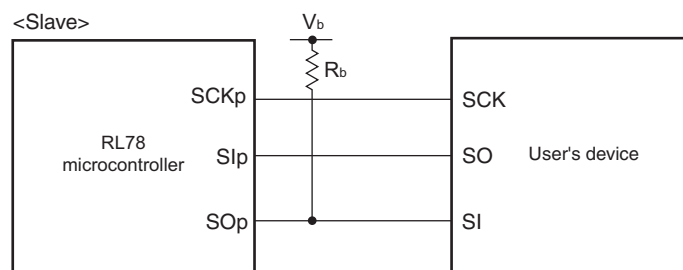
CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
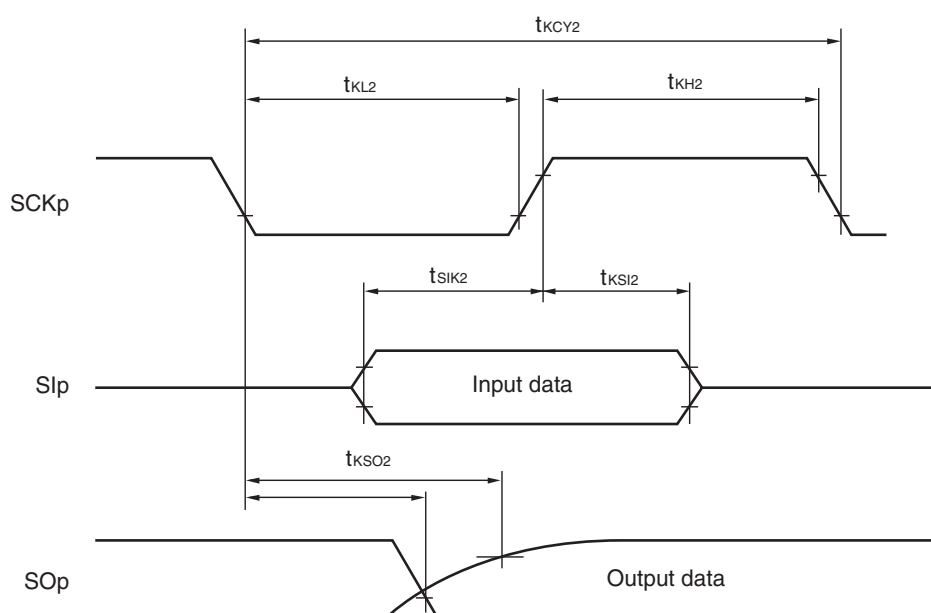
Remarks 1. R$_b$ [Ω]: Communication line (SOp) pull-up resistance, C$_b$ [F]: Communication line (SOp) load capacitance, V$_b$ [V]: Communication line voltage

   2. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

   3. f$_{MCK}$: Serial array unit operation clock frequency
   (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn))

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (−) = AV$_{REFM}$ (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = V$_{BGR}$ [Note 3], Reference voltage (−) = AV$_{REFM}$ [Note 4] = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$			8		bit
Conversion time	t$_{CONV}$	8-bit resolution	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	8-bit resolution			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution			±1.0	LSB
Analog input voltage	V$_{AIN}$		0		V$_{BGR}$ [Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).

     2. This value is indicated as a ratio (%FSR) to the full-scale value.

     3. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

     4. When reference voltage (−) = V$_{SS}$, the MAX. values are as follows.

        Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AV$_{REFM}$.

        Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

        Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

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3.9 Dedicated Flash Memory Programmer Communication (UART)

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.10 Timing of Entry to Flash Memory Programming Modes

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t$_{SUINIT}$	POR and LVD reset are released before external release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t$_{SU}$	POR and LVD reset are released before external release	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t$_{HD}$	POR and LVD reset are released before external release	1			ms
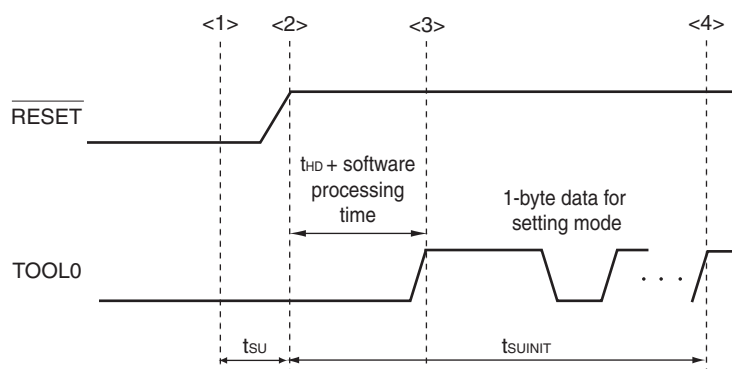
<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t$_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

        t$_{SU}$: Time to release the external reset after the TOOL0 pin is set to the low level

        t$_{HD}$: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

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4.2 24-pin products

R5F1027AANA, R5F10279ANA, R5F10278ANA, R5F10277ANA
R5F1037AANA, R5F10379ANA, R5F10378ANA, R5F10377ANA
R5F1027ADNA, R5F10279DNA, R5F10278DNA, R5F10277DNA
R5F1037ADNA, R5F10379DNA, R5F10378DNA, R5F10377DNA
<R>   R5F1027AGNA, R5F10279GNA, R5F10278GNA, R5F10277GNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN24-4x4-0.50	PWQN0024KE-A	P24K8-50-CAB-1	0.04

DETAIL OF Ⓐ PART

(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.05
E	4.00±0.05
A	0.75±0.05
b	0.25 $^{+0.05}_{-0.07}$
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

EXPOSED DIE PAD

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	2.45	2.50	2.55	2.45	2.50	2.55

Rev.	Date	Description	
		Page	**Summary**
1.00	Dec 10, 2012	-	First Edition issued
2.00	Sep 06, 2013	1	Modification of 1.1 Features
		3	Modification of 1.2 List of Part Numbers
		4	Modification of Table 1-1. List of Ordering Part Numbers, Note, and Caution
		7 to 9	Modification of package name in 1.4.1 to 1.4.3
		14	Modification of tables in 1.7 Outline of Functions
		17	Modification of description of table in 2.1 Absolute Maximum Ratings ($T_A = 25°C$)
		18	Modification of table, Note, and Caution in 2.2.1 X1 oscillator characteristics
		18	Modification of table in 2.2.2 On-chip oscillator characteristics
		19	Modification of Note 3 in 2.3.1 Pin characteristics (1/4)
		20	Modification of Note 3 in 2.3.1 Pin characteristics (2/4)
		23	Modification of Notes 1 and 2 in (1) 20-, 24-pin products (1/2)
		24	Modification of Notes 1 and 3 in (1) 20-, 24-pin products (2/2)
		25	Modification of Notes 1 and 2 in (2) 30-pin products (1/2)
		26	Modification of Notes 1 and 3 in (2) 30-pin products (2/2)
		27	Modification of (3) Peripheral functions (Common to all products)
		28	Modification of table in 2.4 AC Characteristics
		29	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		30	Modification of figures of AC Timing Test Point and External Main System Clock Timing
		31	Modification of figure of AC Timing Test Point
		31	Modification of description and Note 2 in (1) During communication at same potential (UART mode)
		32	Modification of description in (2) During communication at same potential (CSI mode)
		33	Modification of description in (3) During communication at same potential (CSI mode)
		34	Modification of description in (4) During communication at same potential (CSI mode)
		36	Modification of table and Note 2 in (5) During communication at same potential (simplified I^2C mode)
		38, 39	Modification of table and Notes 1 to 9 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)
		40	Modification of Remarks 1 to 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)
		41	Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode)
		42	Modification of Caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode)
		43	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		44	Modification of table and Notes 1 and 2 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		45	Modification of table, Note 1, and Caution 1 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		47	Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode)
		50	Modification of table, Note 1, and Caution 1 in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode)
		52	Modification of Remark in 2.5.2 Serial interface IICA
		53	Addition of table to 2.6.1 A/D converter characteristics
		53	Modification of description in 2.6.1 (1)
		54	Modification of Notes 3 to 5 in 2.6.1 (1)
		54	Modification of description and Notes 2 to 4 in 2.6.1 (2)

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