## What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

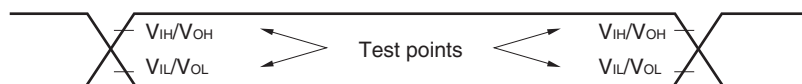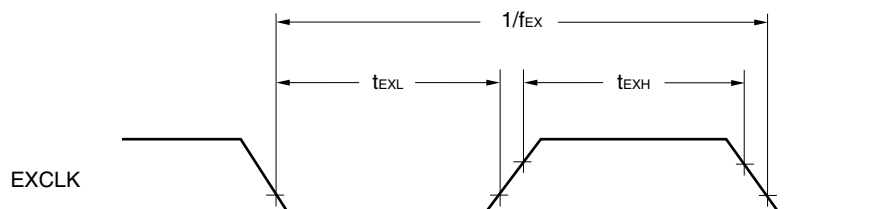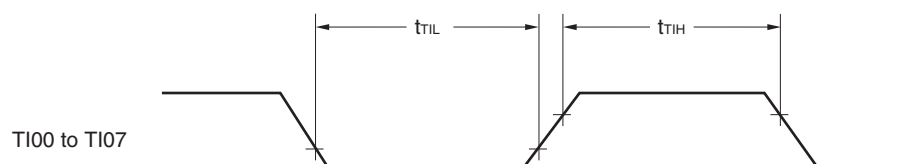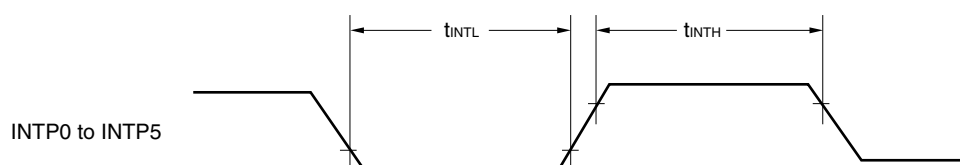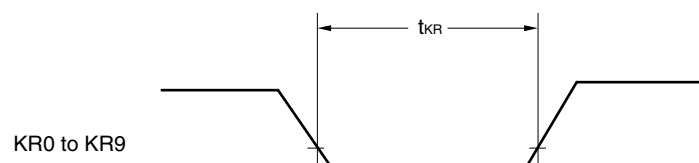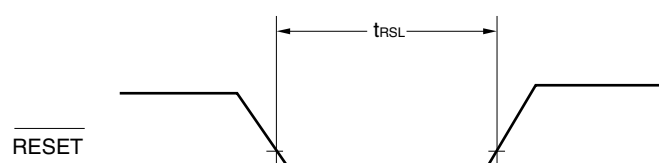| Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1036adsp-v0

1.6.3 30-pin products
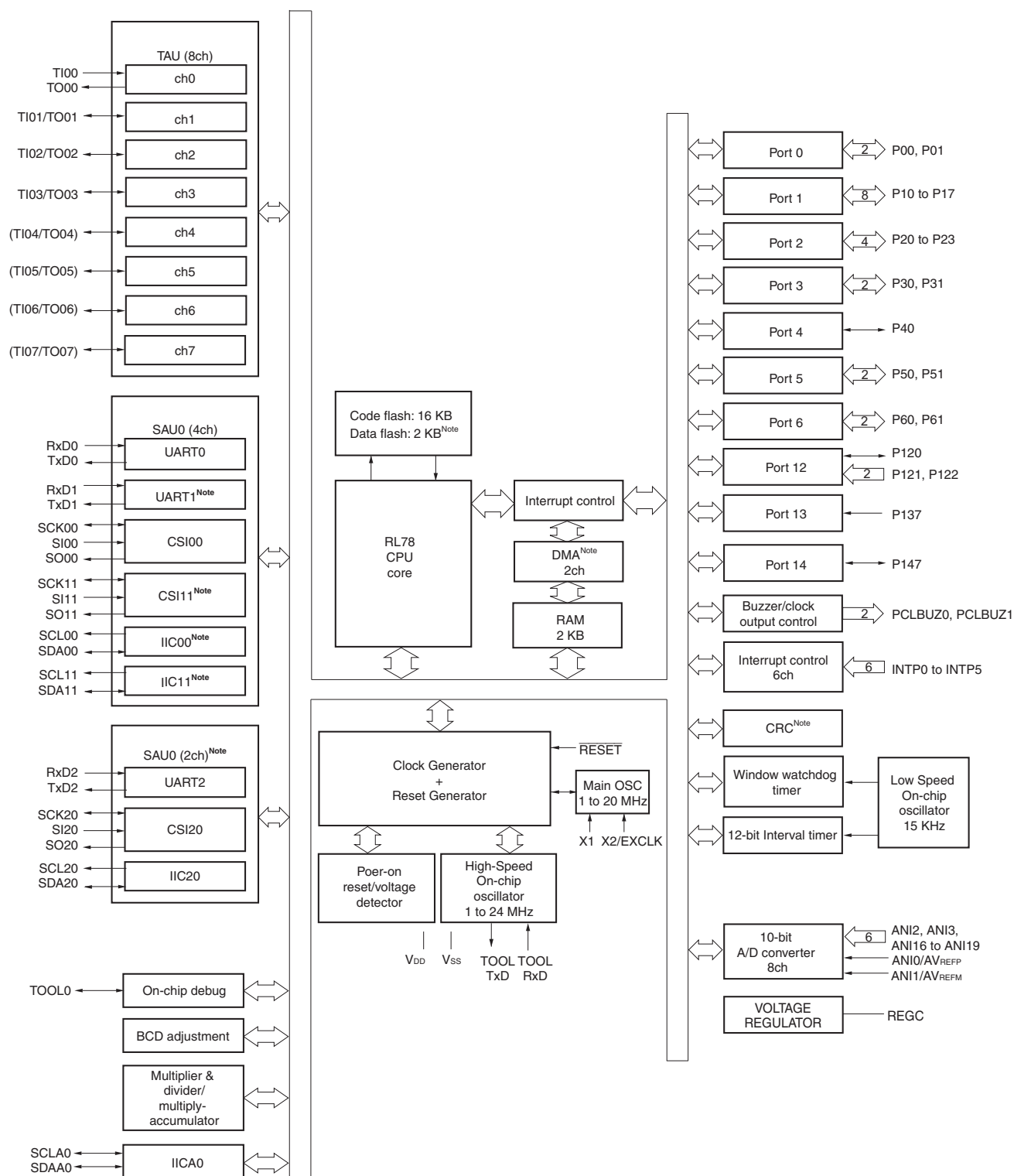
Note   Provided only in the R5F102 products.

Remark   Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V) **(4/4)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V$_{OL1}$	20-, 24-pin products: P00 to P03**Note**, P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 20.0 mA			1.3	V
			4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 8.5 mA			0.7	V
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 3.0 mA			0.6	V
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 1.5 mA			0.4	V
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 0.6 mA			0.4	V
	V$_{OL2}$	P20 to P23	I$_{OL2}$ = 400 μA			0.4	V
	V$_{OL3}$	P60, P61	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 15.0 mA			2.0	V
			4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 5.0 mA			0.4	V
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 3.0 mA			0.4	V
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 2.0 mA			0.4	V
Input leakage current, high	I$_{LIH1}$	Other than P121, P122	V$_I$ = V$_{DD}$			1	μA
	I$_{LIH2}$	P121, P122 (X1, X2/EXCLK)	V$_I$ = V$_{DD}$	Input port or external clock input			1	μA
				When resonator connected			10	μA
Input leakage current, low	I$_{LIL1}$	Other than P121, P122	V$_I$ = V$_{SS}$			−1	μA
	I$_{LIL2}$	P121, P122 (X1, X2/EXCLK)	V$_I$ = V$_{SS}$	Input port or external clock input			−1	μA
				When resonator connected			−10	μA
On-chip pull-up resistance	R$_U$	20-, 24-pin products: P00 to P03**Note**, P10 to P14, P40 to P42, P125, $\overline{RESET}$ 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	V$_I$ = V$_{SS}$, input port	10	20	100	kΩ

Note   24-pin products only.

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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AC Timing Test Point

V$_{IH}$/V$_{OH}$ Test points   V$_{IH}$/V$_{OH}$
V$_{IL}$/V$_{OL}$ V$_{IL}$/V$_{OL}$

External Main System Clock Timing

1/f$_{EX}$

t$_{EXL}$ t$_{EXH}$

EXCLK

TI/TO Timing

t$_{TIL}$ t$_{TIH}$

TI00 to TI07

1/f$_{TO}$

TO00 to TO07

Interrupt Request Input Timing

t$_{INTL}$ t$_{INTH}$

INTP0 to INTP5

Key Interrupt Input Timing

t$_{KR}$

KR0 to KR9

$\overline{\text{RESET}}$ Input Timing

t$_{RSL}$

$\overline{\text{RESET}}$

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time [Note4]	t$_{KCY2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	20 MHz < f$_{MCK}$	8/f$_{MCK}$		−		ns
			f$_{MCK}$ ≤ 20 MHz	6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V	16 MHz < f$_{MCK}$	8/f$_{MCK}$		−		ns
			f$_{MCK}$ ≤ 16 MHz	6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		6/f$_{MCK}$ and 750		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2−7		t$_{KCY2}$/2−7		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2−8		t$_{KCY2}$/2−8		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2−18		t$_{KCY2}$/2−18		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		t$_{KCY2}$/2−18		ns
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK2}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$ + 20		1/f$_{MCK}$ + 30		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		1/f$_{MCK}$ + 30		ns
SIp hold time (from SCKp↑) [Note 2]	t$_{KSI2}$			1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns
Delay time from SCKp↓ to SOp output [Note 3]	t$_{KSO2}$	C = 30 pF [Note4]	2.7 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{MCK}$ + 44		2/f$_{MCK}$ + 110	ns
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{MCK}$ + 75		2/f$_{MCK}$ + 110	ns
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V		−		2/f$_{MCK}$ + 110	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

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5. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 4** above to calculate the maximum transfer rate under conditions of the customer.

6. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V$_{DD}$ < 4.0 V and 2.3 V ≤ V$_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

8. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

9. This value as an example is calculated when the conditions described in the "Conditions" column are   met. Refer to **Note 8** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). **For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

2.6.2 Temperature sensor/internal reference voltage characteristics

(T$_A$ = −40 to +85°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V$_{TMPS25}$	Setting ADS register = 80H, T$_A$ = +25°C		1.05		V
Internal reference voltage	V$_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F$_{VTMPS}$	Temperature sensor output voltage that depends on the temperature		−3.6		mV/°C
Operation stabilization wait time	t$_{AMP}$		5			μs

2.6.3 POR circuit characteristics

(T$_A$ = −40 to +85°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V$_{POR}$	Power supply rise time	1.47	1.51	1.55	V
	V$_{PDR}$	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width [Note]	T$_{PW}$		300			μs

Note Minimum time required for a POR reset when V$_{DD}$ exceeds below V$_{PDR}$. This is also the minimum time required for a POR reset from when V$_{DD}$ exceeds below 0.7 V to when V$_{DD}$ exceeds V$_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).
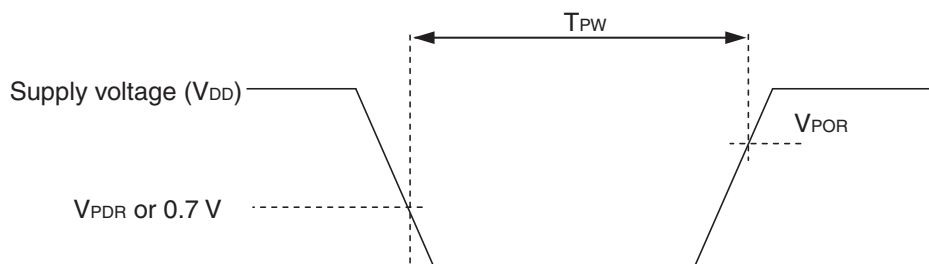
3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T$_A$ = 25°C)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V$_{DD}$			−0.5 to + 6.5	V
REGC terminal input voltage[Note1]	V$_{IREGC}$	REGC		−0.3 to +2.8 and −0.3 to V$_{DD}$ + 0.3 [Note 2]	V
Input Voltage	V$_{I1}$	Other than P60, P61		−0.3 to V$_{DD}$ + 0.3[Note 3]	V
	V$_{I2}$	P60, P61 (N-ch open drain)		−0.3 to 6.5	V
Output Voltage	V$_O$			−0.3 to V$_{DD}$ + 0.3[Note 3]	V
Analog input voltage	V$_{AI}$	20, 24-pin products: ANI0 to ANI3, ANI16 to ANI22 30-pin products: ANI0 to ANI3, ANI16 to ANI19		−0.3 to V$_{DD}$ + 0.3 and −0.3 to AVREF(+)+0.3[Notes 3, 4]	V
Output current, high	I$_{OH1}$	Per pin	Other than P20 to P23	−40	mA
		Total of all pins	All the terminals other than P20 to P23	−170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	−70	mA
			20-, 24-pin products: P00 to P03[Note 5], P10 to P14 30-pin products: P10 to P17, P30, P31, P50, P51, P147	−100	mA
	I$_{OH2}$	Per pin	P20 to P23	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I$_{OL1}$	Per pin	Other than P20 to P23	40	mA
		Total of all pins	All the terminals other than P20 to P23	170	mA
			20-, 24-pin products: P40 to P42 30-pin products: P00, P01, P40, P120	70	mA
			20-, 24-pin products: P00 to P03 [Note 5], P10 to P14, P60, P61 30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147	100	mA
	I$_{OL2}$	Per pin	P20 to P23	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T$_A$			−40 to +105	°C
Storage temperature	T$_{stg}$			−65 to +150	°C

Notes 1. 30-pin product only.
   2. Connect the REGC pin to V$_{SS}$ via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.
   3. Must be 6.5 V or lower.
   4. Do not exceed AV$_{REF}$(+) + 0.3 V in case of A/D conversion target pin.
   5. 24-pin products only.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
   2. AV$_{REF}$(+) : + side reference voltage of the A/D converter.
   3. V$_{SS}$: Reference voltage

3.2 Oscillator Characteristics

3.2.1 X1 oscillator characteristics

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f$_X$)[Note]	Ceramic resonator / crystal oscillator	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V	1.0		8.0	

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **5.4 System Clock Oscillator**.

3.2.2 On-chip oscillator characteristics

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency [Notes 1, 2]	f$_{IH}$			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		R5F102 products	T$_A$ = −20 to +85°C	-1.0		+1.0	%
			T$_A$ = −40 to −20°C	-1.5		+1.5	%
			T$_A$ = +85 to +105°C	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f$_{IL}$				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, Vss = 0 V) (1/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I$_{OH1}$	20-, 24-pin products: Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42 30-pin products: Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147				−3.0 Note 2	mA
		20-, 24-pin products: Total of P40 to P42 30-pin products: Total of P00, P01, P40, P120 (When duty ≤ 70%[Note 3])	4.0 V ≤ V$_{DD}$ ≤ 5.5 V			−9.0	mA
			2.7 V ≤ V$_{DD}$ < 4.0 V			−6.0	mA
			2.4 V ≤ V$_{DD}$ < 2.7 V			−4.5	mA
		20-, 24-pin products: Total of P00 to P03[Note 4], P10 to P14 30-pin products: Total of P10 to P17, P30, P31, P50, P51, P147 (When duty ≤ 70%[Note 3])	4.0 V ≤ V$_{DD}$ ≤ 5.5 V			−27.0	mA
			2.7 V ≤ V$_{DD}$ < 4.0 V			−18.0	mA
			2.4 V ≤ V$_{DD}$ < 2.7 V			−10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				−36.0	mA
	I$_{OH2}$	Per pin for P20 to P23				−0.1	mA
		Total of all pins				−0.4	mA

Notes 1. value of current at which the device operation is guaranteed even if the current flows from the V$_{DD}$ pin to an output pin.

2. However, do not exceed the total current value.

3. The output current value under conditions where the duty factor ≤ 70%.
If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).
- Total output current of pins = (I$_{OH}$ × 0.7)/(n × 0.01)
  <Example> Where n = 80% and I$_{OH}$ = −10.0 mA
  Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ −8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. 24-pin products only.

Caution P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V) **(2/4)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I$_{OL1}$	20-, 24-pin products: Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42 30-pin products: Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147				8.5 Note 2	mA
		Per pin for P60, P61				15.0 Note 2	mA
		20-, 24-pin products: Total of P40 to P42 30-pin products: Total of P00, P01, P40, P120 (When duty ≤ 70%[Note 3])	4.0 V ≤ V$_{DD}$ ≤ 5.5 V			25.5	mA
			2.7 V ≤ V$_{DD}$ < 4.0 V			9.0	mA
			2.4 V ≤ V$_{DD}$ < 2.7 V			1.8	mA
		20-, 24-pin products: Total of P00 to P03[Note 4], P10 to P14, P60, P61 30-pin products: Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147 (When duty ≤ 70%[Note 3])	4.0 V ≤ V$_{DD}$ ≤ 5.5 V			40.0	mA
			2.7 V ≤ V$_{DD}$ < 4.0 V			27.0	mA
			2.4 V ≤ V$_{DD}$ < 2.7 V			5.4	mA
		Total of all pins (When duty ≤ 70%[Note 3])				65.5	mA
	I$_{OL2}$	Per pin for P20 to P23				0.4	mA
		Total of all pins				1.6	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V$_{SS}$ pin.

2. However, do not exceed the total current value.

3. The output current value under conditions where the duty factor ≤ 70%.

If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

• Total output current of pins = (I$_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and I$_{OL}$ = 10.0 mA

　　　　Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. 24-pin products only.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(1) 20-, 24-pin products

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I$_{DD1}$	Operating mode	HS (High-speed main) mode[Note 4]	f$_{IH}$ = 24 MHz[Note 3]	Basic operation	V$_{DD}$ = 5.0 V		1.5		mA
						V$_{DD}$ = 3.0 V		1.5		
					Normal operation	V$_{DD}$ = 5.0 V		3.3	5.3	mA
						V$_{DD}$ = 3.0 V		3.3	5.3	
				f$_{IH}$ = 16 MHz[Note 3]		V$_{DD}$ = 5.0 V		2.5	3.9	mA
						V$_{DD}$ = 3.0 V		2.5	3.9	
				f$_{MX}$ = 20 MHz[Note 2], V$_{DD}$ = 5.0 V		Square wave input		2.8	4.7	mA
						Resonator connection		3.0	4.8	
				f$_{MX}$ = 20 MHz[Note 2], V$_{DD}$ = 3.0 V		Square wave input		2.8	4.7	mA
						Resonator connection		3.0	4.8	
				f$_{MX}$ = 10 MHz[Note 2], V$_{DD}$ = 5.0 V		Square wave input		1.8	2.8	mA
						Resonator connection		1.8	2.8	
				f$_{MX}$ = 10 MHz[Note 2], V$_{DD}$ = 3.0 V		Square wave input		1.8	2.8	mA
						Resonator connection		1.8	2.8	

Notes 1. Total current flowing into V$_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$ or V$_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.

3. When high-speed system clock is stopped

4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V$_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz

V$_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T$_A$ = 25°C.

RENESAS

(2) 30-pin products

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)　　　　　　　　　　　　　　　　　　　　　　　　　　(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (High-speed main) mode[Note 6]	f$_{IH}$ = 24 MHz[Note 4]	V$_{DD}$ = 5.0 V		440	2300	μA
					V$_{DD}$ = 3.0 V		440	2300	
				f$_{IH}$ = 16 MHz[Note 4]	V$_{DD}$ = 5.0 V		400	1700	μA
					V$_{DD}$ = 3.0 V		400	1700	
				f$_{MX}$ = 20 MHz[Note 3], V$_{DD}$ = 5.0 V	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				f$_{MX}$ = 20 MHz[Note 3], V$_{DD}$ = 3.0 V	Square wave input		280	1900	μA
					Resonator connection		450	2000	
				f$_{MX}$ = 10 MHz[Note 3], V$_{DD}$ = 5.0 V	Square wave input		190	1020	μA
					Resonator connection		260	1100	
				f$_{MX}$ = 10 MHz[Note 3], V$_{DD}$ = 3.0 V	Square wave input		190	1020	μA
					Resonator connection		260	1100	
	I$_{DD3}$ [Note 5]	STOP mode	T$_A$ = −40°C				0.18	0.50	μA
			T$_A$ = +25°C				0.23	0.50	
			T$_A$ = +50°C				0.30	1.10	
			T$_A$ = +70°C				0.46	1.90	
			T$_A$ = +85°C				0.75	3.30	
			T$_A$ = +105°C				2.94	15.30	

Notes 1. Total current flowing into V$_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$ or V$_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator clock is stopped.

4. When high-speed system clock is stopped.

5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: V$_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
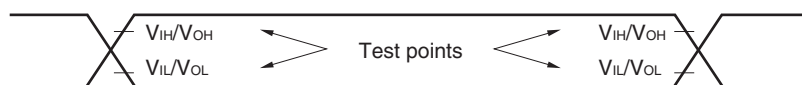
V$_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: high-speed on-chip oscillator clock frequency

3. Except STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C.

3.5 Peripheral Functions Characteristics

AC Timing Test Point

3.5.1 Serial array unit

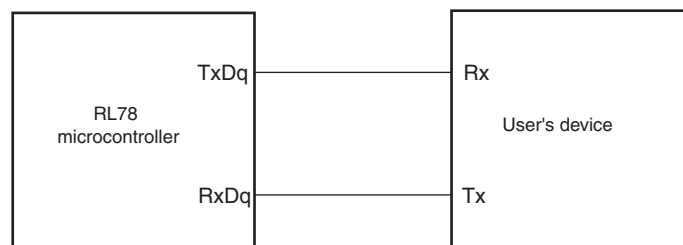**(1) During communication at same potential (UART mode)**

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

| Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate Note 1					f$_{MCK}$/12	bps
		Theoretical value of the maximum transfer rate f$_{CLK}$ = f$_{MCK}$Note2			2.0	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f$_{CLK}$) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ V$_{DD}$ ≤ 5.5 V)

16 MHz (2.4 V ≤ V$_{DD}$ ≤ 5.5 V)

Caution   Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)


**UART mode bit width (during communication at same potential) (reference)**
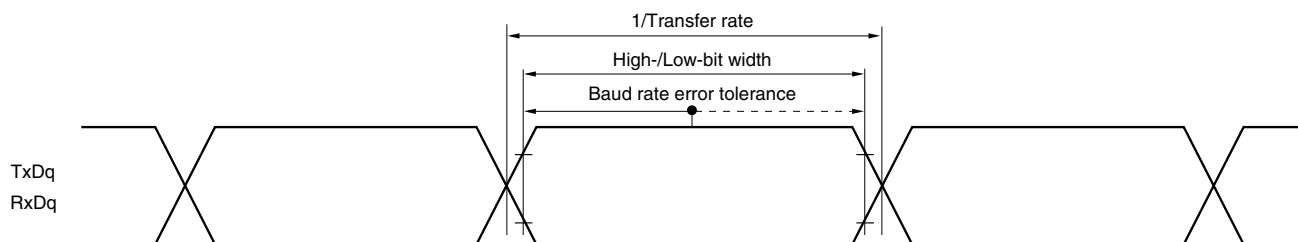
Remarks 1. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

2. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
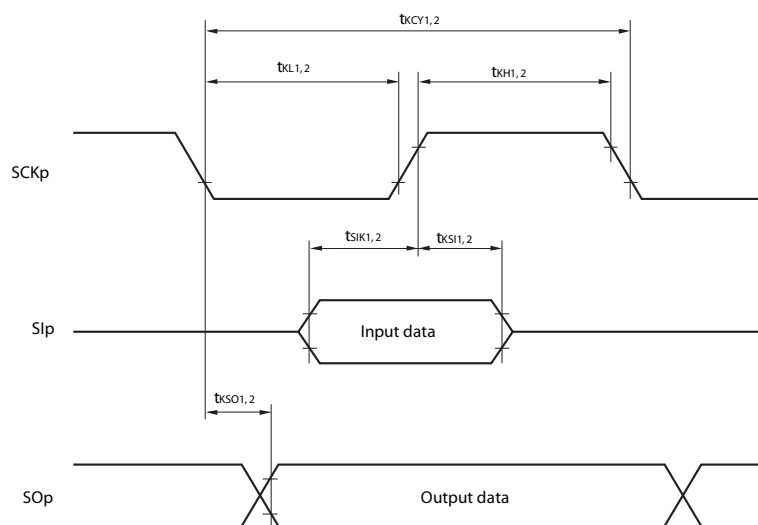
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
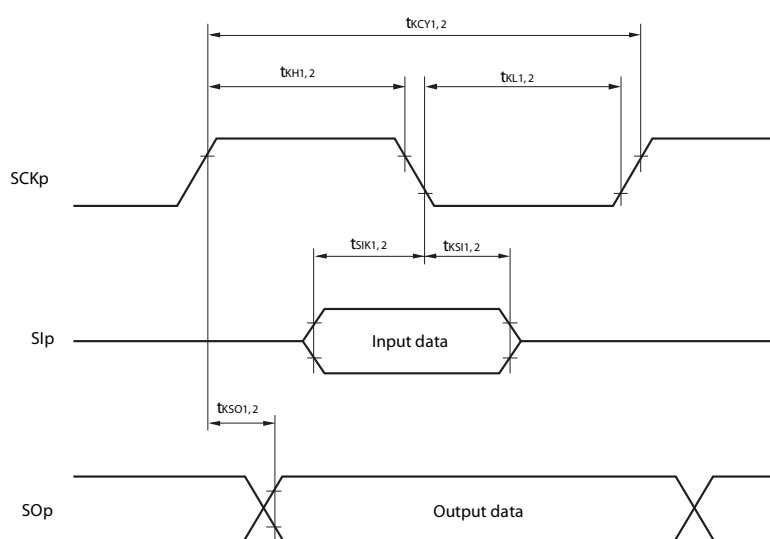
Remarks 1.   p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)

2.   f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0,1), n: Channel number (n = 0, 1, 3))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) **Note**	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	162		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	354		ns
		2.4 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	958		ns
SIp hold time (from SCKp↑) **Note**	t$_{KSI1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	38		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	38		ns
		2.4 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output **Note**	t$_{KSO1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		200	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		390	ns
		2.4 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		966	ns

Note   When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

(**Cautions** and **Remarks** are listed on the next page.)

3.5.2 Serial interface IICA

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode: f$_{CLK}$ ≥ 3.5 MHz			0	400	kHz
		Normal mode: f$_{CLK}$ ≥ 1 MHz	0	100			kHz
Setup time of restart condition	t$_{SU:STA}$		4.7		0.6		μs
Hold time[Note 1]	t$_{HD:STA}$		4.0		0.6		μs
Hold time when SCLA0 = "L"	t$_{LOW}$		4.7		1.3		μs
Hold time when SCLA0 = "H"	t$_{HIGH}$		4.0		0.6		μs
Data setup time (reception)	t$_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	t$_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	t$_{SU:STO}$		4.0		0.6		μs
Bus-free time	t$_{BUF}$		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

\<R>   **2.** The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution   Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I$_{OH1}$, I$_{OL1}$, V$_{OH1}$, V$_{OL1}$) must satisfy the values in the redirect destination.

Remark   The maximum value of C$_b$ (communication line capacitance) and the value of R$_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: C$_b$ = 400 pF, R$_b$ = 2.7 kΩ
Fast mode: C$_b$ = 320 pF, R$_b$ = 1.1 kΩ

IICA serial transfer timing
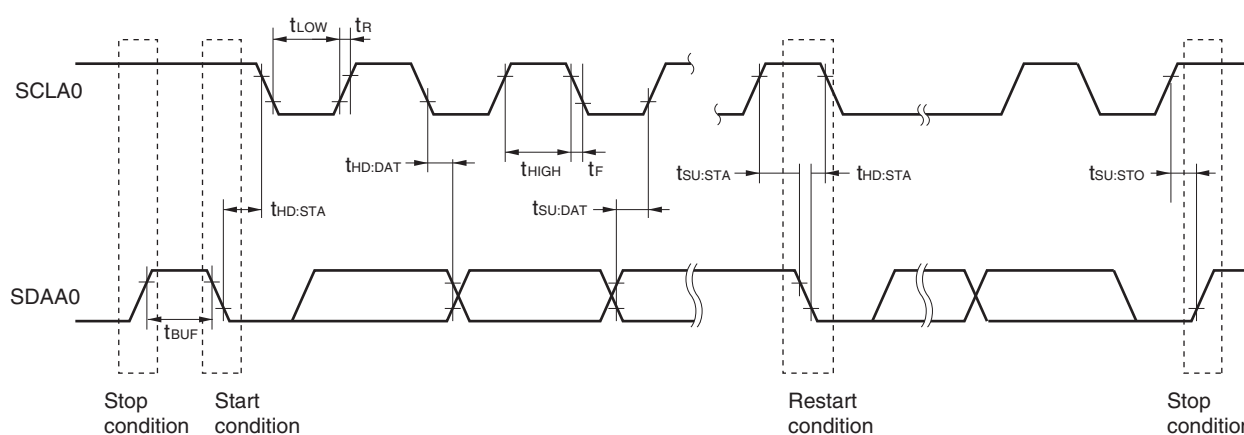
3.6　Analog Characteristics

3.6.1　A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (−) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (−) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (−) = AV_{REFM}
ANI0 to ANI3	Refer to **29.6.1 (1)**.	Refer to **29.6.1 (3)**.	Refer to **29.6.1 (4)**.
ANI16 to ANI22	Refer to **29.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **29.6.1 (1)**.		−

(1)　When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage

(T_A = −40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (−) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}[Note 3]			1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2, ANI3	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD}[Note 3]				±0.25	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD}[Note 3]				±0.25	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD}[Note 3]				±2.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD}[Note 3]				±1.5	LSB
Analog input voltage	V_{AIN}	ANI2, ANI3		0		AV_{REFP}	V
		Internal reference voltage (HS (high-speed main) mode)			V_{BGR}[Note 4]		V
		Temperature sensor output voltage (HS (high-speed main) mode)			V_{TMPS25}[Note 4]		V

(**Notes** are listed on the next page.)

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +105°C, 2.4 V $\leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[1]	AINL	10-bit resolution			1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22	3.6 V $\leq V_{DD} \leq$ 5.5 V	2.125		39	μs
			2.7 V $\leq V_{DD} \leq$ 5.5 V	3.1875		39	μs
			2.4 V $\leq V_{DD} \leq$ 5.5 V	17		39	μs
Conversion time	t_{CONV}	10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V $\leq V_{DD} \leq$ 5.5 V	2.375		39	μs
			2.7 V $\leq V_{DD} \leq$ 5.5 V	3.5625		39	μs
			2.4 V $\leq V_{DD} \leq$ 5.5 V	17		39	μs
Zero-scale error[1,2]	EZS	10-bit resolution				±0.60	%FSR
Full-scale error[1,2]	EFS	10-bit resolution				±0.60	%FSR
Integral linearity error[1]	ILE	10-bit resolution				±4.0	LSB
Differential linearity error[1]	DLE	10-bit resolution				±2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI3, ANI16 to ANI22		0		V_{DD}	V
		Internal reference voltage (HS (high-speed main) mode)		V_{BGR} [3]			V
		Temperature sensor output voltage (HS (high-speed main) mode)		V_{TMPS25} [3]			V

Notes **1.** Excludes quantization error (±1/2 LSB).

      2. This value is indicated as a ratio (%FSR) to the full-scale value.

      3. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (−) = AV$_{REFM}$ (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = V$_{BGR}$[Note 3], Reference voltage (−) = AV$_{REFM}$ [Note 4]= 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$			8		bit
Conversion time	t$_{CONV}$	8-bit resolution	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	8-bit resolution			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution			±1.0	LSB
Analog input voltage	V$_{AIN}$		0		V$_{BGR}$[Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).

     2. This value is indicated as a ratio (%FSR) to the full-scale value.

     3. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

     4. When reference voltage (−) = V$_{SS}$, the MAX. values are as follows.

       Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AV$_{REFM}$.

       Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

       Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

4. PACKAGE DRAWINGS

4.1 20-pin products

R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP
R5F1036AASP, R5F10369ASP, R5F10368ASP, R5F10367ASP, R5F10366ASP
R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP
R5F1036ADSP, R5F10369DSP, R5F10368DSP, R5F10367DSP, R5F10366DSP

<R>   R5F1026AGSP, R5F10269GSP, R5F10268GSP, R5F10267GSP, R5F10266GSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1

detail of lead end
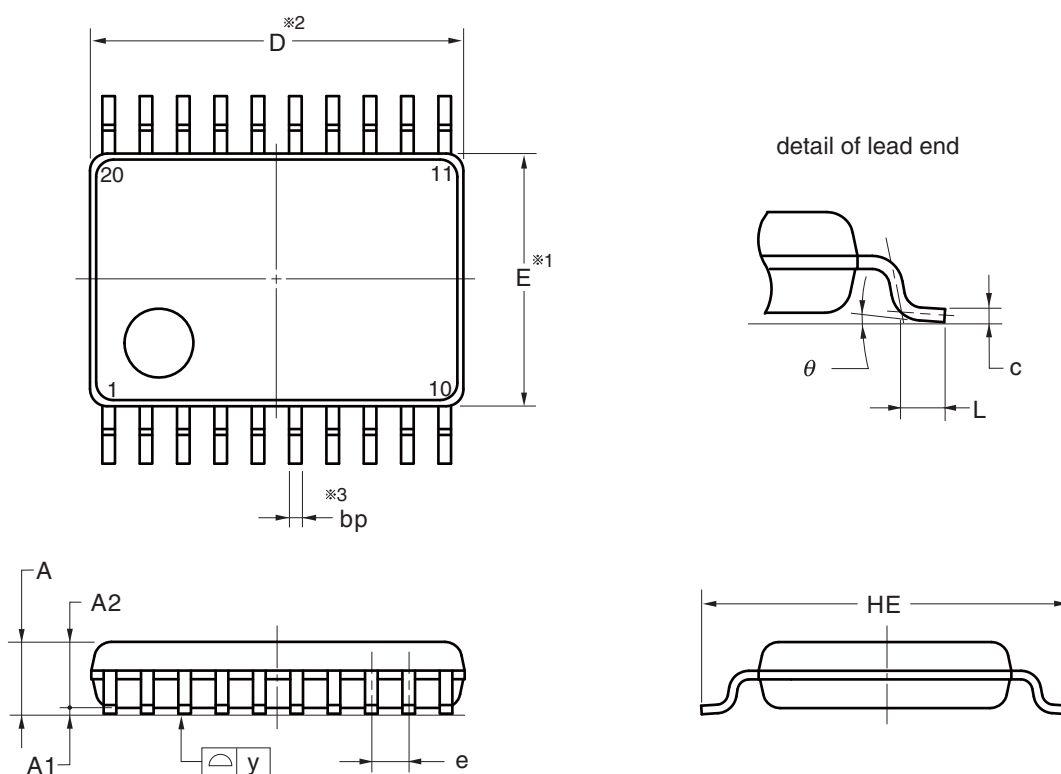
NOTE

1. Dimensions "※1" and "※2" do not include mold flash.

2. Dimension "※3" does not include trim offset.

(UNIT:mm)

ITEM	DIMENSIONS
D	6.50±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.45 MAX.
A1	0.10±0.10
A2	1.15
e	0.65±0.12
bp	$0.22 \begin{smallmatrix} +0.10 \\ -0.05 \end{smallmatrix}$
c	$0.15 \begin{smallmatrix} +0.05 \\ -0.02 \end{smallmatrix}$
L	0.50±0.20
y	0.10
θ	0° to 10°