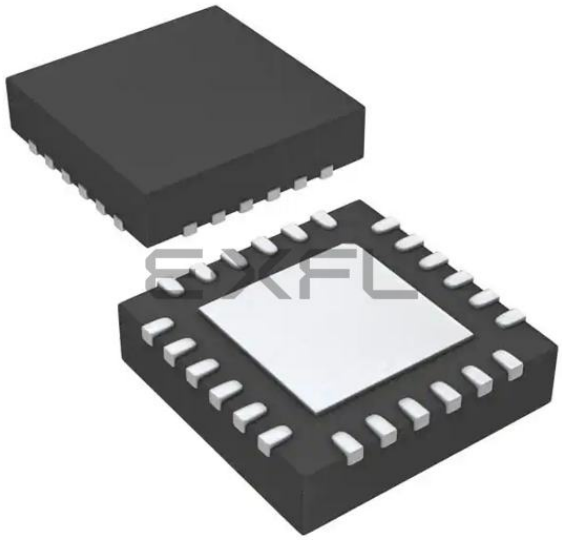
# Renesas Electronics America Inc - R5F10377ANA#W0 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CSI, I²C, UART/USART |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 18 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 11x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-WFQFN Exposed Pad |
| Supplier Device Package | 24-HWQFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10377ana-w0 |

(2/2)

| Item | | 20-pin | | 24-pin | | 30-pin | |
|---|---|---|---|---|---|---|---|
| | | R5F1026x | R5F1036x | R5F1027x | R5F1037x | R5F102Ax | R5F103Ax |
| Clock output/buzzer output | | 1 | | | | 2 | |
| | | 2.44 kHz to 10 MHz: (Peripheral hardware clock: $f_{MAIN}$ = 20 MHz operation) | | | | | |
| 8/10-bit resolution A/D converter | | 11 channels | | | | 8 channels | |
| Serial interface | | [R5F1026x (20-pin), R5F1027x (24-pin)]<br>・ CSI: 2 channels/Simplified $I^2C$: 2 channels/UART: 1 channel<br>[R5F102Ax (30-pin)]<br>・ CSI: 1 channel/Simplified $I^2C$: 1 channel/UART: 1 channel<br>・ CSI: 1 channel/Simplified $I^2C$: 1 channel/UART: 1 channel<br>・ CSI: 1 channel/Simplified $I^2C$: 1 channel/UART: 1 channel<br>[R5F1036x (20-pin), R5F1037x (24-pin)]<br>・ CSI: 1 channel/Simplified $I^2C$: 0 channel/UART: 1 channel<br>[R5F103Ax (30-pin)]<br>・ CSI: 1 channel/Simplified $I^2C$: 0 channel/UART: 1 channel | | | | | |
| | $I^2C$ bus | 1 channel | | | | | |
| Multiplier and divider/multiply-accumulator | | • 16 bits × 16 bits = 32 bits (unsigned or signed)<br>• 32 bits × 32 bits = 32 bits (unsigned)<br>• 16 bits × 16 bits + 32 bits = 32 bits (unsigned or signed) | | | | | |
| DMA controller | | 2 channels | — | 2 channels | — | 2 channels | — |
| Vectored interrupt sources | Internal | 18 | 16 | 18 | 16 | 26 | 19 |
| | External | 5 | | | | 6 | |
| Key interrupt | | 6 | | 10 | | — | |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | | | | | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 V (TYP)<br>• Power-down-reset: 1.50 V (TYP) | | | | | |
| Voltage detector | | • Rising edge : 1.88 to 4.06 V (12 stages)<br>• Falling edge : 1.84 to 3.98 V (12 stages) | | | | | |
| On-chip debug function | | Provided | | | | | |
| Power supply voltage | | $V_{DD}$ = 1.8 to 5.5 V | | | | | |
| Operating ambient temperature | | $T_A$ = −40 to +85°C (A: Consumer applications, D: Industrial applications), $T_A$ = −40 to +105°C (G: Industrial applications) | | | | | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (2/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low[Note 1] | $I_{OL1}$ | 20-, 24-pin products:<br>Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42<br>30-pin products:<br>Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | | | 20.0 [Note 2] | mA |
| | | Per pin for P60, P61 | | | | 15.0 [Note 2] | mA |
| | | 20-, 24-pin products:<br>Total of P40 to P42<br>30-pin products:<br>Total of P00, P01, P40, P120<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 60.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 9.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 1.8 | mA |
| | | 20-, 24-pin products:<br>Total of P00 to P03[Note 4], P10 to P14, P60, P61<br>30-pin products:<br>Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 80.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 27.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 5.4 | mA |
| | | Total of all pins (When duty ≤ 70% [Note 3]) | | | | 140 | mA |
| | $I_{OL2}$ | Per pin for P20 to P23 | | | | 0.4 | mA |
| | | Total of all pins | | | | 1.6 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $V_{SS}$ pin.

**2.** However, do not exceed the total current value.

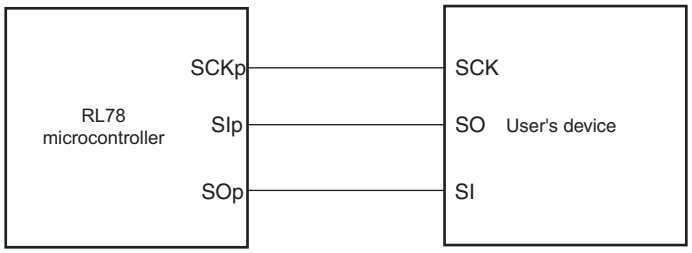
**3.** The output current value under conditions where the duty factor ≤ 70%.
If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).
- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

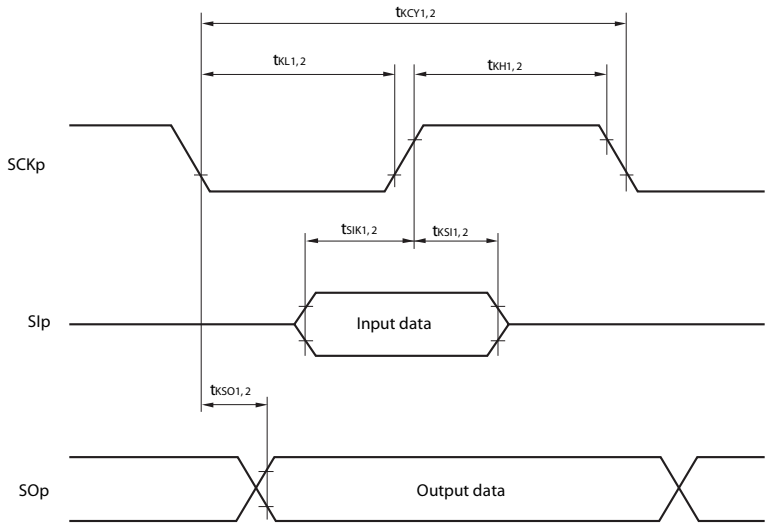
**4.** 24-pin products only.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

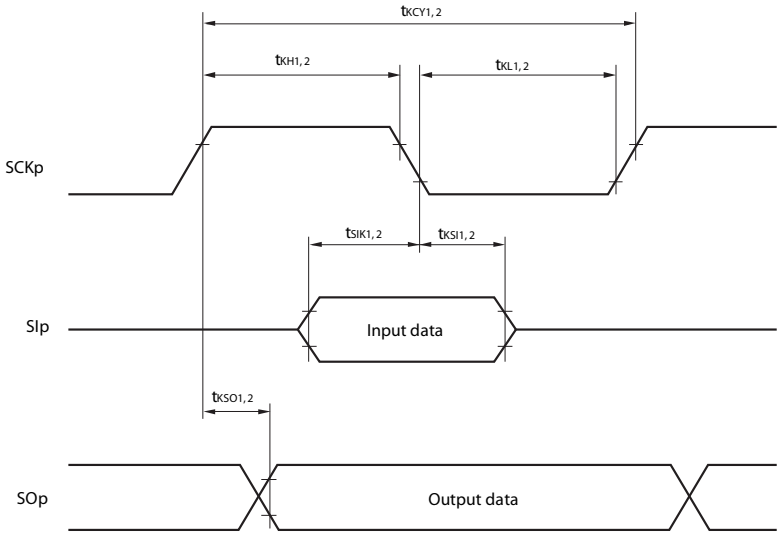
**CSI mode connection diagram (during communication at same potential)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




(**Remarks** are listed on the next page.)

**Remarks 1.** p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products.)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products.))

### (5) During communication at same potential (simplified $I^2C$ mode)

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode<br>LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | | 400 Note 1 | kHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 5 kΩ | | 300 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | $1/f_{MCK}$ + 145 Note 2 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 5 kΩ | $1/f_{MCK}$ + 230 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 355 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | ns |

**Notes 1.** The value must also be equal to or less than $f_{MCK}$/4.

**2.** Set $t_{SU:DAT}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

**Caution** Select the N-ch open drain output ($V_{DD}$ tolerance) mode for SDAr by using port output mode register h (POMh).

(**Remarks** are listed on the next page.)

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note4 | | Reception | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $f_{MCK}$/6 Note1 | | $f_{MCK}$/6 Note1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note3 | | 4.0 | | 1.3 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/6 Note1 | | $f_{MCK}$/6 Note1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note3 | | 4.0 | | 1.3 | Mbps |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/6 Notes1, 2 | | $f_{MCK}$/6 Notes1, 2 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note3 | | 4.0 | | 1.3 | Mbps |
| | | Transmission | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | **Note4** | | **Note4** | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.8 Note5 | | 2.8 Note5 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, | | **Note6** | | **Note6** | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note7 | | 1.2 Note7 | Mbps |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | **Notes 2, 8** | | **Notes 2, 8** | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note9 | | 0.43 Note9 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** Use it with $V_{DD} \geq V_b$.

**3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)

16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)

**4.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.

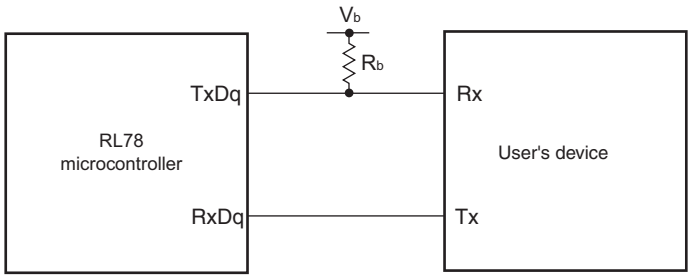
Expression for calculating the transfer rate when 4.0 V ≤ $V_{DD}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

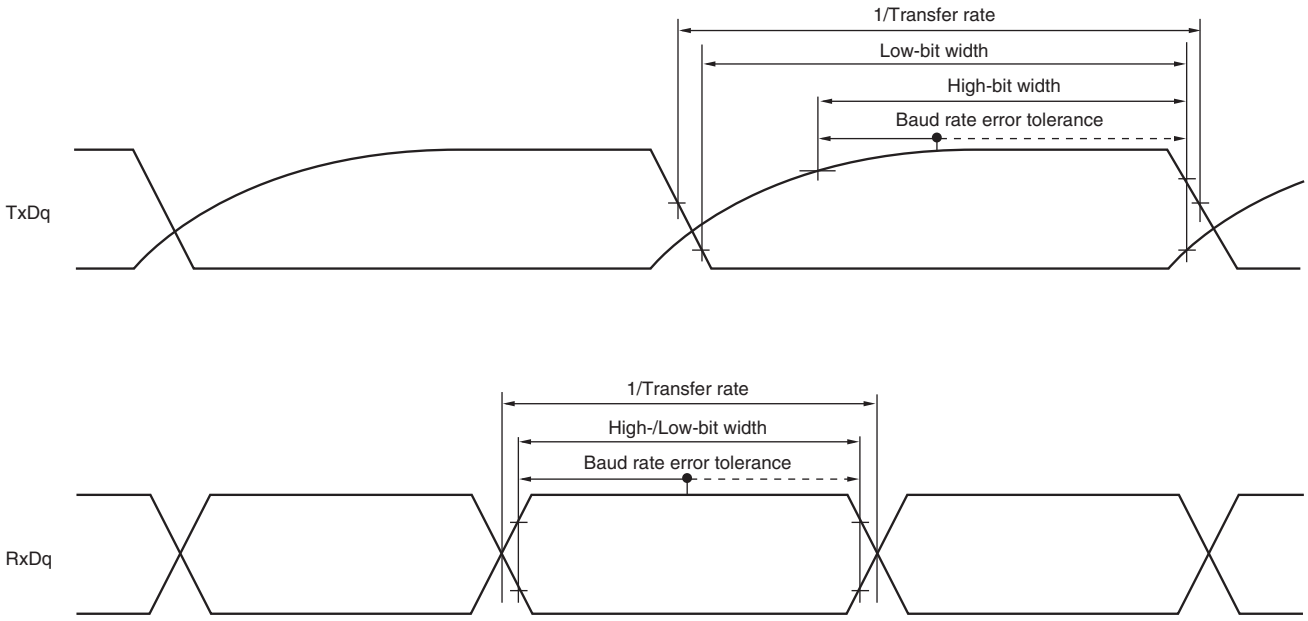
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**UART mode connection diagram (during communication at different potential)**




**UART mode bit width (during communication at different potential) (reference)**




**Remarks 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance, $C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**4.** UART0 of the 20- and 24-pin products supports communication at different potential only when the peripheral I/O redirection function is not used.

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 300 | | 1150 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 500 | | 1150 | | ns |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 −75 | | $t_{KCY1}$/2−75 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 −170 | | $t_{KCY1}$/2−170 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 −458 | | $t_{KCY1}$/2−458 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 −12 | | $t_{KCY1}$/2−50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 −18 | | $t_{KCY1}$/2−50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 −50 | | $t_{KCY1}$/2−50 | | ns |

**Note** Use it with $V_{DD} \geq V_b$.

**Cautions 1.** Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.

**2.** CSI01 and CSI11 cannot communicate at different potential.

**Remarks 1.** $R_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$ [F]: Communication line (SCKp, SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20)

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**

**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 44 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 44 | | 110 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | ns |
| Delay time from SCKp↑ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 25 | | 25 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 25 | | 25 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 25 | | 25 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** Use it with $V_{DD} \geq V_b$.

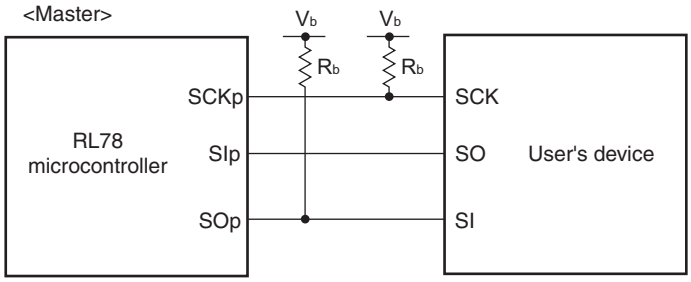
**Cautions 1.** Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.

**2.** CSI01 and CSI11 cannot communicate at different potential.

**Remarks 1.** $R_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$ [F]: Communication line (SCKp, SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

**CSI mode connection diagram (during communication at different potential)**



**(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = −40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 12/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 10/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 − 12 | | $t_{KCY2}$/2 − 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 − 18 | | $t_{KCY2}$/2 − 50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | $t_{KCY2}$/2 − 50 | | $t_{KCY2}$/2 − 50 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_{DD}$ ≤ 4.0 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_{DD}$ ≤ 2.0 V Note 2 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 5 | $t_{KSO2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 120 | | 2/$f_{MCK}$ + 573 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

**Notes 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**2.** Use it with $V_{DD} \geq V_b$.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

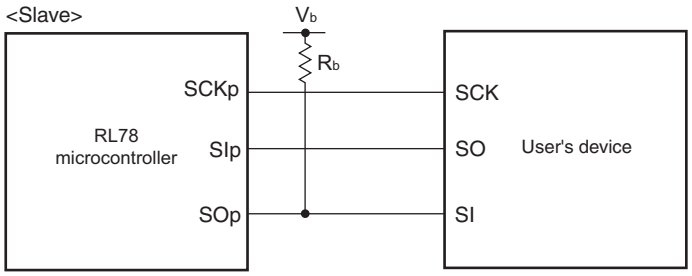
**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Cautions 1.** Select the TTL input buffer for the SIp and SCKp pins and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**2.** CSI01 and CSI11 cannot communicate at different potential.

**CSI mode connection diagram (during communication at different potential)**

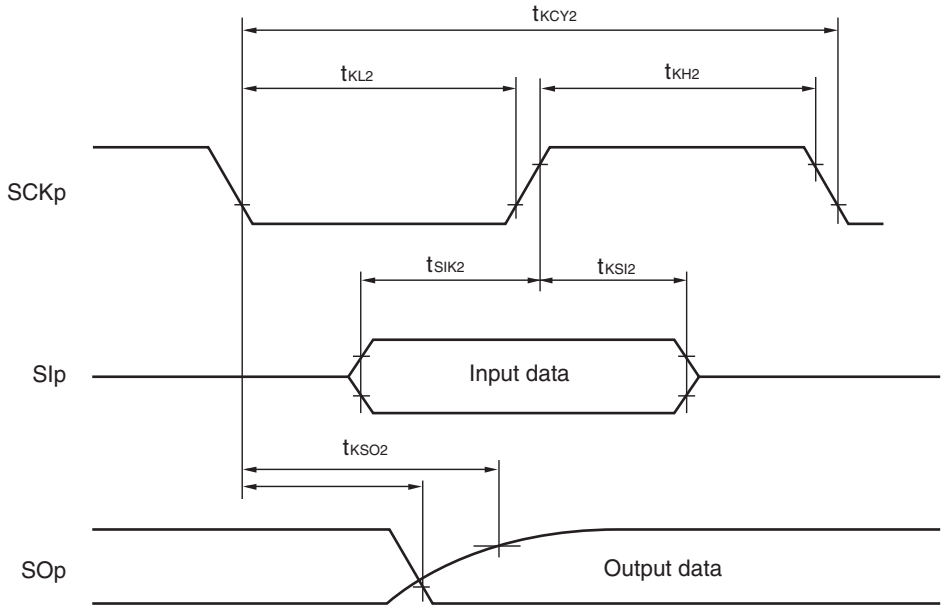



**Remarks 1.** $R_b$ [Ω]: Communication line (SOp) pull-up resistance, $C_b$ [F]: Communication line (SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 10))

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (3/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | Normal input buffer<br>20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | TTL input buffer<br>20-, 24-pin products: P10, P11<br>30-pin products: P01, P10, P11, P13 to P17 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 2.2 | | $V_{DD}$ | V |
| | | | 3.3 V ≤ $V_{DD}$ < 4.0 V | 2.0 | | $V_{DD}$ | V |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V | 1.5 | | $V_{DD}$ | V |
| | $V_{IH3}$ | Normal input buffer<br>P20 to P23 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60, P61 | | 0.7$V_{DD}$ | | 6.0 | V |
| | $V_{IH5}$ | P121, P122, P125[Note 1], P137, EXCLK, $\overline{\text{RESET}}$ | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | Normal input buffer<br>20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | 0 | | 0.2$V_{DD}$ | V |
| | $V_{IL2}$ | TTL input buffer<br>20-, 24-pin products: P10, P11<br>30-pin products: P01, P10, P11, P13 to P17 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | 3.3 V ≤ $V_{DD}$ < 4.0 V | 0 | | 0.5 | V |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P23 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL4}$ | P60, P61 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL5}$ | P121, P122, P125[Note 1], P137, EXCLK, $\overline{\text{RESET}}$ | | 0 | | 0.2$V_{DD}$ | V |
| Output voltage, high | $V_{OH1}$ | 20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –3.0 mA | $V_{DD}$–0.7 | | | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –2.0 mA | $V_{DD}$–0.6 | | | V |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –1.5 mA | $V_{DD}$–0.5 | | | V |
| | $V_{OH2}$ | P20 to P23 | $I_{OH2}$ = –100 μA | $V_{DD}$–0.5 | | | V |

**Notes 1.** 20, 24-pin products only.

**2.** 24-pin products only.

**Caution** The maximum value of $V_{IH}$ of pins P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products is $V_{DD}$ even in N-ch open-drain mode. High level is not output in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(4/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, low | $V_{OL1}$ | 20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P23 | $I_{OL2}$ = 400 μA | | | 0.4 | V |
| | $V_{OL3}$ | P60, P61 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 2.0 mA | | | 0.4 | V |
| Input leakage current, high | $I_{LIH1}$ | Other than P121, P122 | $V_I$ = $V_{DD}$ | | | 1 | μA |
| | $I_{LIH2}$ | P121, P122 (X1, X2/EXCLK) | $V_I$ = $V_{DD}$ Input port or external clock input | | | 1 | μA |
| | | | $V_I$ = $V_{DD}$ When resonator connected | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | Other than P121, P122 | $V_I$ = $V_{SS}$ | | | –1 | μA |
| | $I_{LIL2}$ | P121, P122 (X1, X2/EXCLK) | $V_I$ = $V_{SS}$ Input port or external clock input | | | –1 | μA |
| | | | $V_I$ = $V_{SS}$ When resonator connected | | | –10 | μA |
| On-chip pull-up resistance | $R_U$ | 20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42, P125, $\overline{\text{RESET}}$<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | $V_I$ = $V_{SS}$, input port | 10 | 20 | 100 | kΩ |

**Note** 24-pin products only.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**(2) 30-pin products**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD1}$ | Operating mode | HS (High-speed main) mode[Note 4] | $f_{IH}$ = 24 MHz[Note 3] | Basic operation | $V_{DD}$ = 5.0 V | | 1.5 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.5 | | |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.7 | 5.8 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.7 | 5.8 | |
| | | | | $f_{IH}$ = 16 MHz[Note 3] | | $V_{DD}$ = 5.0 V | | 2.7 | 4.2 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.7 | 4.2 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 3.0 | 4.9 | mA |
| | | | | | | Resonator connection | | 3.2 | 5.0 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 3.0 | 4.9 | mA |
| | | | | | | Resonator connection | | 3.2 | 5.0 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 1.9 | 2.9 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.9 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 1.9 | 2.9 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.9 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator clock is stopped.

**3.** When high-speed system clock is stopped

**4.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Temperature condition of the TYP. value is $T_A$ = 25°C.

### (2) 30-pin products

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 6 | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 440 | 2300 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 2300 | |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 400 | 1700 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 1700 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 190 | 1020 | μA |
| | | | | | Resonator connection | | 260 | 1100 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 190 | 1020 | μA |
| | | | | | Resonator connection | | 260 | 1100 | |
| | $I_{DD3}$ Note 5 | STOP mode | $T_A$ = –40°C | | | | 0.18 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.30 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.46 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.75 | 3.30 | |
| | | | $T_A$ = +105°C | | | | 2.94 | 15.30 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C.

### (3) Peripheral functions (Common to all products)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed onchip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | μA |
| 12-bit interval timer operating current | $I_{TMKA}$ Notes 1, 2, 3 | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 4 | $f_{IL}$ = 15 kHz | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 5 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | 1.30 | 1.70 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.50 | 0.70 | mA |
| A/D converter reference voltage operating current | $I_{ADREF}$ Note 1 | | | | 75.0 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | 75.0 | | μA |
| LVD operating current | $I_{LVD}$ Notes 1, 6 | | | | 0.08 | | μA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 8 | | | | 2.00 | 12.20 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 7 | | | | 2.00 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 9 | | 0.50 | 1.10 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 2.04 | mA |
| | | CSI/UART operation | | | 0.70 | 1.54 | mA |

**Notes 1.** Current flowing to the $V_{DD}$.

**2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**3.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$, and $I_{FIL}$ and $I_{TMKA}$ when the 12-bit interval timer operates.

**4.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer operates.

**5.** Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**6.** Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit operates.

**7.** Current flowing only during data flash rewrite.

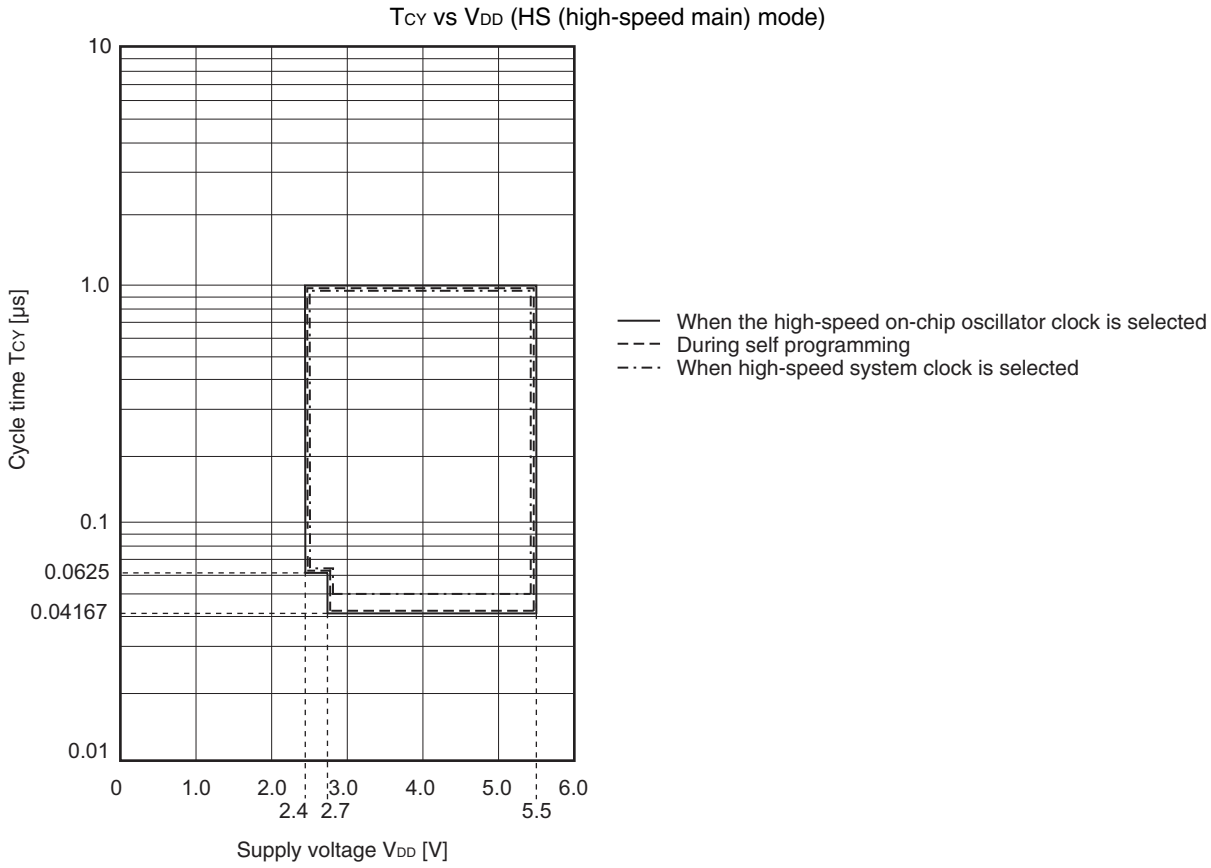
**8.** Current flowing only during self programming.

**9.** For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.

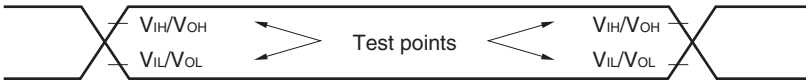
**Remarks 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**2.** Temperature condition of the TYP. value is $T_A$ = 25°C

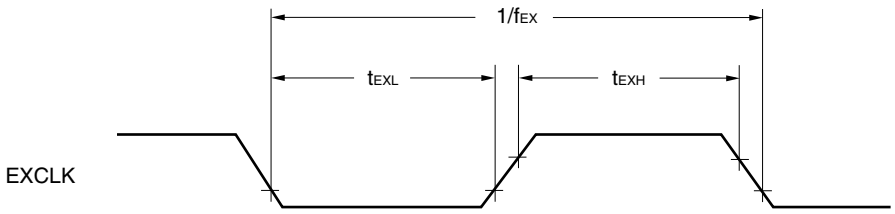
**Minimum Instruction Execution Time during Main System Clock Operation**




**AC Timing Test Point**




**External Main System Clock Timing**



### (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note4 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 12/$f_{MCK}$ and 1000 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–14 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–16 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–36 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note4 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 66 | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 113 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

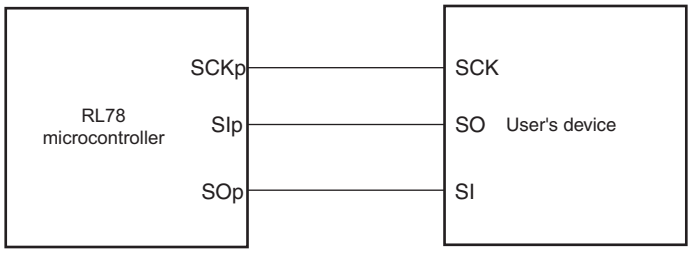
**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SOp output lines.

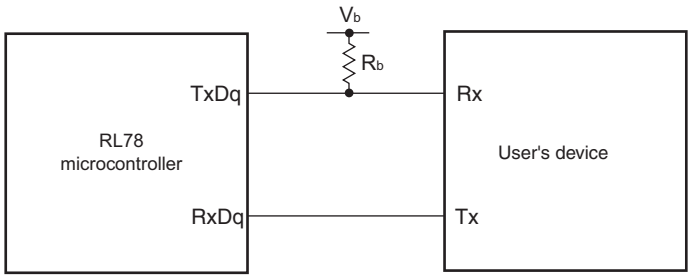
**5.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Caution** Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

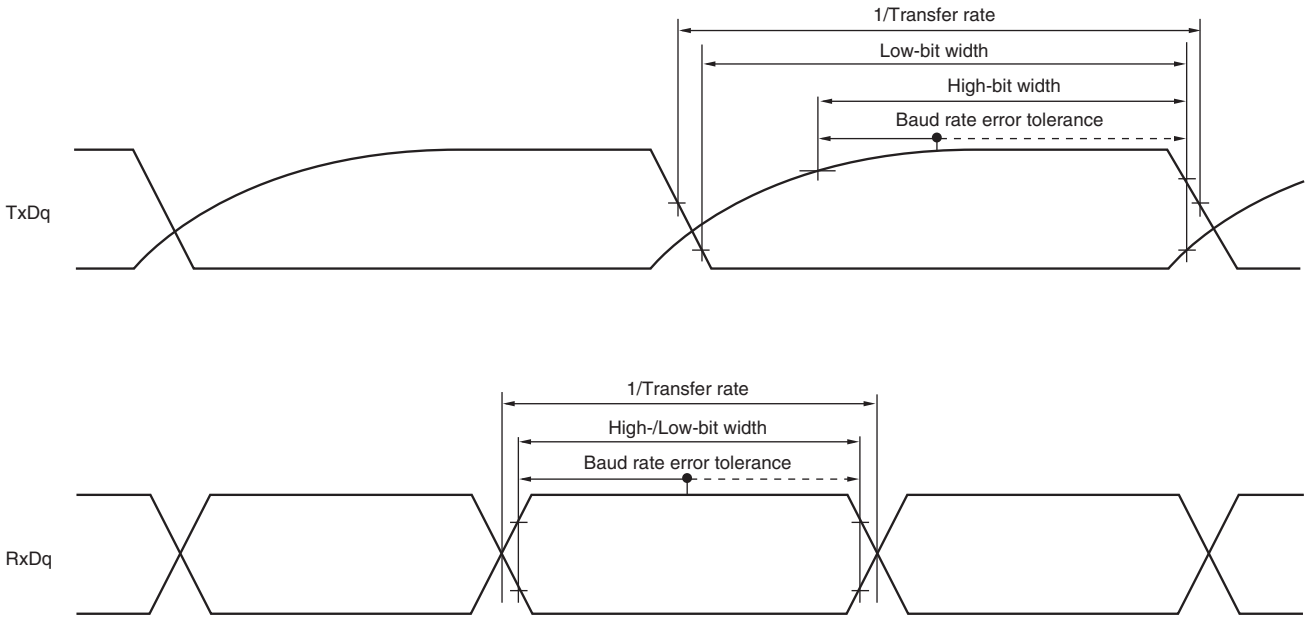
**CSI mode connection diagram (during communication at same potential)**



**UART mode connection diagram (during communication at different potential)**




**UART mode bit width (during communication at different potential) (reference)**




**Remarks 1.** $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage

**2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**4.** UART0 of the 20- and 24-pin products supports communication at different potential only when the peripheral I/O redirection function is not used.

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

**($T_A$ = −40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 88 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 88 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 220 | | ns |
| SIp hold time (from SCKp↓) Note | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↑ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 50 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 50 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 50 | ns |

**Note** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

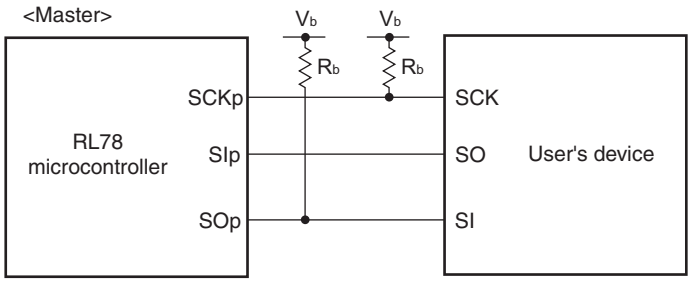
**Cautions 1.** Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.

**2.** CSI01 and CSI11 cannot communicate at different potential.

**Remarks 1.** $R_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$ [F]: Communication line (SCKp, SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

**CSI mode connection diagram (during communication at different potential)**



**(3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = $V_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (–) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution | | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI3, ANI16 to ANI22 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error[Notes 1, 2] | EZS | 10-bit resolution | | | | ±0.60 | %FSR |
| Full-scale error[Notes 1, 2] | EFS | 10-bit resolution | | | | ±0.60 | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution | | | | ±4.0 | LSB |
| Differential linearity error[Note 1] | DLE | 10-bit resolution | | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI3, ANI16 to ANI22 | | 0 | | $V_{DD}$ | V |
| | | Internal reference voltage (HS (high-speed main) mode) | | $V_{BGR}$[Note 3] | | | V |
| | | Temperature sensor output voltage (HS (high-speed main) mode) | | $V_{TMPS25}$[Note 3] | | | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.