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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I <sup>2</sup> C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-HWQFN (4x4)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10379dna-u0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10379dna-u0</a>

Table 1-1. List of Ordering Part Numbers

	Pin count	Package	Data flash	Fields of Application	Part Number
<R>	20 pins	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)	Mounted	A	R5F1026AASP#V5, R5F10269ASP#V5, R5F10268ASP#V5, R5F10267ASP#V5, R5F10266ASP#V5 R5F1026AASP#X5, R5F10269ASP#X5, R5F10268ASP#X5, R5F10267ASP#X5, R5F10266ASP#X5
				D	R5F1026ADSP#V5, R5F10269DSP#V5, R5F10268DSP#V5, R5F10267DSP#V5, R5F10266DSP#V5 R5F1026ADSP#X5, R5F10269DSP#X5, R5F10268DSP#X5, R5F10267DSP#X5, R5F10266DSP#X5
				G	R5F1026AGSP#V5, R5F10269GSP#V5, R5F10268GSP#V5, R5F10267GSP#V5, R5F10266GSP#V5 R5F1026AGSP#X5, R5F10269GSP#X5, R5F10268GSP#X5, R5F10267GSP#X5, R5F10266GSP#X5
			Not mounted	A	R5F1036AASP#V5, R5F10369ASP#V5, R5F10368ASP#V5, R5F10367ASP#V5, R5F10366ASP#V5 R5F1036AASP#X5, R5F10369ASP#X5, R5F10368ASP#X5, R5F10367ASP#X5, R5F10366ASP#X5
				D	R5F1036ADSP#V5, R5F10369DSP#V5, R5F10368DSP#V5, R5F10367DSP#V5, R5F10366DSP#V5 R5F1036ADSP#X5, R5F10369DSP#X5, R5F10368DSP#X5, R5F10367DSP#X5, R5F10366DSP#X5
				G	R5F1036AGSP#V5, R5F10369GSP#V5, R5F10368GSP#V5, R5F10367GSP#V5, R5F10366GSP#V5 R5F1036AGSP#X5, R5F10369GSP#X5, R5F10368GSP#X5, R5F10367GSP#X5, R5F10366GSP#X5
<R>	24 pins	24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)	Mounted	A	R5F1027AANA#U5, R5F10279ANA#U5, R5F10278ANA#U5, R5F10277ANA#U5 R5F1027AANA#W5, R5F10279ANA#W5, R5F10278ANA#W5, R5F10277ANA#W5
				D	R5F1027ADNA#U5, R5F10279DNA#U5, R5F10278DNA#U5, R5F10277DNA#U5 R5F1027ADNA#W5, R5F10279DNA#W5, R5F10278DNA#W5, R5F10277DNA#W5
				G	R5F1027AGNA#U5, R5F10279GNA#U5, R5F10278GNA#U5, R5F10277GNA#U5 R5F1027AGNA#W5, R5F10279GNA#W5, R5F10278GNA#W5, R5F10277GNA#W5
			Not mounted	A	R5F1037AANA#V5, R5F10379ANA#V5, R5F10378ANA#V5, R5F10377ANA#V5 R5F1037AANA#X5, R5F10379ANA#X5, R5F10378ANA#X5, R5F10377ANA#X5
				D	R5F1037ADNA#V5, R5F10379DNA#V5, R5F10378DNA#V5, R5F10377DNA#V5 R5F1037ADNA#X5, R5F10379DNA#X5, R5F10378DNA#X5, R5F10377DNA#X5
				G	R5F1037AGSP#V5, R5F10379GSP#V5, R5F10378GSP#V5, R5F10377GSP#V5 R5F1037AGSP#X5, R5F10379GSP#X5, R5F10378GSP#X5, R5F10377GSP#X5
<R>	30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A	R5F102AAASP#V0, R5F102A9ASP#V0, R5F102A8ASP#V0, R5F102A7ASP#V0 R5F102AAASP#X0, R5F102A9ASP#X0, R5F102A8ASP#X0, R5F102A7ASP#X0
				D	R5F102AADSP#V0, R5F102A9DSP#V0, R5F102A8DSP#V0, R5F102A7DSP#V0 R5F102AADSP#X0, R5F102A9DSP#X0, R5F102A8DSP#X0, R5F102A7DSP#X0
				G	R5F102AAGSP#V0, R5F102A9GSP#V0, R5F102A8GSP#V0, R5F102A7GSP#V0 R5F102AAGSP#X0, R5F102A9GSP#X0, R5F102A8GSP#X0, R5F102A7GSP#X0
			Not mounted	A	R5F103AAASP#V0, R5F103A9ASP#V0, R5F103A8ASP#V0, R5F103A7ASP#V0 R5F103AAASP#X0, R5F103A9ASP#X0, R5F103A8ASP#X0, R5F103A7ASP#X0
				D	R5F103AADSP#V0, R5F103A9DSP#V0, R5F103A8DSP#V0, R5F103A7DSP#V0 R5F103AADSP#X0, R5F103A9DSP#X0, R5F103A8DSP#X0, R5F103A7DSP#X0
				G	R5F103AAGSP#V0, R5F103A9GSP#V0, R5F103A8GSP#V0, R5F103A7GSP#V0 R5F103AAGSP#X0, R5F103A9GSP#X0, R5F103A8GSP#X0, R5F103A7GSP#X0

**Note** For fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G12**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

### 1.3.2 On-chip oscillator characteristics

(1) High-speed on-chip oscillator oscillation frequency of the R5F102 products

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	$T_A = -20$ to $+85$ °C	-1.0	+1.0	%
	$T_A = -40$ to $-20$ °C	-1.5	+1.5	
	$T_A = +85$ to $+105$ °C	-2.0	+2.0	

(2) High-speed on-chip oscillator oscillation frequency of the R5F103 products

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	$T_A = -40$ to $+85$ °C	-5.0	+5.0	%

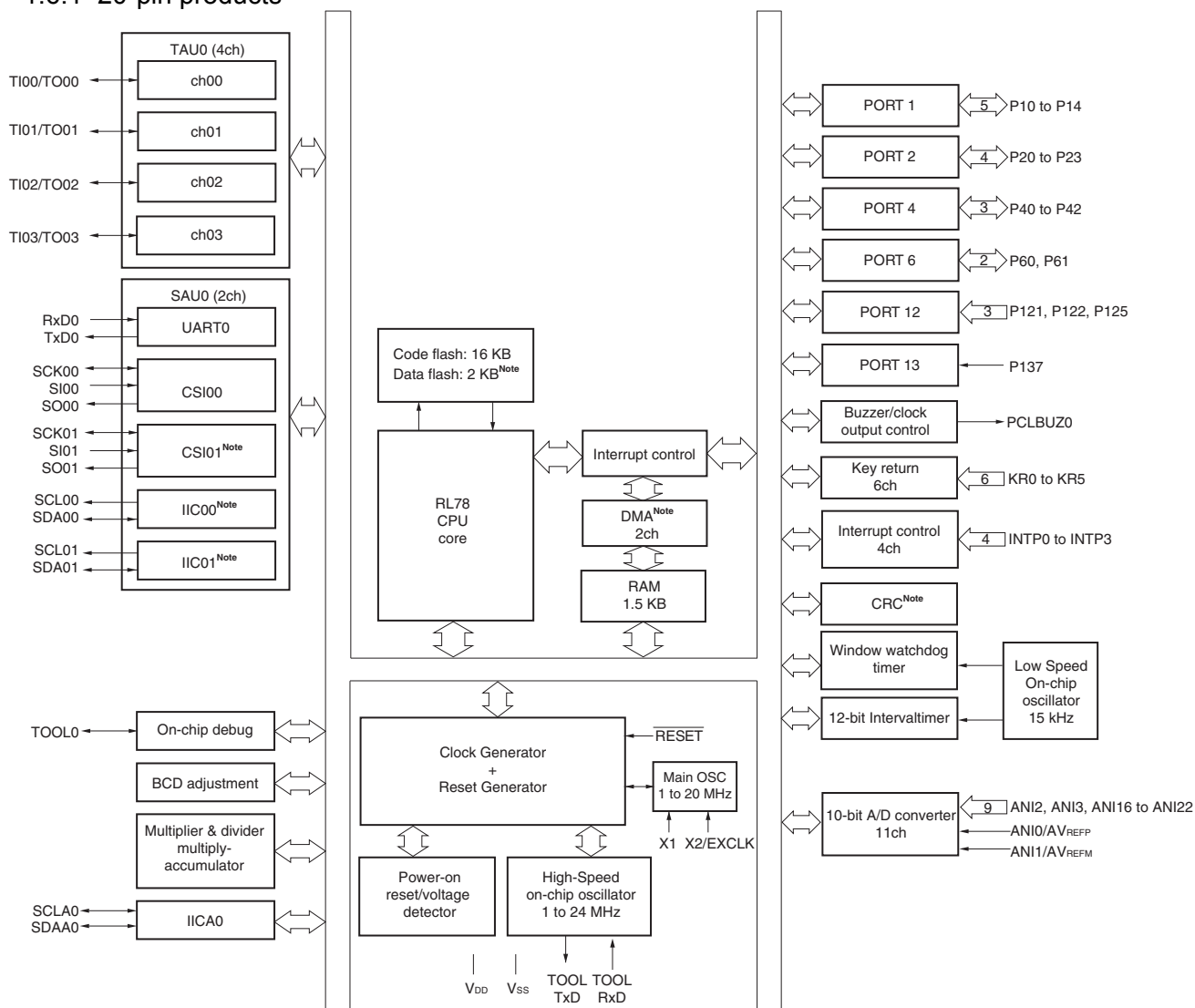
### 1.3.3 Peripheral Functions

The following are differences in peripheral functions between the R5F102 products and the R5F103 products.

RL78/G12		R5F102 product		R5F103 product	
		20, 24 pin product	30 pin product	20, 24 pin product	30 pin product
Serial interface	UART	1 channel	3 channels	1 channel	
	CSI	2 channels	3 channels	1 channel	
	Simplified I <sup>2</sup> C	2 channels	3 channels	None	
DMA function		2 channels		None	
Safety function	CRC operation	Yes		None	
	RAM guard	Yes		None	
	SFR guard	Yes		None	

## 1.6 Block Diagram

## 1.6.1 20-pin products



**Note** Provided only in the R5F102 products.

## <R> 2. ELECTRICAL SPECIFICATIONS ( $T_A = -40$ to $+85^\circ\text{C}$ )

<R> This chapter describes the following electrical specifications.

Target products A: Consumer applications  $T_A = -40$  to  $+85^\circ\text{C}$

<R> R5F102xxAxx, R5F103xxAxx

D: Industrial applications  $T_A = -40$  to  $+85^\circ\text{C}$

<R> R5F102xxDxx, R5F103xxDxx

G: Industrial applications when  $T_A = -40$  to  $+105^\circ\text{C}$  products is used in the range of  $T_A = -40$  to  $+85^\circ\text{C}$

<R> R5F102xxGxx

**Cautions** 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product.

## (2) 30-pin products

 $(T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note 1</sup>	I <sub>DD2</sub> <sup>Note 2</sup>	HALT mode	HS (High-speed main) mode <sup>Note 6</sup>	f <sub>IH</sub> = 24 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		440	1280	μA	
					V <sub>DD</sub> = 3.0 V		440	1280		
				f <sub>IH</sub> = 16 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		400	1000	μA	
					V <sub>DD</sub> = 3.0 V		400	1000		
				LS (Low-speed main) mode <sup>Note 6</sup>	f <sub>IH</sub> = 8 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 3.0 V		260	530	μA
						V <sub>DD</sub> = 2.0 V		260	530	
			HS (High-speed main) mode <sup>Note 6</sup>	f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		280	1000	μA	
					Resonator connection		450	1170		
				f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		280	1000	μA	
					Resonator connection		450	1170		
				f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		190	600	μA	
					Resonator connection		260	670		
				f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		190	600	μA	
					Resonator connection		260	670		
			LS (Low-speed main) mode <sup>Note 6</sup>	f <sub>MX</sub> = 8 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380		
				f <sub>MX</sub> = 8 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 2.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380		
	I <sub>DD3</sub> <sup>Note 5</sup>	STOP mode	T <sub>A</sub> = −40°C					0.18	0.50	μA
			T <sub>A</sub> = +25°C					0.23	0.50	
			T <sub>A</sub> = +50°C					0.30	1.10	
			T <sub>A</sub> = +70°C					0.46	1.90	
			T <sub>A</sub> = +85°C					0.75	3.30	

**Notes** 1. Total current flowing into  $V_{DD}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$  or  $V_{SS}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator clock is stopped.

4. When high-speed system clock is stopped.

5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode:  $V_{DD} = 2.7\text{ V}$  to  $5.5\text{ V}$  @  $1\text{ MHz}$  to  $24\text{ MHz}$

$V_{DD} = 2.4\text{ V}$  to  $5.5\text{ V}$  @  $1\text{ MHz}$  to  $16\text{ MHz}$

LS (Low speed main) mode:  $V_{DD} = 1.8\text{ V}$  to  $5.5\text{ V}$  @  $1\text{ MHz}$  to  $8\text{ MHz}$

**Remarks** 1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2.  $f_{IH}$ : high-speed on-chip oscillator clock frequency

3. Except STOP mode, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$ .

## 2.4 AC Characteristics

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

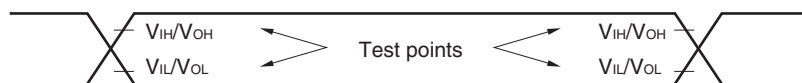
Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T <sub>CY</sub>	Main system clock (f <sub>MAIN</sub> ) operation	HS (High-speed main) mode	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V <sub>DD</sub> < 2.7 V	0.0625		1	μs
			During self programming	LS (Low-speed main) mode	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V	0.125		1
		HS (High-speed main) mode		2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V <sub>DD</sub> < 2.7 V	0.0625		1	μs
		LS (Low-speed main) mode	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V	0.125		1	μs	
External main system clock frequency	f <sub>EX</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V <sub>DD</sub> < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V <sub>DD</sub> < 2.4 V			1.0		8.0	MHz
External main system clock input high-level width, low-level width	t <sub>EXH</sub> , t <sub>EXL</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V			24			ns
		2.4 V ≤ V <sub>DD</sub> < 2.7 V			30			ns
		1.8 V ≤ V <sub>DD</sub> < 2.4 V			60			ns
TI00 to TI07 input high-level width, low-level width	t <sub>TIH</sub> , t <sub>TIL</sub>				1/f <sub>MCK</sub> + 10			ns
TO00 to TO07 output frequency	f <sub>TO</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V					12	MHz
		2.7 V ≤ V <sub>DD</sub> < 4.0 V					8	MHz
		1.8 V ≤ V <sub>DD</sub> < 2.7 V					4	MHz
PCLBUZ0, or PCLBUZ1 output frequency	f <sub>PCL</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V					16	MHz
		2.7 V ≤ V <sub>DD</sub> < 4.0 V					8	MHz
		1.8 V ≤ V <sub>DD</sub> < 2.7 V					4	MHz
INTP0 to INTP5 input high-level width, low-level width	t <sub>INTH</sub> , t <sub>INTL</sub>				1			μs
KR0 to KR9 input available width	t <sub>KR</sub>				250			ns
RESET low-level width	t <sub>RSL</sub>				10			μs

**Remark** fMCK: Timer array unit operation clock frequency

(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

## 2.5 Peripheral Functions Characteristics

### AC Timing Test Point



### 2.5.1 Serial array unit

#### (1) During communication at same potential (UART mode)

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate				$f_{MCK}/6$		$f_{MCK}/6$	bps
Note 1		Theoretical value of the maximum transfer rate $f_{CLK} = f_{MCK}$ <sup>Note2</sup>		4.0		1.3	Mbps

**Notes** 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock ( $f_{CLK}$ ) are:

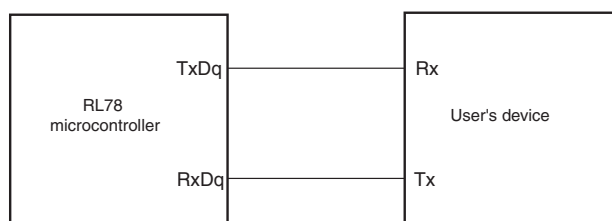
HS (high-speed main) mode: 24 MHz ( $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

16 MHz ( $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

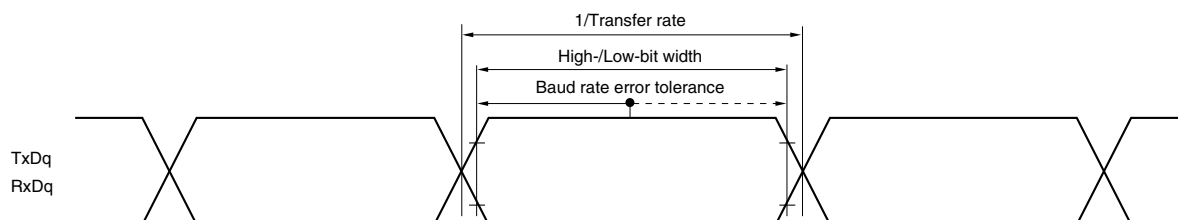
LS (low-speed main) mode: 8 MHz ( $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

#### UART mode connection diagram (during communication at same potential)



#### UART mode bit width (during communication at same potential) (reference)



**Remarks** 1. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

2.  $f_{MCK}$ : Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))



(2) During communication at same potential (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)

(T<sub>A</sub> = -40 to +85°C, 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCK00 cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ 2/f <sub>CLK</sub>	83.3		250		ns
SCK00 high-/low-level width	t <sub>KH1</sub> , t <sub>KL1</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	t <sub>KCY1</sub> /2-7		t <sub>KCY1</sub> /2-50		ns
		2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	t <sub>KCY1</sub> /2-10		t <sub>KCY1</sub> /2-50		ns
SI00 setup time (to SCK00↑) <sup>Note 1</sup>	t <sub>SIK1</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	23		110		ns
		2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	33		110		ns
SI00 hold time (from SCK00↑) <sup>Note 2</sup>	t <sub>KSI1</sub>		10		10		ns
Delay time from SCK00↓ to SO00 output <sup>Note 3</sup>	t <sub>KSO1</sub>	C = 20 pF <sup>Note 4</sup>		10		10	ns

- Notes**
1. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 setup time becomes “to SCK00↓” when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.
  2. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 hold time becomes “from SCK00↓” when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.
  3. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The delay time to SO00 output becomes “from SCK00↑” when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.
  4. C is the load capacitance of the SCK00 and SO00 output lines.

**Caution** Select the normal input buffer for the SI00 pin and the normal output mode for the SO00 and SCK00 pins by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).

- Remarks**
1. This specification is valid only when CSI00's peripheral I/O redirect function is not used.
  2. f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS00 bit of serial mode register 00 (SMR00).)

- Remarks 1.** p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products.)
- 2.**  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products.))

**(5) During communication at same potential (simplified I<sup>2</sup>C mode)**

**( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	HS (high-speed main) Mode LS (low-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	$f_{SCL}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$		400 <sup>Note 1</sup>	kHz
		$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 5\text{ k}\Omega$		300 <sup>Note 1</sup>	kHz
Hold time when SCLr = "L"	$t_{LOW}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	1150		ns
		$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 5\text{ k}\Omega$	1550		ns
Hold time when SCLr = "H"	$t_{HIGH}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	1150		ns
		$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 5\text{ k}\Omega$	1550		ns
Data setup time (reception)	$t_{SU:DAT}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	$1/f_{MCK} + 145$ <sup>Note 2</sup>		ns
		$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 5\text{ k}\Omega$	$1/f_{MCK} + 230$ <sup>Note 2</sup>		ns
Data hold time (transmission)	$t_{HD:DAT}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	0	355	ns
		$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 5\text{ k}\Omega$	0	405	ns

- Notes 1.** The value must also be equal to or less than  $f_{MCK}/4$ .
- 2.** Set  $t_{SU:DAT}$  so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

**Caution** Select the N-ch open drain output ( $V_{DD}$  tolerance) mode for SDAr by using port output mode register h (POMh).

(Remarks are listed on the next page.)

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate <small>Note4</small>		Reception	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V			f <sub>MCK</sub> /6 <small>Note1</small>	bps
			Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> <small>Note3</small>			4.0	Mbps
			2.7 V ≤ V <sub>DD</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V			f <sub>MCK</sub> /6 <small>Note1</small>	bps
			Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> <small>Note3</small>			4.0	Mbps
			1.8 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V			f <sub>MCK</sub> /6 <small>Notes1, 2</small>	bps
			Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> <small>Note3</small>			4.0	Mbps
		Transmission	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V			<b>Note4</b>	bps
			Theoretical value of the maximum transfer rate C <sub>b</sub> = 50 pF, R <sub>b</sub> = 1.4 kΩ, V <sub>b</sub> = 2.7 V			2.8 <small>Note5</small>	Mbps
			2.7 V ≤ V <sub>DD</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V			<b>Note6</b>	bps
			Theoretical value of the maximum transfer rate C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ, V <sub>b</sub> = 2.3 V			1.2 <small>Note7</small>	Mbps
			1.8 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V			<b>Notes 2, 8</b>	bps
			Theoretical value of the maximum transfer rate C <sub>b</sub> = 50 pF, R <sub>b</sub> = 5.5 kΩ, V <sub>b</sub> = 1.6 V			0.43 <small>Note9</small>	Mbps

**Notes** 1. Transfer rate in the SNOOZE mode is 4800 bps only.2. Use it with V<sub>DD</sub> ≥ V<sub>b</sub>.3. The maximum operating frequencies of the CPU/peripheral hardware clock (f<sub>CLK</sub>) are:HS (high-speed main) mode: 24 MHz (2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V)16 MHz (2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V)LS (low-speed main) mode: 8 MHz (1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V)4. The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.Expression for calculating the transfer rate when 4.0 V ≤ V<sub>DD</sub> ≤ 5.5 V and 2.7 V ≤ V<sub>b</sub> ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)****( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

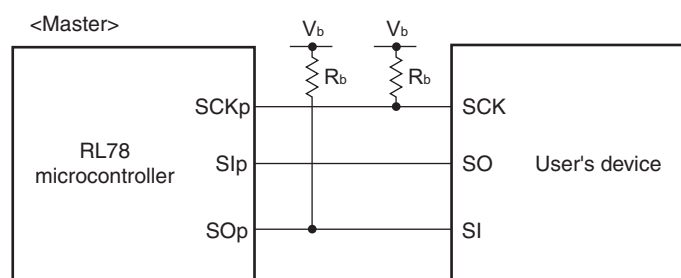
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↓) <sup>Note 1</sup>	$t_{SIK1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	44		110		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	44		110		ns
		$1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ <sup>Note 2</sup> , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	110		110		ns
Slp hold time (from SCKp↓) <sup>Note 1</sup>	$t_{KSI1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	19		19		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	19		19		ns
		$1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ <sup>Note 2</sup> , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	19		19		ns
Delay time from SCKp↑ to SOp output <sup>Note 1</sup>	$t_{KSO1}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$		25		25	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		25		25	ns
		$1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ <sup>Note 2</sup> , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$		25		25	ns

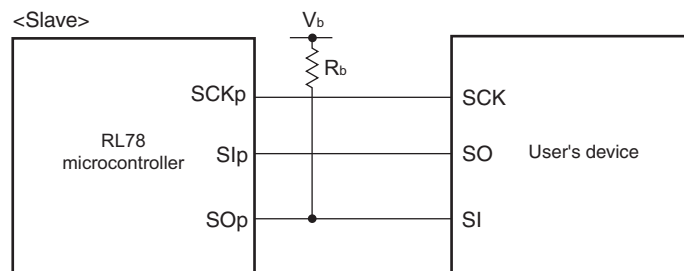
**Notes** 1. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.2. Use it with  $V_{DD} \geq V_b$ .**Cautions** 1. Select the TTL input buffer for the Slp pin and the N-ch open drain output ( $V_{DD}$  tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

2. CSI01 and CSI11 cannot communicate at different potential.

**Remarks** 1.  $R_b$  [ $\Omega$ ]: Communication line (SCKp, SOp) pull-up resistance,  $C_b$  [F]: Communication line (SCKp, SOp) load capacitance,  $V_b$  [V]: Communication line voltage

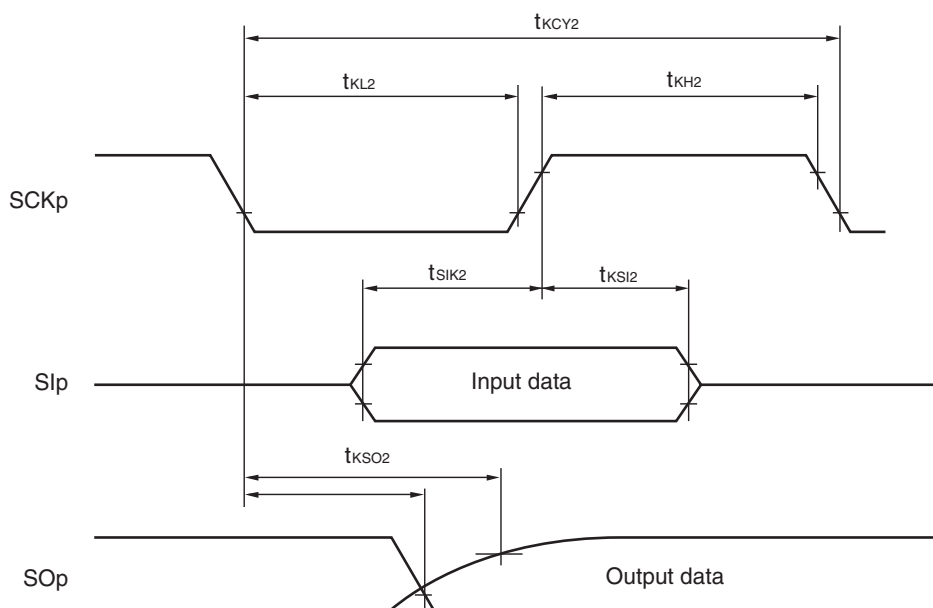
2. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

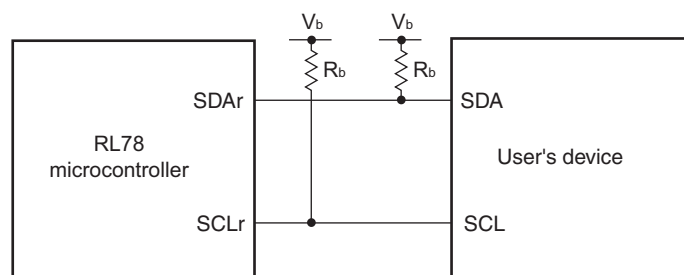
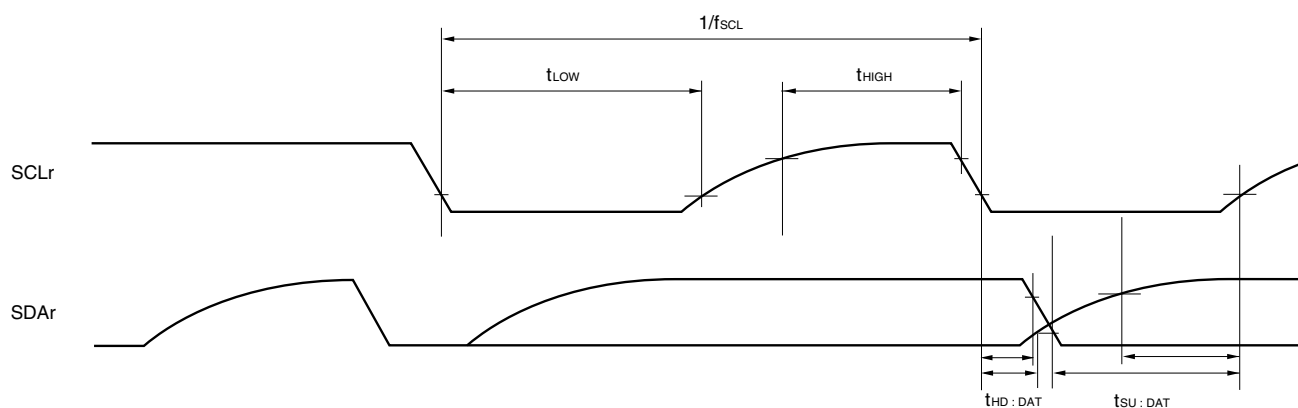
**CSI mode connection diagram (during communication at different potential)**

**CSI mode connection diagram (during communication at different potential)**

- Remarks**
1.  $R_b$  [ $\Omega$ ]: Communication line (SOp) pull-up resistance,  $C_b$  [F]: Communication line (SOp) load capacitance,  $V_b$  [V]: Communication line voltage
  2. p: CSI number ( $p = 00, 20$ ), m: Unit number ( $m = 0, 1$ ), n: Channel number ( $n = 0$ )
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number ( $mn = 00, 10$ ))

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**Simplified I<sup>2</sup>C mode connection diagram (during communication at different potential)****Simplified I<sup>2</sup>C mode serial transfer timing (during communication at different potential)**

- Remarks**
1.  $R_b$  [ $\Omega$ ]: Communication line (SDAr, SCLr) pull-up resistance,  $C_b$  [F]: Communication line (SDAr, SCLr) load capacitance,  $V_b$  [V]: Communication line voltage
  2.  $r$ : IIC Number ( $r = 00, 20$ )
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the serial clock select register  $m$  (SPS $m$ ) and the CKS $mn$  bit of serial mode register  $mn$  (SMR $mn$ ).  
 $m$ : Unit number ( $m = 0, 1$ ),  $n$ : Channel number ( $n = 0$ ))
  4. Simplified I<sup>2</sup>C mode is supported only by the R5F102 products.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

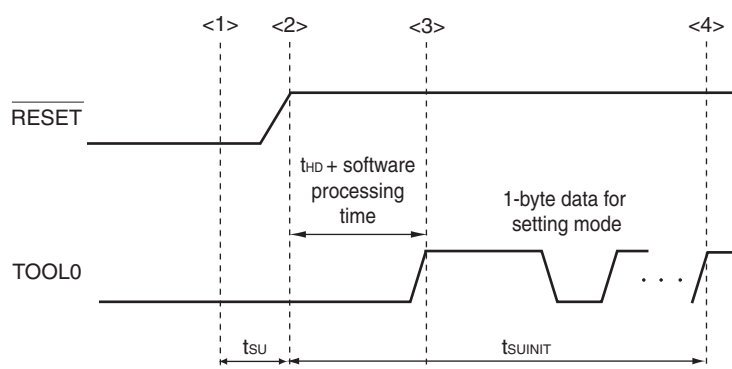
( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

## 2.10 Timing of Entry to Flash Memory Programming Modes

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	$t_{\text{SUNIT}}$	POR and LVD reset are released before external reset release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	$t_{\text{SU}}$	POR and LVD reset are released before external reset release	10			$\mu\text{s}$
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	$t_{\text{HD}}$	POR and LVD reset are released before external reset release	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark**  $t_{\text{SUNIT}}$ : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{\text{SU}}$ : Time to release the external reset after the TOOL0 pin is set to the low level

$t_{\text{HD}}$ : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

(T<sub>A</sub> = -40 to +105°C, 2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

(2/4)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low <sup>Note 1</sup>	I <sub>OL1</sub>	20-, 24-pin products: Per pin for P00 to P03 <sup>Note 4</sup> , P10 to P14, P40 to P42			8.5 <sup>Note 2</sup>	mA
		30-pin products: Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147				
		Per pin for P60, P61			15.0 <sup>Note 2</sup>	mA
		20-, 24-pin products: Total of P40 to P42	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V		25.5	mA
			2.7 V ≤ V <sub>DD</sub> < 4.0 V		9.0	mA
		30-pin products: Total of P00, P01, P40, P120 (When duty ≤ 70% <sup>Note 3</sup> )	2.4 V ≤ V <sub>DD</sub> < 2.7 V		1.8	mA
		20-, 24-pin products: Total of P00 to P03 <sup>Note 4</sup> , P10 to P14, P60, P61	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V		40.0	mA
			2.7 V ≤ V <sub>DD</sub> < 4.0 V		27.0	mA
		30-pin products: Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147 (When duty ≤ 70% <sup>Note 3</sup> )	2.4 V ≤ V <sub>DD</sub> < 2.7 V		5.4	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )			65.5	mA
	I <sub>OL2</sub>	Per pin for P20 to P23			0.4	mA
		Total of all pins			1.6	mA

**Notes** 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V<sub>SS</sub> pin.

2. However, do not exceed the total current value.

3. The output current value under conditions where the duty factor ≤ 70%.

If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = (I<sub>OL</sub> × 0.7)/(n × 0.01)

<Example> Where n = 80% and I<sub>OL</sub> = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. 24-pin products only.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



**(3) Peripheral functions (Common to all products)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed onchip oscillator operating current	$I_{FIL}$ <sup>Note 1</sup>				0.20		$\mu\text{A}$
12-bit interval timer operating current	$I_{TMKA}$ <sup>Notes 1, 2, 3</sup>				0.02		$\mu\text{A}$
Watchdog timer operating current	$I_{WDT}$ <sup>Notes 1, 2, 4</sup>	$f_{IL} = 15\text{ kHz}$			0.22		$\mu\text{A}$
A/D converter operating current	$I_{ADC}$ <sup>Notes 1, 5</sup>	When conversion at maximum speed	Normal mode, $AV_{REFP} = V_{DD} = 5.0\text{ V}$		1.30	1.70	$\text{mA}$
			Low voltage mode, $AV_{REFP} = V_{DD} = 3.0\text{ V}$		0.50	0.70	$\text{mA}$
A/D converter reference voltage operating current	$I_{ADREF}$ <sup>Note 1</sup>				75.0		$\mu\text{A}$
Temperature sensor operating current	$I_{TMPS}$ <sup>Note 1</sup>				75.0		$\mu\text{A}$
LVD operating current	$I_{LVD}$ <sup>Notes 1, 6</sup>				0.08		$\mu\text{A}$
Self-programming operating current	$I_{FSP}$ <sup>Notes 1, 8</sup>				2.00	12.20	$\text{mA}$
BGO operating current	$I_{BGO}$ <sup>Notes 1, 7</sup>				2.00	12.20	$\text{mA}$
SNOOZE operating current	$I_{SNOZ}$ <sup>Note 1</sup>	ADC operation	The mode is performed <sup>Note 9</sup>		0.50	1.10	$\text{mA}$
			The A/D conversion operations are performed, Low voltage mode, $AV_{REFP} = V_{DD} = 3.0\text{ V}$		1.20	2.04	$\text{mA}$
		CSI/UART operation			0.70	1.54	$\text{mA}$

**Notes** 1. Current flowing to the  $V_{DD}$ .

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$ , and  $I_{FIL}$  and  $I_{TMKA}$  when the 12-bit interval timer operates.4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$  and  $I_{WDT}$  when the watchdog timer operates.5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of  $I_{DD1}$  or  $I_{DD2}$  and  $I_{ADC}$  when the A/D converter operates in an operation mode or the HALT mode.6. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$  and  $I_{LVD}$  when the LVD circuit operates.

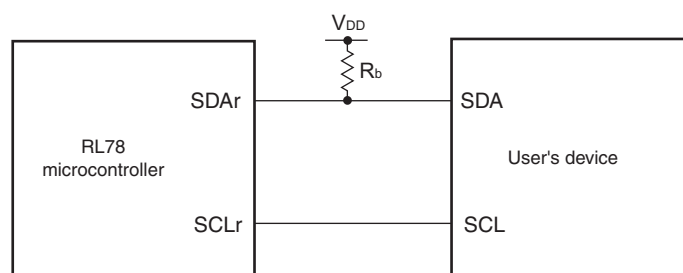
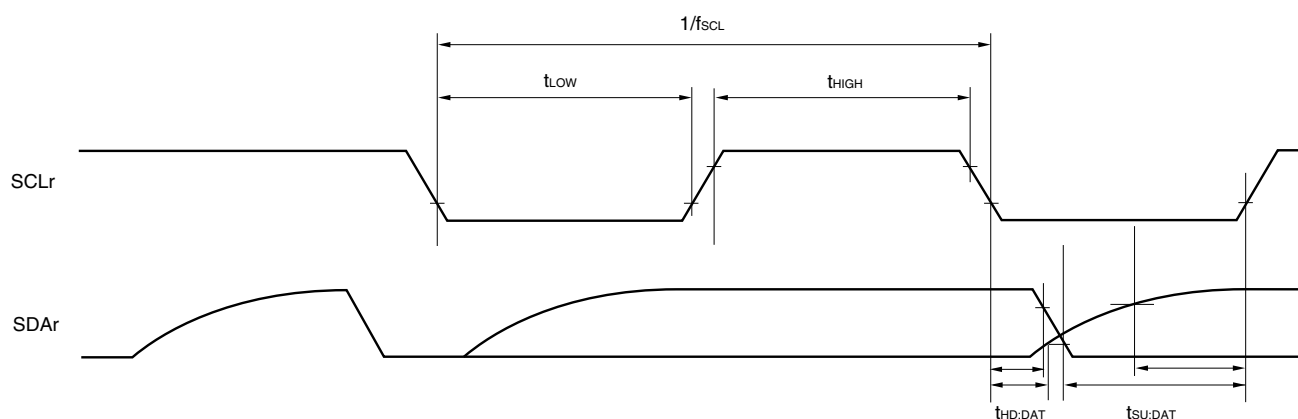
7. Current flowing only during data flash rewrite.

8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.**Remarks** 1.  $f_{IL}$ : Low-speed on-chip oscillator clock frequency2. Temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

**(4) During communication at same potential (simplified I<sup>2</sup>C mode)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	$f_{\text{SCL}}$	$C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$		100 <sup>Note 1</sup>	kHz
Hold time when SCLr = "L"	$t_{\text{LOW}}$	$C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	4600		ns
Hold time when SCLr = "H"	$t_{\text{HIGH}}$	$C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	4600		ns
Data setup time (reception)	$t_{\text{SU:DAT}}$	$C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 580$ <sup>Note 2</sup>		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	0	1420	ns

**Notes 1.** The value must also be equal to or less than  $f_{\text{MCK}}/4$ .**2.** Set  $t_{\text{SU:DAT}}$  so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".**Caution** Select the N-ch open drain output ( $V_{DD}$  tolerance) mode for SDAr by using port output mode register h (POMh).**Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)****Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)****Remarks 1.**  $R_b$  [ $\Omega$ ]: Communication line (SDAr) pull-up resistance $C_b$  [F]: Communication line (SCLr, SDAr) load capacitance**2.** r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1, 4, 5)**3.**  $f_{\text{MCK}}$ : Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number (m = 0, 1), n: Channel number (0, 1, 3))

**(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate <small>Note 4</small>		Reception	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$		$f_{MCK}/12$ <small>Note 1</small>	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ <small>Note 2</small>		2.0	Mbps
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$		$f_{MCK}/12$ <small>Note 1</small>	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ <small>Note 2</small>		2.0	Mbps
		Transmission	$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$		$f_{MCK}/12$ <small>Note 1</small>	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ <small>Note 2</small>		2.0	Mbps
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$		<b>Note 3</b>	bps
			Theoretical value of the maximum transfer rate $C_b = 50\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ , $V_b = 2.7\text{ V}$		2.0 <small>Note 4</small>	Mbps
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$		<b>Note 5</b>	bps
			Theoretical value of the maximum transfer rate $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$ , $V_b = 2.3\text{ V}$		1.2 <small>Note 6</small>	Mbps
			$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$		<b>Notes 2, 7</b>	bps
			Theoretical value of the maximum transfer rate $C_b = 50\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$ , $V_b = 1.6\text{ V}$		0.43 <small>Note 8</small>	Mbps

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.**2.** The maximum operating frequencies of the CPU/peripheral hardware clock ( $f_{CLK}$ ) are:HS (high-speed main) mode: 24 MHz ( $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )16 MHz ( $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )**3.** The smaller maximum transfer rate derived by using  $f_{MCK}/12$  or the following expression is the valid maximum transfer rate.Expression for calculating the transfer rate when  $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  and  $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ 

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \quad [\text{bps}]$$

## NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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