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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WQFN Exposed Pad
Supplier Device Package	24-HWQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1037adna-u0

○ ROM, RAM capacities

Code flash	Data flash	RAM	20 pins	24 pins	30 pins
16 KB	2 KB	2 KB	—	—	R5F102AA
	—		—	—	R5F103AA
	2 KB	1.5 KB	R5F1026A ^{Note 1}	R5F1027A ^{Note 1}	—
	—		R5F1036A ^{Note 1}	R5F1037A ^{Note 1}	—
12 KB	2KB	1 KB	R5F10269 ^{Note 1}	R5F10279 ^{Note 1}	R5F102A9
	—		R5F10369 ^{Note 1}	R5F10379 ^{Note 1}	R5F103A9
8 KB	2 KB	768 B	R5F10268 ^{Note 1}	R5F10278 ^{Note 1}	R5F102A8
	—		R5F10368 ^{Note 1}	R5F10378 ^{Note 1}	R5F103A8
4 KB	2KB	512 B	R5F10267	R5F10277	R5F102A7
	—		R5F10367	R5F10377	R5F103A7
2 KB	2 KB	256 B	R5F10266 ^{Note 2}	—	—
	—		R5F10366 ^{Note 2}	—	—

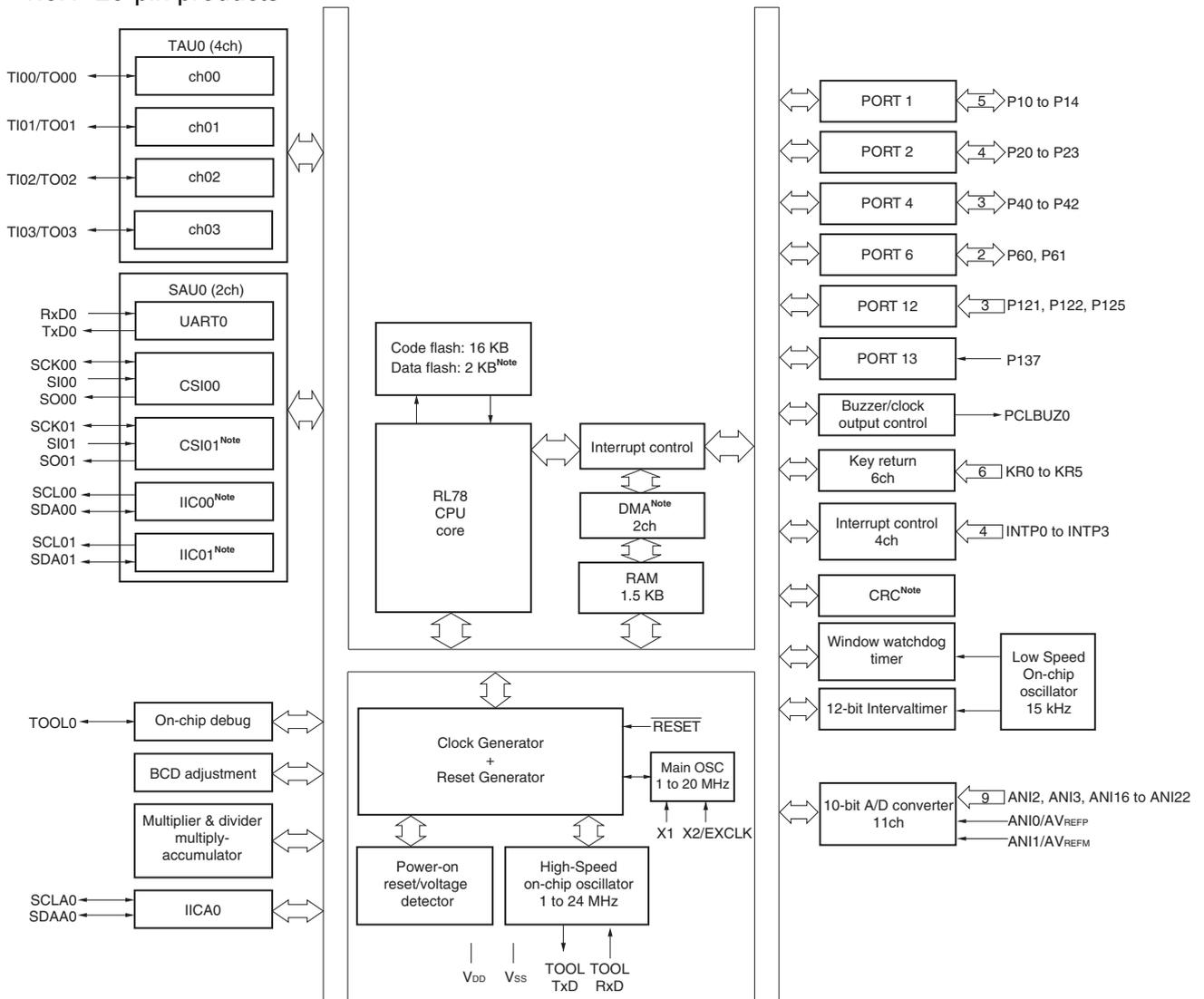
Notes 1. This is 640 bytes when the self-programming function or data flash function is used. (For details, see **CHAPTER 3 CPU ARCHITECTURE.**)

2. The self-programming function cannot be used for R5F10266 and R5F10366.

Caution When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

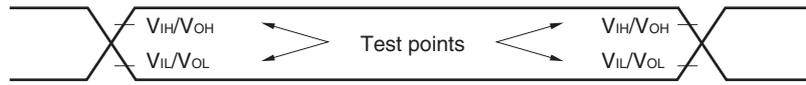
1.6 Block Diagram

1.6.1 20-pin products

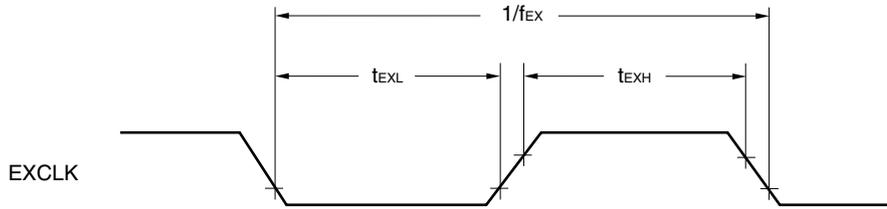


Note Provided only in the R5F102 products.

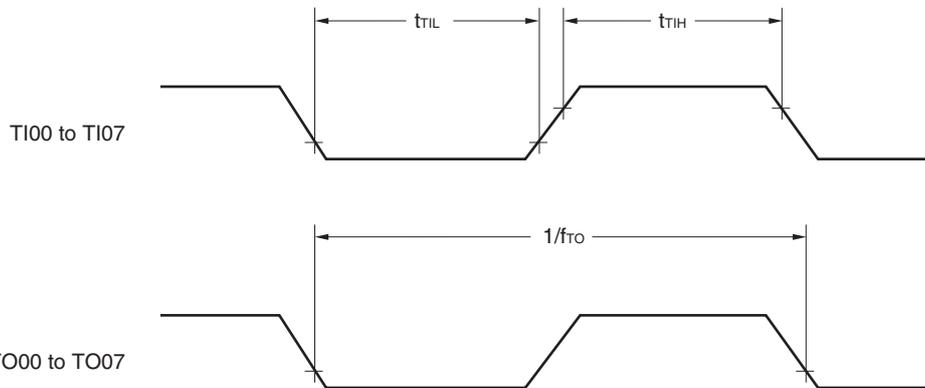
AC Timing Test Point



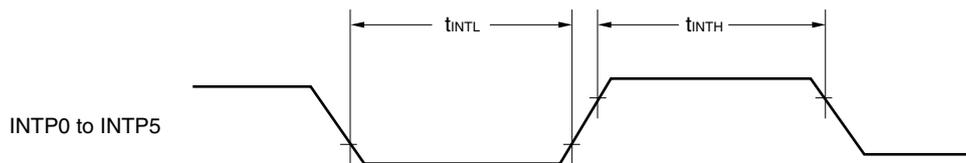
External Main System Clock Timing



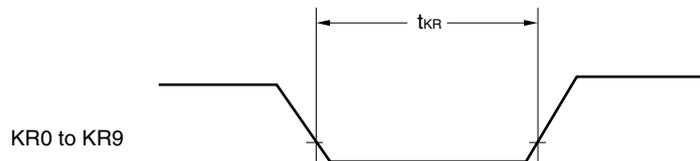
TI/TO Timing



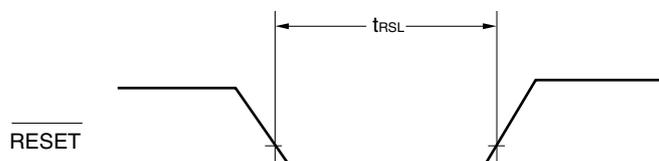
Interrupt Request Input Timing



Key Interrupt Input Timing



RESET Input Timing

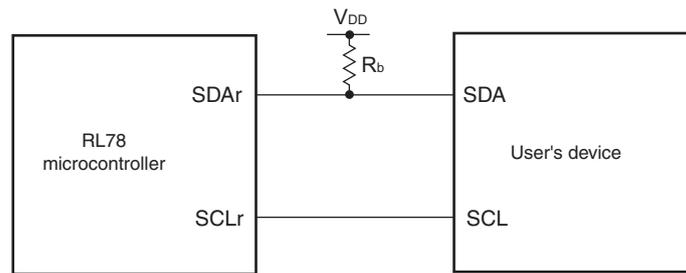
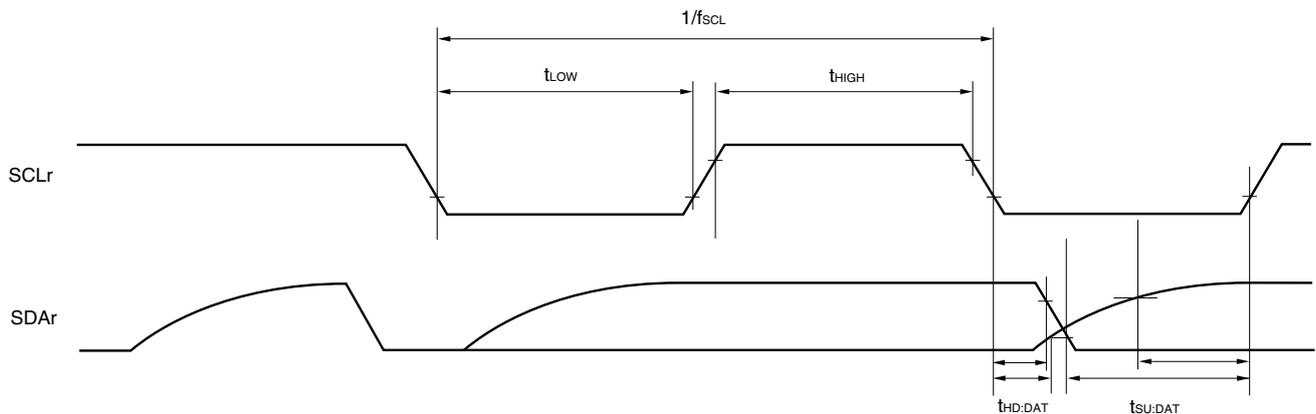


(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 4}	t_{KCY2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$20\text{ MHz} < f_{MCK}$	$8/f_{MCK}$		–		ns
			$f_{MCK} \leq 20\text{ MHz}$	$6/f_{MCK}$		$6/f_{MCK}$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$16\text{ MHz} < f_{MCK}$	$8/f_{MCK}$		–		ns
			$f_{MCK} \leq 16\text{ MHz}$	$6/f_{MCK}$		$6/f_{MCK}$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$6/f_{MCK}$ and 500		$6/f_{MCK}$ and 500		ns
$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		–		$6/f_{MCK}$ and 750		ns		
SCKp high-/low-level width	t_{KH2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-7$		$t_{KCY2}/2-7$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-8$		$t_{KCY2}/2-8$		ns
	t_{KL2}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-18$		$t_{KCY2}/2-18$		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		–		$t_{KCY2}/2-18$		ns
Slp setup time (to SCKp \uparrow) ^{Note 1}	t_{SIK2}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 20$		$1/f_{MCK} + 30$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 30$		$1/f_{MCK} + 30$		ns
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		–		$1/f_{MCK} + 30$		ns
Slp hold time (from SCKp \uparrow) ^{Note 2}	t_{KSI2}			$1/f_{MCK} + 31$		$1/f_{MCK} + 31$		ns
Delay time from SCKp \downarrow to SOp output ^{Note 3}	t_{KSO2}	$C = 30\text{ pF}$ ^{Note 4}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$2/f_{MCK} + 44$		$2/f_{MCK} + 110$	ns
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$2/f_{MCK} + 75$		$2/f_{MCK} + 110$	ns
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		–		$2/f_{MCK} + 110$	ns

- Notes**
1. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 2. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 3. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The delay time to SOp output becomes “from SCKp \uparrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the Slp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

- Remarks 1.** R_b [Ω]: Communication line (SDAr) pull-up resistance
 C_b [F]: Communication line (SCLr, SDAr) load capacitance
2. r : IIC number ($r = 00, 01, 11, 20$), h : = POM number ($h = 0, 1, 4, 5$)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m : Unit number ($m = 0, 1$), n : Channel number (0, 1, 3))
 4. Simplified I²C mode is supported only by the R5F102 products.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)**(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCK00 cycle time	t _{KCY1}	t _{KCY1} ≥ 2/fCLK 4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	200		1150		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	300		1150		ns
SCK00 high-level width	t _{KH1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	t _{KCY1} /2 – 120		t _{KCY1} /2 – 120		ns
SCK00 low-level width	t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	t _{KCY1} /2 – 7		t _{KCY1} /2 – 50		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	t _{KCY1} /2 – 10		t _{KCY1} /2 – 50		ns
SI00 setup time (to SCK00↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	58		479		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	121		479		ns
SI00 hold time (from SCK00↑) ^{Note 1}	t _{KS1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	10		10		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	10		10		ns
Delay time from SCK00↓ to SO00 output ^{Note 1}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		60		60	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		130		130	ns
SI00 setup time (to SCK00↓) ^{Note 2}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	23		110		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	33		110		ns
SI00 hold time (from SCK00↓) ^{Note 2}	t _{KS1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	10		10		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	10		10		ns
Delay time from SCK00↑ to SO00 output ^{Note 2}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		10		10	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		10		10	ns

(Notes, Caution, and Remarks are listed on the next page.)

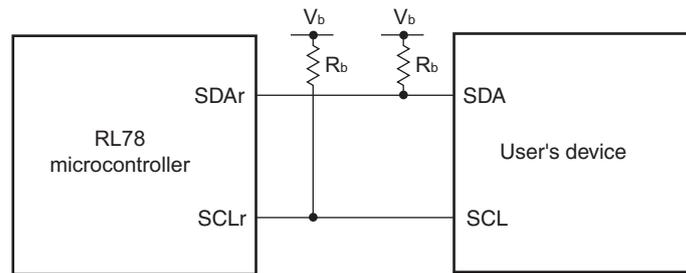
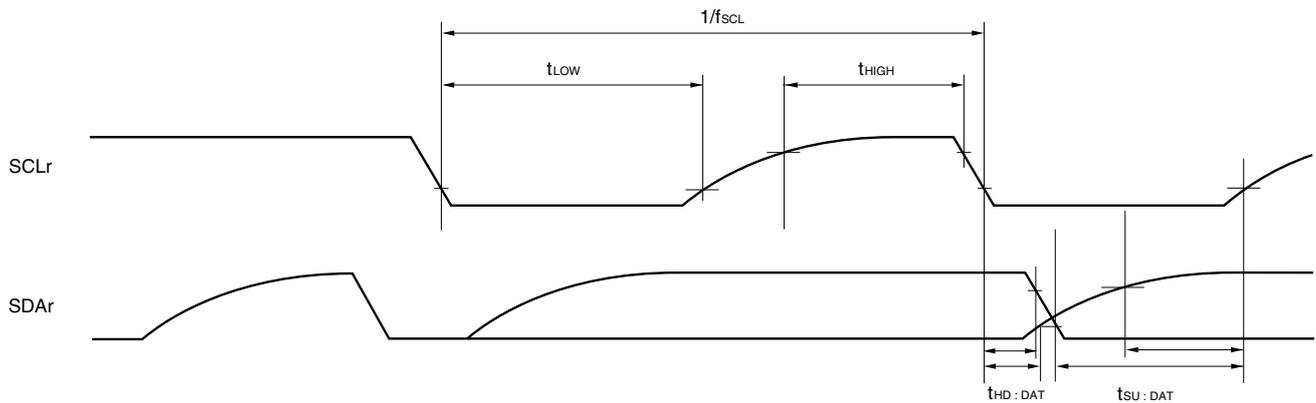
(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	20 MHz < f _{MCK} ≤ 24 MHz	12/f _{MCK}		–		ns
			8 MHz < f _{MCK} ≤ 20 MHz	10/f _{MCK}		–		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/f _{MCK}		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	20 MHz < f _{MCK} ≤ 24 MHz	16/f _{MCK}		–		ns
			16 MHz < f _{MCK} ≤ 20 MHz	14/f _{MCK}		–		ns
			8 MHz < f _{MCK} ≤ 16 MHz	12/f _{MCK}		–		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	20 MHz < f _{MCK} ≤ 24 MHz	36/f _{MCK}		–		ns
			16 MHz < f _{MCK} ≤ 20 MHz	32/f _{MCK}		–		ns
			8 MHz < f _{MCK} ≤ 16 MHz	26/f _{MCK}		–		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		16/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		t _{KCY2} /2 – 12		t _{KCY2} /2 – 50		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		t _{KCY2} /2 – 18		t _{KCY2} /2 – 50		ns
Slp setup time (to SCKp↑) ^{Note 3}	t _{SIK2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _{DD} ≤ 4.0 V		1/f _{MCK} + 20		1/f _{MCK} + 30		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		1/f _{MCK} + 20		1/f _{MCK} + 30		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
Slp hold time (from SCKp↑) ^{Note 4}	t _{KSJ2}			1/f _{MCK} + 31		1/f _{MCK} + 31		ns
Delay time from SCKp↓ to SOP output ^{Note 5}	t _{KSO2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			2/f _{MCK} + 120		2/f _{MCK} + 573	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			2/f _{MCK} + 214		2/f _{MCK} + 573	ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ			2/f _{MCK} + 573		2/f _{MCK} + 573	ns

- Notes**
1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps
 2. Use it with V_{DD} ≥ V_b.
 3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 4. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 5. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOP output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

- Cautions**
1. Select the TTL input buffer for the Slp and SCKp pins and the N-ch open drain output (V_{DD} tolerance) mode for the SOP pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).
For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

2. CSI01 and CSI11 cannot communicate at different potential.

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

- Remarks 1.** R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b [V]: Communication line voltage
- 2.** r: IIC Number (r = 00, 20)
- 3.** f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0,1), n: Channel number (n = 0))
- 4.** Simplified I²C mode is supported only by the R5F102 products.

2.5.2 Serial interface IICA

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode LS (low-speed main) mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz			0	400	kHz
		Normal mode: f _{CLK} ≥ 1 MHz	0	100			kHz
Setup time of restart condition	t _{SU:STA}		4.7		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}		4.0		0.6		μs
Hold time when SCLA0 = "L"	t _{LOW}		4.7		1.3		μs
Hold time when SCLA0 = "H"	t _{HIGH}		4.0		0.6		μs
Data setup time (reception)	t _{SU:DAT}		250		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		0	3.45	0	0.9	μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		μs
Bus-free time	t _{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

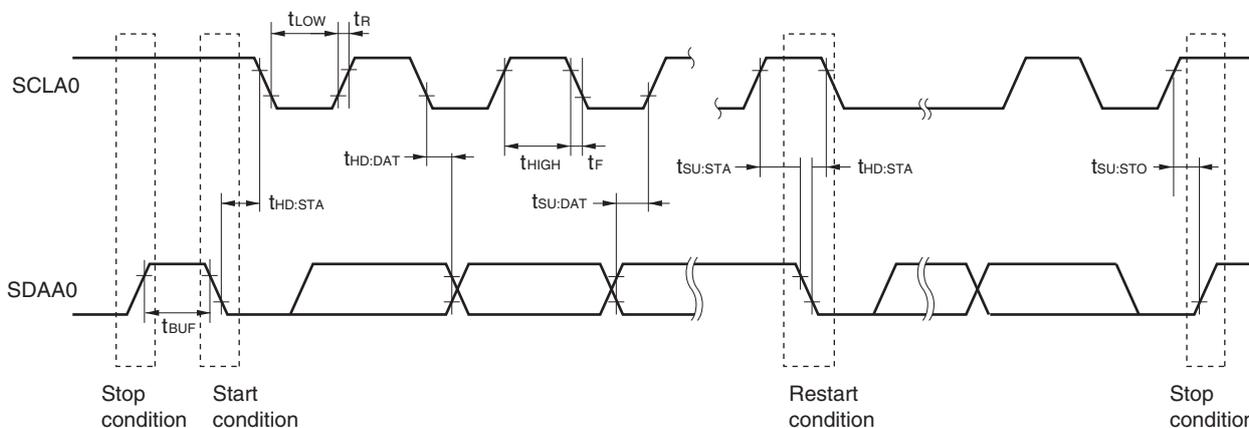
Caution Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV _{REFP} Reference voltage (-) = AV _{REFM}	Reference voltage (+) = V _{DD} Reference voltage (-) = V _{SS}	Reference voltage (+) = V _{BGR} Reference voltage (-) = AV _{REFM}
ANI0 to ANI3	Refer to 28.6.1 (1) .	Refer to 28.6.1 (3) .	Refer to 28.6.1 (4) .
ANI16 to ANI22			
Internal reference voltage Temperature sensor output voltage	Refer to 28.6.1 (1) .		-

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 1.8 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}		1.2	±3.5	LSB
				1.2	±7.0 ^{Note 4}	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI2, ANI3	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125	39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875	39	μs
			1.8 V ≤ V _{DD} ≤ 5.5 V	17	39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375	39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625	39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17	39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}			±0.25	%FSR
					±0.50 ^{Note 4}	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}			±0.25	%FSR
					±0.50 ^{Note 4}	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}			±2.5	LSB
					±5.0 ^{Note 4}	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}			±1.5	LSB
					±2.0 ^{Note 4}	LSB
Analog input voltage	V _{AIN}	ANI2, ANI3	0		AV _{REFP}	V
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)			V _{BGR} ^{Note 5}	V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)			V _{TMP25} ^{Note 5}	V

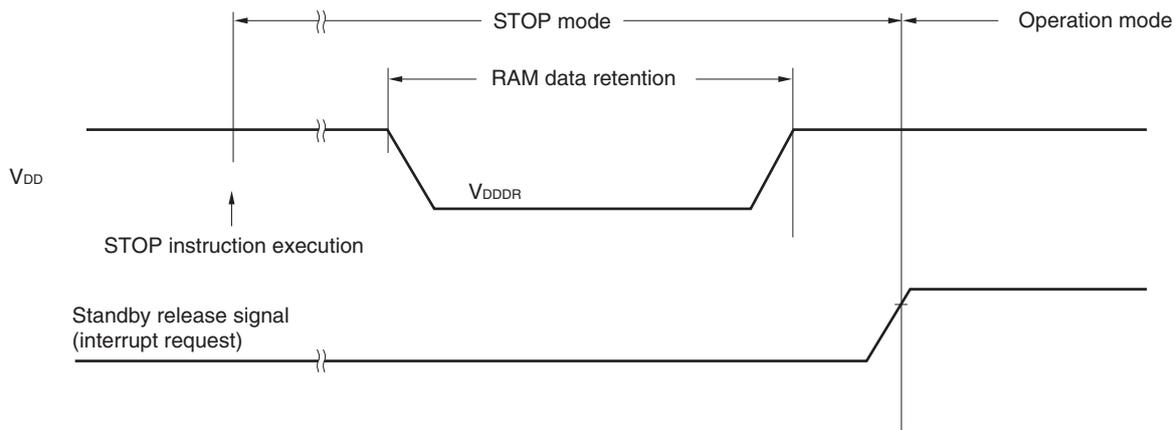
(Notes are listed on the next page.)

<R> 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{DDDR}		1.46 ^{Note}		5.5	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



2.8 Flash Memory Programming Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f _{CLK}		1		24	MHz
Code flash memory rewritable times <small>Notes 1, 2, 3</small>	C _{erwr}	Retained for 20 years T _A = 85°C	1,000			Times
Data flash memory rewritable times <small>Notes 1, 2, 3</small>		Retained for 1 year T _A = 25°C		1,000,000		
		Retained for 5 years T _A = 85°C	100,000			
		Retained for 20 years T _A = 85°C	10,000			

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library
 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

3.3.2 Supply current characteristics

(1) 20-, 24-pin products

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit			
Supply current ^{Note 1}	I _{DD1}	Operating mode	HS (High-speed main) mode ^{Note 4}	f _{IH} = 24 MHz ^{Note 3}	Basic operation	V _{DD} = 5.0 V		1.5		mA		
						V _{DD} = 3.0 V		1.5				
					Normal operation	V _{DD} = 5.0 V		3.3	5.3	mA		
						V _{DD} = 3.0 V		3.3	5.3			
						f _{IH} = 16 MHz ^{Note 3}	V _{DD} = 5.0 V		2.5		3.9	mA
							V _{DD} = 3.0 V		2.5		3.9	
				f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V	Square wave input		2.8	4.7	mA			
					Resonator connection		3.0	4.8				
				f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 3.0 V	Square wave input		2.8	4.7	mA			
					Resonator connection		3.0	4.8				
				f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 5.0 V	Square wave input		1.8	2.8	mA			
					Resonator connection		1.8	2.8				
f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 3.0 V	Square wave input		1.8	2.8	mA							
	Resonator connection		1.8	2.8								

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.
3. When high-speed system clock is stopped
4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V_{DD} = 2.7 V to 5.5 V @ 1 MHz to 24 MHz

V_{DD} = 2.4 V to 5.5 V @ 1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: high-speed on-chip oscillator clock frequency
3. Temperature condition of the TYP. value is T_A = 25°C.

3.4 AC Characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (fMAIN) operation	HS (High-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V	0.04167	1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625	1	μs
		During self programming	HS (High-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V	0.04167	1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625	1	μs
External main system clock frequency	fEX	2.7 V ≤ VDD ≤ 5.5 V		1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V		1.0		16.0	MHz
External main system clock input high-level width, low-level width	tEXH, tEXL	2.7 V ≤ VDD ≤ 5.5 V		24			ns
		2.4 V ≤ VDD < 2.7 V		30			ns
TI00 to TI07 input high-level width, low-level width	tTIH, tTIL			1/fMCK + 10			ns
TO00 to TO07 output frequency	fTO	4.0 V ≤ VDD ≤ 5.5 V				12	MHz
		2.7 V ≤ VDD < 4.0 V				8	MHz
		2.4 V ≤ VDD < 2.7 V				4	MHz
PCLBUZ0, or PCLBUZ1 output frequency	fPCL	4.0 V ≤ VDD ≤ 5.5 V				16	MHz
		2.7 V ≤ VDD < 4.0 V				8	MHz
		2.4 V ≤ VDD < 2.7 V				4	MHz
INTP0 to INTP5 input high-level width, low-level width	tINTH, tINTL			1			μs
KR0 to KR9 input available width	tKR			250			ns
RESET low-level width	tRSL			10			μs

Remark fMCK: Timer array unit operation clock frequency
 (Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

(4) During communication at same potential (simplified I²C mode)

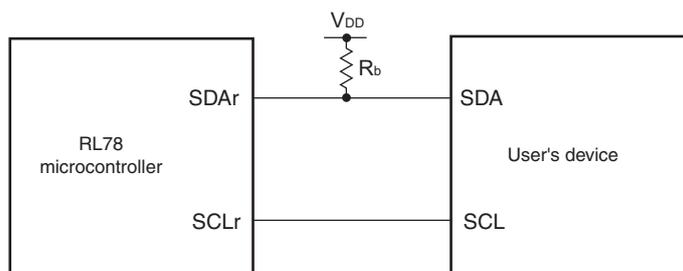
(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f _{SCL}	C _b = 100 pF, R _b = 3 kΩ		100 ^{Note 1}	kHz
Hold time when SCLr = "L"	t _{LOW}	C _b = 100 pF, R _b = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t _{HIGH}	C _b = 100 pF, R _b = 3 kΩ	4600		ns
Data setup time (reception)	t _{SU:DAT}	C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 580 ^{Note 2}		ns
Data hold time (transmission)	t _{HD:DAT}	C _b = 100 pF, R _b = 3 kΩ	0	1420	ns

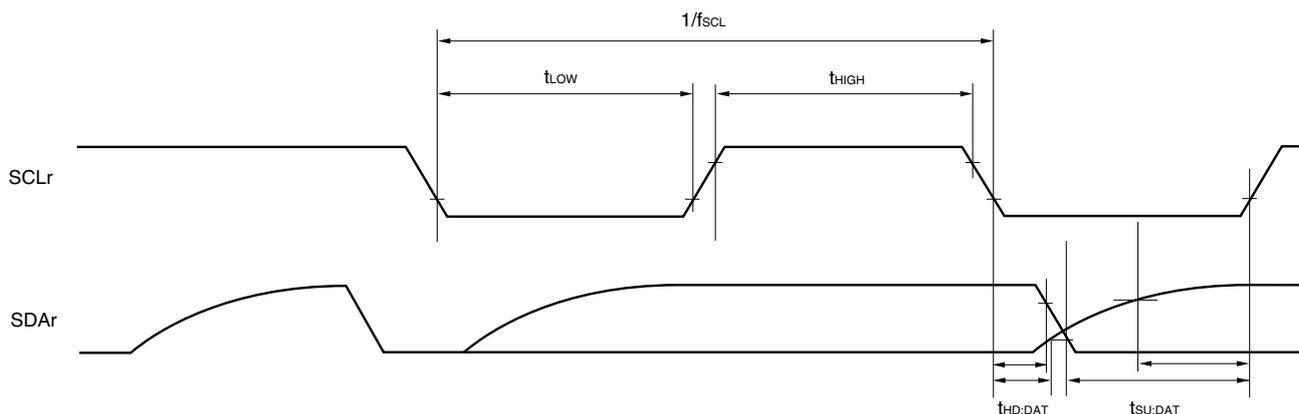
- Notes**
- The value must also be equal to or less than f_{MCK}/4.
 - Set t_{SU:DAT} so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

Caution Select the N-ch open drain output (V_{DD} tolerance) mode for SDAr by using port output mode register h (POMh).

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



- Remarks**
- R_b [Ω]: Communication line (SDAr) pull-up resistance
C_b [F]: Communication line (SCLr, SDAr) load capacitance
 - r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1, 4, 5)
 - f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0, 1), n: Channel number (0, 1, 3))

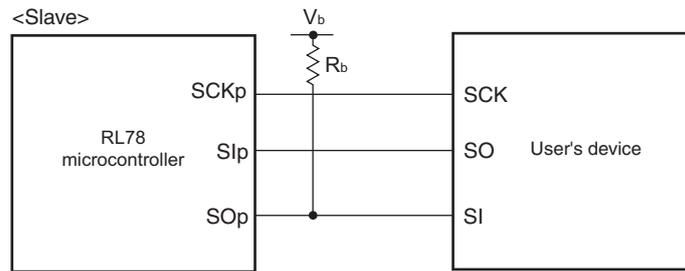
(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp \uparrow) <small>Note</small>	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	162		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	354		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	958		ns
Slp hold time (from SCKp \uparrow) <small>Note</small>	t_{KSI1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp \downarrow to SOp output <small>Note</small>	t_{KSO1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		200	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		390	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		966	ns

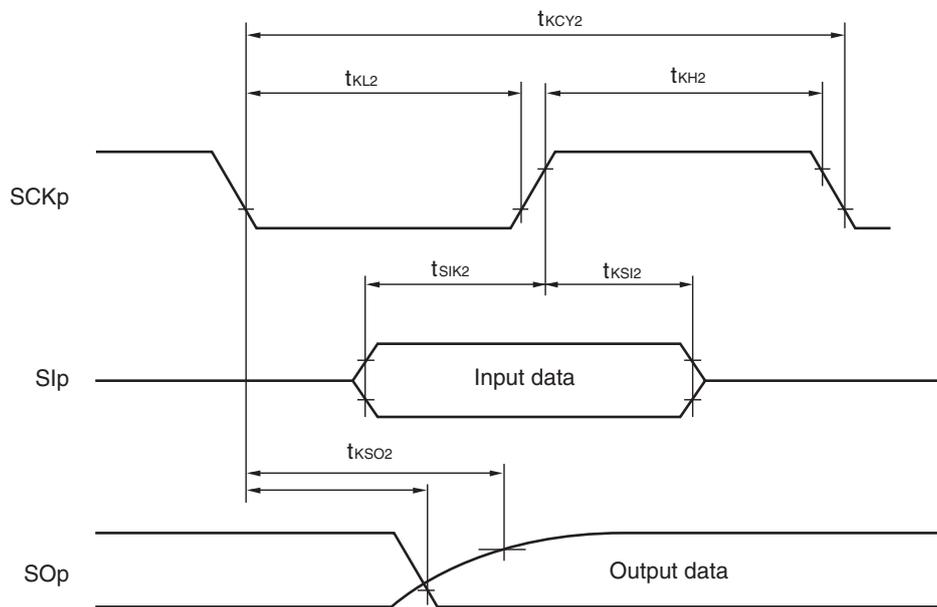
Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

(Cautions and Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

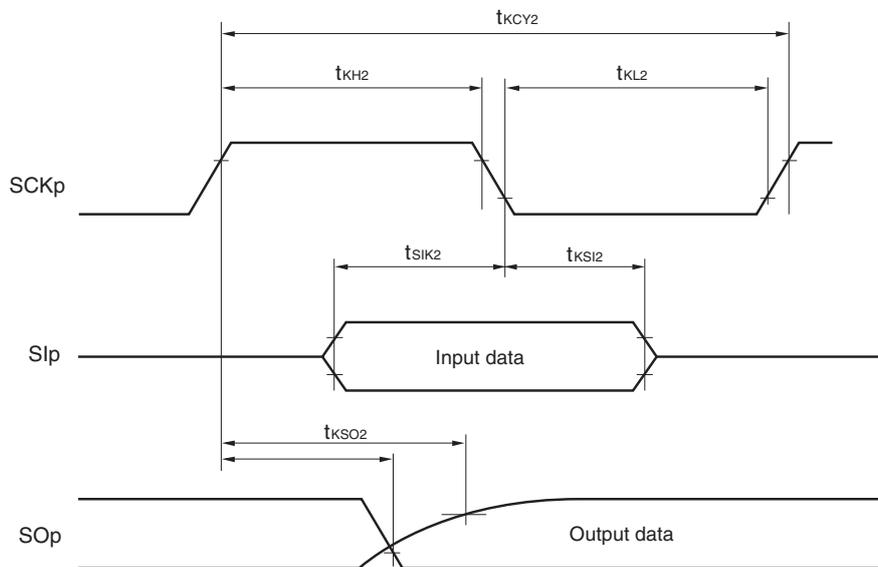


CSI mode serial transfer timing (slave mode) (during communication at different potential)
 (When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$.)



- Remarks**
1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage
 2. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Resolution	RES		8		10	bit	
Overall error ^{Note 1}	AINL	10-bit resolution		1.2	± 7.0	LSB	
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Conversion time	t _{CONV}	10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution			± 0.60	%FSR	
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution			± 0.60	%FSR	
Integral linearity error ^{Note 1}	ILE	10-bit resolution			± 4.0	LSB	
Differential linearity error ^{Note 1}	DLE	10-bit resolution			± 2.0	LSB	
Analog input voltage	V _{AIN}	ANI0 to ANI3, ANI16 to ANI22	0		V_{DD}	V	
		Internal reference voltage (HS (high-speed main) mode)	V_{BGR} ^{Note 3}			V	
		Temperature sensor output voltage (HS (high-speed main) mode)	V_{TMPS25} ^{Note 3}			V	

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

3.6.2 Temperature sensor/internal reference voltage characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		-3.6		$\text{mV}/^\circ\text{C}$
Operation stabilization wait time	t_{AMP}		5			μs

3.6.3 POR circuit characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width ^{Note}	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).

