# Renesas Electronics America Inc - R5F103A7ASP#V0 Datasheet

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CSI, I²C, UART/USART |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 30-LSSOP (0.240", 6.10mm Width) |
| Supplier Device Package | 30-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f103a7asp-v0 |

○ ROM, RAM capacities

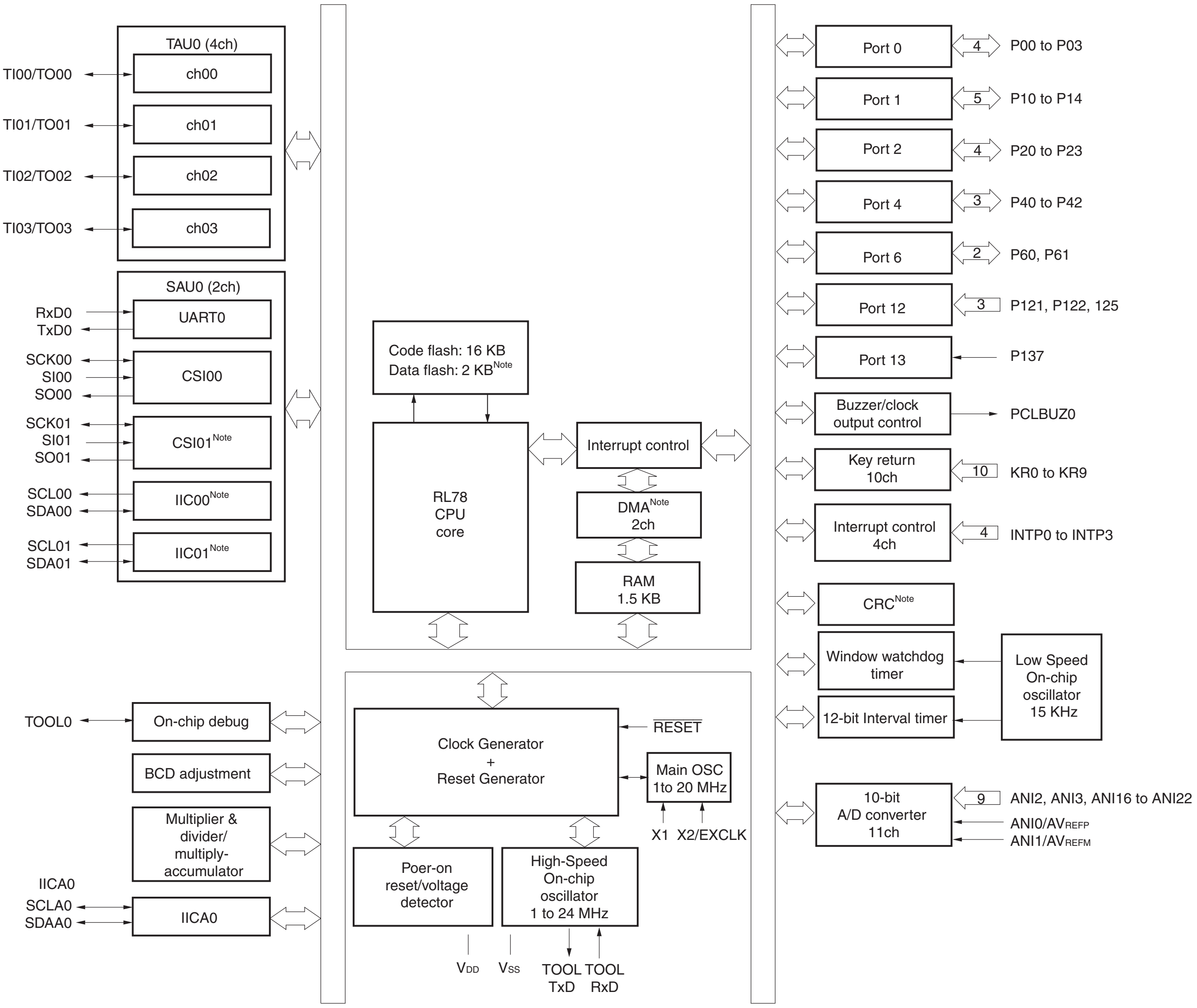
| Code flash | Data flash | RAM | 20 pins | 24 pins | 30 pins |
|---|---|---|---|---|---|
| 16 KB | 2 KB | 2 KB | — | — | R5F102AA |
|  | — |  | — | — | R5F103AA |
|  | 2 KB | 1.5 KB | R5F1026A [Note 1] | R5F1027A [Note 1] | — |
|  | — |  | R5F1036A [Note 1] | R5F1037A [Note 1] | — |
| 12 KB | 2KB | 1 KB | R5F10269 [Note 1] | R5F10279 [Note 1] | R5F102A9 |
|  | — |  | R5F10369 [Note 1] | R5F10379 [Note 1] | R5F103A9 |
| 8 KB | 2 KB | 768 B | R5F10268 [Note 1] | R5F10278 [Note 1] | R5F102A8 |
|  | — |  | R5F10368 [Note 1] | R5F10378 [Note 1] | R5F103A8 |
| 4 KB | 2KB | 512 B | R5F10267 | R5F10277 | R5F102A7 |
|  | — |  | R5F10367 | R5F10377 | R5F103A7 |
| 2 KB | 2 KB | 256 B | R5F10266 [Note 2] | — | — |
|  | — |  | R5F10366 [Note 2] | — | — |

**Notes 1.** This is 640 bytes when the self-programming function or data flash function is used. (For details, see **CHAPTER 3 CPU ARCHITECTURE**.)

**2.** The self-programming function cannot be used for R5F10266 and R5F10366.

**Caution** When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

### 1.6.2 24-pin products



**Note** Provided only in the R5F102 products.

## 2.1 Absolute Maximum Ratings

**Absolute Maximum Ratings ($T_A$ = 25°C)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | | −0.5 to + 6.5 | V |
| REGC terminal input voltage[Note1] | $V_{IREGC}$ | REGC | | −0.3 to +2.8<br>and −0.3 to $V_{DD}$ + 0.3 [Note 2] | V |
| Input Voltage | $V_{I1}$ | Other than P60, P61 | | −0.3 to $V_{DD}$ + 0.3[Note 3] | V |
| | $V_{I2}$ | P60, P61 (N-ch open drain) | | −0.3 to 6.5 | V |
| Output Voltage | $V_O$ | | | −0.3 to $V_{DD}$ + 0.3[Note 3] | V |
| Analog input voltage | $V_{AI}$ | 20-, 24-pin products: ANI0 to ANI3, ANI16 to ANI22<br>30-pin products: ANI0 to ANI3, ANI16 to ANI19 | | −0.3 to $V_{DD}$ + 0.3<br>and −0.3 to AVREF(+)+0.3[Notes 3, 4] | V |
| Output current, high | $I_{OH1}$ | Per pin | Other than P20 to P23 | −40 | mA |
| | | Total of all pins | All the terminals other than P20 to P23 | −170 | mA |
| | | | 20-, 24-pin products: P40 to P42<br>30-pin products: P00, P01, P40, P120 | −70 | mA |
| | | | 20-, 24-pin products: P00 to P03[Note 5], P10 to P14<br>30-pin products: P10 to P17, P30, P31, P50, P51, P147 | −100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P23 | −0.5 | mA |
| | | Total of all pins | | −2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | Other than P20 to P23 | 40 | mA |
| | | Total of all pins | All the terminals other than P20 to P23 | 170 | mA |
| | | | 20-, 24-pin products: P40 to P42<br>30-pin products: P00, P01, P40, P120 | 70 | mA |
| | | | 20-, 24-pin products: P00 to P03[Note 5], P10 to P14, P60, P61<br>30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P23 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | | | −40 to +85 | °C |
| Storage temperature | $T_{stg}$ | | | −65 to +150 | °C |

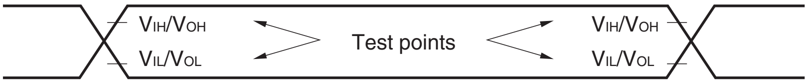
**Notes**
1. 30-pin product only.
2. Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.
3. Must be 6.5 V or lower.
4. Do not exceed $AV_{REF}(+)$ + 0.3 V in case of A/D conversion target pin.
5. 24-pin products only.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks**
1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
2. $AV_{REF}(+)$ : + side reference voltage of the A/D converter.
3. $V_{SS}$ : Reference voltage

## 2.5 Peripheral Functions Characteristics

**AC Timing Test Point**



### 2.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**
**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

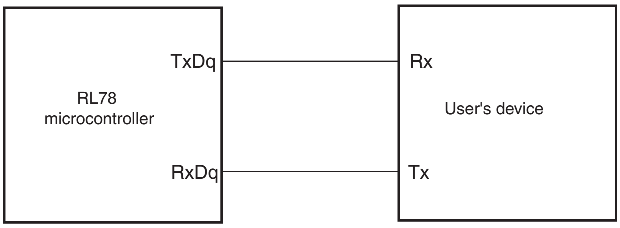
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate [Note 1] | | | | $f_{MCK}/6$ | | $f_{MCK}/6$ | bps |
| | | Theoretical value of the maximum transfer rate<br>$f_{CLK} = f_{MCK}$ [Note2] | | 4.0 | | 1.3 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

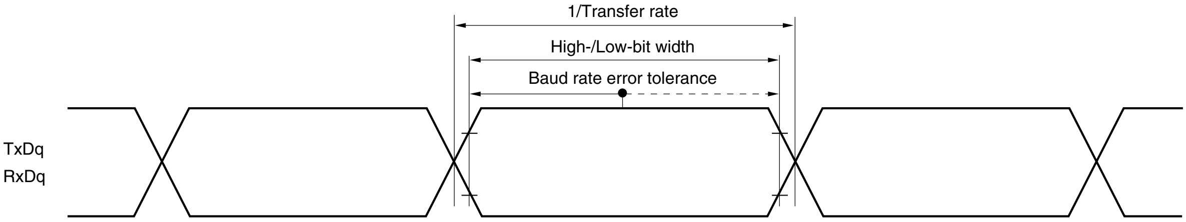
**2.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**UART mode connection diagram (during communication at same potential)**



**UART mode bit width (during communication at same potential) (reference)**



**Remarks 1.** q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

### (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) ($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time [Note4] | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 500 | | 6/$f_{MCK}$ and 500 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | 6/$f_{MCK}$ and 750 | | ns |
| SCKp high-/low-level width | $t_{KH2}$,<br>$t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–7 | | $t_{KCY2}$/2–7 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–8 | | $t_{KCY2}$/2–8 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–18 | | $t_{KCY2}$/2–18 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | $t_{KCY2}$/2–18 | | ns |
| SIp setup time (to SCKp↑) [Note 1] | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) [Note 2] | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output [Note 3] | $t_{KSO2}$ | C = 30 pF [Note4] | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 44 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 75 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | 2/$f_{MCK}$ + 110 | ns |

**Notes**

1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. C is the load capacitance of the SOp output lines.
5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Caution** Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)
### ($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate [Note4] | | Reception | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V | | | $f_{MCK}$/6<br>Note1 | | $f_{MCK}$/6<br>Note1 | bps |
| | | | | Theoretical value of the maximum transfer rate<br>$f_{MCK}$ = $f_{CLK}$ Note3 | | 4.0 | | 1.3 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V | | | $f_{MCK}$/6<br>Note1 | | $f_{MCK}$/6<br>Note1 | bps |
| | | | | Theoretical value of the maximum transfer rate<br>$f_{MCK}$ = $f_{CLK}$ Note3 | | 4.0 | | 1.3 | Mbps |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V | | | $f_{MCK}$/6<br>Notes1, 2 | | $f_{MCK}$/6<br>Notes1, 2 | bps |
| | | | | Theoretical value of the maximum transfer rate<br>$f_{MCK}$ = $f_{CLK}$ Note3 | | 4.0 | | 1.3 | Mbps |
| | | Transmission | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V | | | **Note4** | | **Note4** | bps |
| | | | | Theoretical value of the maximum transfer rate<br>$C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.8<br>Note5 | | 2.8<br>Note5 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V, | | | **Note6** | | **Note6** | bps |
| | | | | Theoretical value of the maximum transfer rate<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2<br>Note7 | | 1.2<br>Note7 | Mbps |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V | | | **Notes 2, 8** | | **Notes 2, 8** | bps |
| | | | | Theoretical value of the maximum transfer rate<br>$C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43<br>Note9 | | 0.43<br>Note9 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** Use it with $V_{DD}$ ≥ $V_b$.

**3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)

**4.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ $V_{DD}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln\,(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln\,(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

### (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)

**($T_A$ = –40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCK00 cycle time | $t_{KCY1}$ | $t_{KCY1} \ge 2/f_{CLK}$ | $4.0\ V \le V_{DD} \le 5.5\ V$,<br>$2.7\ V \le V_b \le 4.0\ V$,<br>$C_b = 20\ pF$, $R_b = 1.4\ k\Omega$ | 200 | | 1150 | | ns |
| | | | $2.7\ V \le V_{DD} < 4.0\ V$,<br>$2.3\ V \le V_b \le 2.7\ V$,<br>$C_b = 20\ pF$, $R_b = 2.7\ k\Omega$ | 300 | | 1150 | | ns |
| SCK00 high-level width | $t_{KH1}$ | $4.0\ V \le V_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$,<br>$C_b = 20\ pF$, $R_b = 1.4\ k\Omega$ | | $t_{KCY1}/2 - 50$ | | $t_{KCY1}/2 - 50$ | | ns |
| | | $2.7\ V \le V_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$,<br>$C_b = 20\ pF$, $R_b = 2.7\ k\Omega$ | | $t_{KCY1}/2 - 120$ | | $t_{KCY1}/2 - 120$ | | ns |
| SCK00 low-level width | $t_{KL1}$ | $4.0\ V \le V_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$,<br>$C_b = 20\ pF$, $R_b = 1.4\ k\Omega$ | | $t_{KCY1}/2 - 7$ | | $t_{KCY1}/2 - 50$ | | ns |
| | | $2.7\ V \le V_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$,<br>$C_b = 20\ pF$, $R_b = 2.7\ k\Omega$ | | $t_{KCY1}/2 - 10$ | | $t_{KCY1}/2 - 50$ | | ns |
| SI00 setup time (to SCK00↑) Note 1 | $t_{SIK1}$ | $4.0\ V \le V_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$,<br>$C_b = 20\ pF$, $R_b = 1.4\ k\Omega$ | | 58 | | 479 | | ns |
| | | $2.7\ V \le V_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$,<br>$C_b = 20\ pF$, $R_b = 2.7\ k\Omega$ | | 121 | | 479 | | ns |
| SI00 hold time (from SCK00↑) Note 1 | $t_{KSI1}$ | $4.0\ V \le V_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$,<br>$C_b = 20\ pF$, $R_b = 1.4\ k\Omega$ | | 10 | | 10 | | ns |
| | | $2.7\ V \le V_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$,<br>$C_b = 20\ pF$, $R_b = 2.7\ k\Omega$ | | 10 | | 10 | | ns |
| Delay time from SCK00↓ to SO00 output Note 1 | $t_{KSO1}$ | $4.0\ V \le V_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$,<br>$C_b = 20\ pF$, $R_b = 1.4\ k\Omega$ | | | 60 | | 60 | ns |
| | | $2.7\ V \le V_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$,<br>$C_b = 20\ pF$, $R_b = 2.7\ k\Omega$ | | | 130 | | 130 | ns |
| SI00 setup time (to SCK00↓) Note 2 | $t_{SIK1}$ | $4.0\ V \le V_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$,<br>$C_b = 20\ pF$, $R_b = 1.4\ k\Omega$ | | 23 | | 110 | | ns |
| | | $2.7\ V \le V_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$,<br>$C_b = 20\ pF$, $R_b = 2.7\ k\Omega$ | | 33 | | 110 | | ns |
| SI00 hold time (from SCK00↓) Note 2 | $t_{KSI1}$ | $4.0\ V \le V_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$,<br>$C_b = 20\ pF$, $R_b = 1.4\ k\Omega$ | | 10 | | 10 | | ns |
| | | $2.7\ V \le V_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$,<br>$C_b = 20\ pF$, $R_b = 2.7\ k\Omega$ | | 10 | | 10 | | ns |
| Delay time from SCK00↑ to SO00 output Note 2 | $t_{KSO1}$ | $4.0\ V \le V_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$,<br>$C_b = 20\ pF$, $R_b = 1.4\ k\Omega$ | | | 10 | | 10 | ns |
| | | $2.7\ V \le V_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$,<br>$C_b = 20\ pF$, $R_b = 2.7\ k\Omega$ | | | 10 | | 10 | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

### (4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV$_{REFM}$ (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22

**($T_A$ = –40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (–) = AV$_{REFM}$ Note 4 = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | EZS | 8-bit resolution | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | 0 | | $V_{BGR}$ Note 3 | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **28.6.2 Temperature sensor/internal reference voltage characteristics**.

**4.** When reference voltage (–) = $V_{SS}$, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = AV$_{REFM}$.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = AV$_{REFM}$.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = AV$_{REFM}$.

### 2.6.2 Temperature sensor/internal reference voltage characteristics

**($T_A$ = –40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, HS (high-speed main) mode**

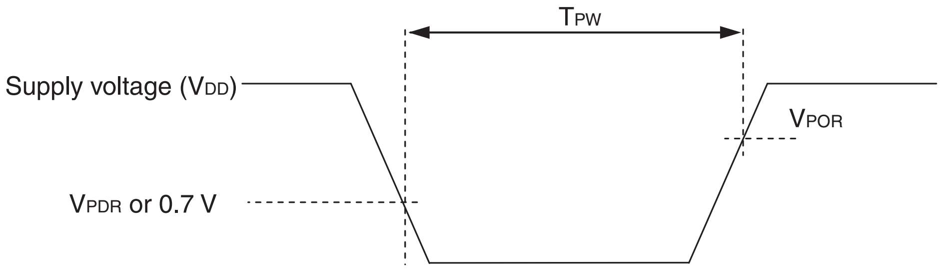
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.50 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor output voltage that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 2.6.3 POR circuit characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Power supply rise time | 1.47 | 1.51 | 1.55 | V |
| | $V_{PDR}$ | Power supply fall time | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width Note | $T_{PW}$ | | 300 | | | μs |

**Note** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 3.1 Absolute Maximum Ratings

### Absolute Maximum Ratings ($T_A$ = 25°C)

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | | −0.5 to + 6.5 | V |
| REGC terminal input voltage[Note1] | $V_{IREGC}$ | REGC | | −0.3 to +2.8<br>and −0.3 to $V_{DD}$ + 0.3 [Note 2] | V |
| Input Voltage | $V_{I1}$ | Other than P60, P61 | | −0.3 to $V_{DD}$ + 0.3[Note 3] | V |
| | $V_{I2}$ | P60, P61 (N-ch open drain) | | −0.3 to 6.5 | V |
| Output Voltage | $V_O$ | | | −0.3 to $V_{DD}$ + 0.3[Note 3] | V |
| Analog input voltage | $V_{AI}$ | 20, 24-pin products: ANI0 to ANI3, ANI16 to ANI22<br>30-pin products: ANI0 to ANI3, ANI16 to ANI19 | | −0.3 to $V_{DD}$ + 0.3<br>and −0.3 to AVREF(+)+0.3 [Notes 3, 4] | V |
| Output current, high | $I_{OH1}$ | Per pin | Other than P20 to P23 | −40 | mA |
| | | Total of all pins | All the terminals other than P20 to P23 | −170 | mA |
| | | | 20-, 24-pin products: P40 to P42<br>30-pin products: P00, P01, P40, P120 | −70 | mA |
| | | | 20-, 24-pin products: P00 to P03[Note 5], P10 to P14<br>30-pin products: P10 to P17, P30, P31, P50, P51, P147 | −100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P23 | −0.5 | mA |
| | | Total of all pins | | −2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | Other than P20 to P23 | 40 | mA |
| | | Total of all pins | All the terminals other than P20 to P23 | 170 | mA |
| | | | 20-, 24-pin products: P40 to P42<br>30-pin products: P00, P01, P40, P120 | 70 | mA |
| | | | 20-, 24-pin products: P00 to P03 [Note 5], P10 to P14, P60, P61<br>30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P23 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | | | −40 to +105 | °C |
| Storage temperature | $T_{stg}$ | | | −65 to +150 | °C |

**Notes 1.** 30-pin product only.

**2.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 μF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.

**3.** Must be 6.5 V or lower.

**4.** Do not exceed $AV_{REF}(+)$ + 0.3 V in case of A/D conversion target pin.

**5.** 24-pin products only.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** $AV_{REF}(+)$ : + side reference voltage of the A/D converter.

**3.** $V_{SS}$ : Reference voltage

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (2/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low[Note 1] | $I_{OL1}$ | 20-, 24-pin products:<br>Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42<br>30-pin products:<br>Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | | | 8.5[Note 2] | mA |
| | | Per pin for P60, P61 | | | | 15.0[Note 2] | mA |
| | | 20-, 24-pin products:<br>Total of P40 to P42<br>30-pin products:<br>Total of P00, P01, P40, P120<br>(When duty ≤ 70%[Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 25.5 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 9.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 1.8 | mA |
| | | 20-, 24-pin products:<br>Total of P00 to P03[Note 4], P10 to P14, P60, P61<br>30-pin products:<br>Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147<br>(When duty ≤ 70%[Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 27.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 5.4 | mA |
| | | Total of all pins (When duty ≤ 70%[Note 3]) | | | | 65.5 | mA |
| | $I_{OL2}$ | Per pin for P20 to P23 | | | | 0.4 | mA |
| | | Total of all pins | | | | 1.6 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $V_{SS}$ pin.

**2.** However, do not exceed the total current value.

**3.** The output current value under conditions where the duty factor ≤ 70%.

If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**4.** 24-pin products only.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### (1) 20-, 24-pin products

**($T_A$ = −40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current [Note 1] | $I_{DD2}$ [Note 2] | HALT mode | HS (High-speed main) mode [Note 6] | $f_{IH}$ = 24 MHz [Note 4] | $V_{DD}$ = 5.0 V | | 440 | 2230 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 2230 | |
| | | | | $f_{IH}$ = 16 MHz [Note 4] | $V_{DD}$ = 5.0 V | | 400 | 1650 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 1650 | |
| | | | | $f_{MX}$ = 20 MHz [Note 3], $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 20 MHz [Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 10 MHz [Note 3], $V_{DD}$ = 5.0 V | Square wave input | | 190 | 1010 | μA |
| | | | | | Resonator connection | | 260 | 1090 | |
| | | | | $f_{MX}$ = 10 MHz [Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 190 | 1010 | μA |
| | | | | | Resonator connection | | 260 | 1090 | |
| | $I_{DD3}$ [Note 5] | STOP mode | $T_A$ = −40°C | | | | 0.19 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.32 | 0.80 | |
| | | | $T_A$ = +70°C | | | | 0.48 | 1.20 | |
| | | | $T_A$ = +85°C | | | | 0.74 | 2.20 | |
| | | | $T_A$ = +105°C | | | | 1.50 | 10.20 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except temperature condition of the TYP. value is $T_A$ = 25°C, other than STOP mode

## 3.4 AC Characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (High-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.04167 | | 1 | μs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | μs |
| | | During self programming | HS (High-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.04167 | | 1 | μs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | μs |
| External main system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 1.0 | | 16.0 | MHz |
| External main system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 30 | | | ns |
| TI00 to TI07 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 | | | ns |
| TO00 to TO07 output frequency | $f_{TO}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | | | 12 | MHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | | | 8 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | | | 4 | MHz |
| PCLBUZ0, or PCLBUZ1 output frequency | $f_{PCL}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | | | 16 | MHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | | | 8 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | | | 4 | MHz |
| INTP0 to INTP5 input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | | | | 1 | | | μs |
| KR0 to KR9 input available width | $t_{KR}$ | | | | 250 | | | ns |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | | 10 | | | μs |

**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

### (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
### ($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time [Note4] | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 12/$f_{MCK}$ and 1000 | | ns |
| SCKp high-/low-level width | $t_{KH2}$,<br>$t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–14 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–16 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–36 | | ns |
| SIp setup time (to SCKp↑) [Note 1] | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) [Note 2] | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output [Note 3] | $t_{KSO2}$ | C = 30 pF [Note4] | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 66 | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 113 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

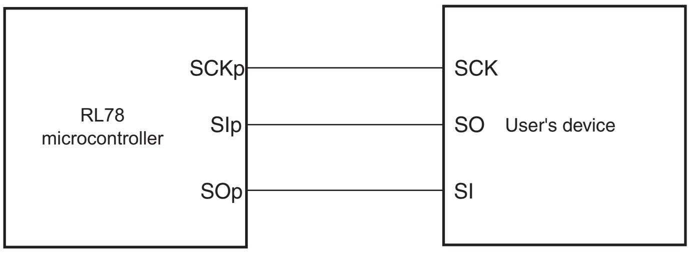
**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SOp output lines.

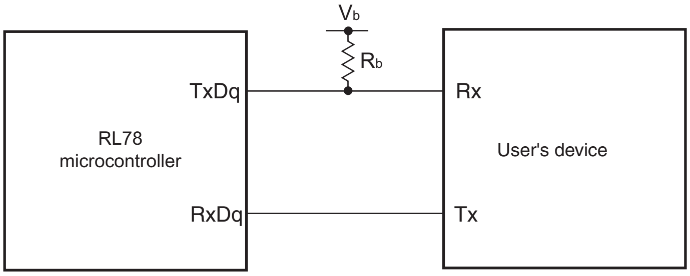
**5.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Caution** Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

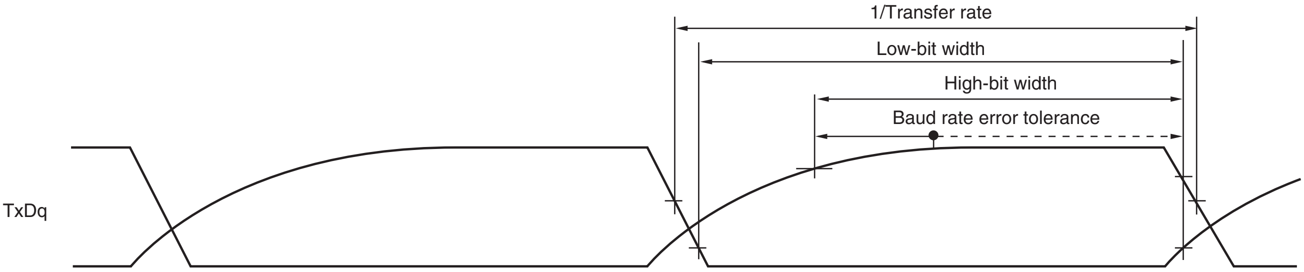
**CSI mode connection diagram (during communication at same potential)**

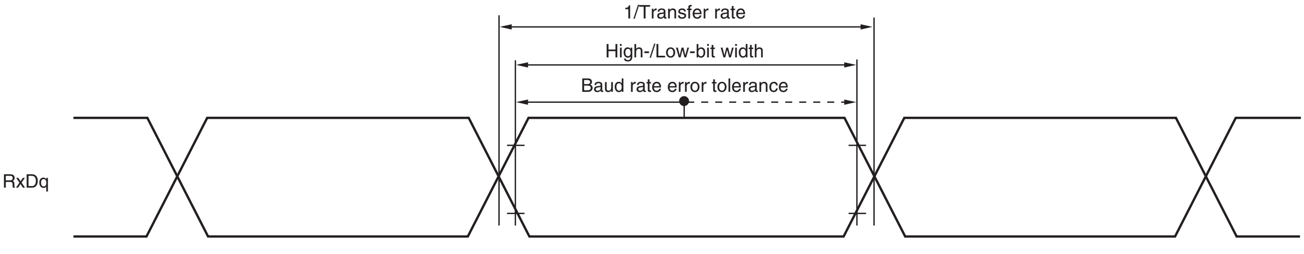


**UART mode connection diagram (during communication at different potential)**



**UART mode bit width (during communication at different potential) (reference)**





**Remarks 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance, $C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**4.** UART0 of the 20- and 24-pin products supports communication at different potential only when the peripheral I/O redirection function is not used.

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 600 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 1000 | | ns |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V,<br>$C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 2300 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}/2$ –150 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}/2$ –340 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V,<br>$C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}/2$ –916 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}/2$ –24 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}/2$ –36 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V,<br>$C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}/2$ –100 | | ns |

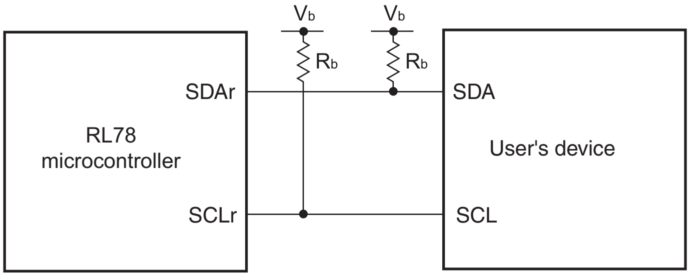
**Cautions 1.** Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.

**2.** CSI01 and CSI11 cannot communicate at different potential.

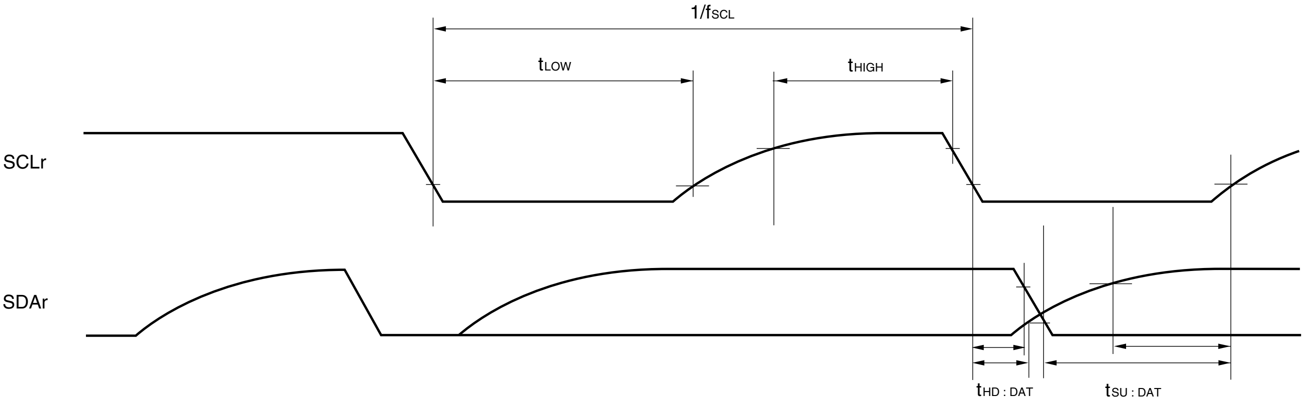
**Remarks 1.** $R_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$ [F]: Communication line (SCKp, SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20)

**Simplified I²C mode connection diagram (during communication at different potential)**



**Simplified I²C mode serial transfer timing (during communication at different potential)**



**Remarks 1.** $R_b$ [Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$ [F]: Communication line (SDAr, SCLr) load capacitance, $V_b$ [V]: Communication line voltage

**2.** r: IIC Number (r = 00, 20)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0,1), n: Channel number (n = 0))

### (3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = $V_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (–) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution | | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI3, ANI16 to ANI22 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error[Notes 1, 2] | EZS | 10-bit resolution | | | | ±0.60 | %FSR |
| Full-scale error[Notes 1, 2] | EFS | 10-bit resolution | | | | ±0.60 | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution | | | | ±4.0 | LSB |
| Differential linearity error[Note 1] | DLE | 10-bit resolution | | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI3, ANI16 to ANI22 | | 0 | | $V_{DD}$ | V |
| | | Internal reference voltage<br>(HS (high-speed main) mode) | | $V_{BGR}$[Note 3] | | | V |
| | | Temperature sensor output voltage<br>(HS (high-speed main) mode) | | $V_{TMPS25}$[Note 3] | | | V |

**Notes** **1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

| Rev. | Date | Description | |
|---|---|---|---|
| | | **Page** | **Summary** |
| 1.00 | Dec 10, 2012 | - | First Edition issued |
| 2.00 | Sep 06, 2013 | 1 | Modification of 1.1 Features |
| | | 3 | Modification of 1.2 List of Part Numbers |
| | | 4 | Modification of Table 1-1. List of Ordering Part Numbers, Note, and Caution |
| | | 7 to 9 | Modification of package name in 1.4.1 to 1.4.3 |
| | | 14 | Modification of tables in 1.7 Outline of Functions |
| | | 17 | Modification of description of table in 2.1 Absolute Maximum Ratings ($T_A$ = 25°C) |
| | | 18 | Modification of table, Note, and Caution in 2.2.1 X1 oscillator characteristics |
| | | 18 | Modification of table in 2.2.2 On-chip oscillator characteristics |
| | | 19 | Modification of Note 3 in 2.3.1 Pin characteristics (1/4) |
| | | 20 | Modification of Note 3 in 2.3.1 Pin characteristics (2/4) |
| | | 23 | Modification of Notes 1 and 2 in (1) 20-, 24-pin products (1/2) |
| | | 24 | Modification of Notes 1 and 3 in (1) 20-, 24-pin products (2/2) |
| | | 25 | Modification of Notes 1 and 2 in (2) 30-pin products (1/2) |
| | | 26 | Modification of Notes 1 and 3 in (2) 30-pin products (2/2) |
| | | 27 | Modification of (3) Peripheral functions (Common to all products) |
| | | 28 | Modification of table in 2.4 AC Characteristics |
| | | 29 | Addition of Minimum Instruction Execution Time during Main System Clock Operation |
| | | 30 | Modification of figures of AC Timing Test Point and External Main System Clock Timing |
| | | 31 | Modification of figure of AC Timing Test Point |
| | | 31 | Modification of description and Note 2 in (1) During communication at same potential (UART mode) |
| | | 32 | Modification of description in (2) During communication at same potential (CSI mode) |
| | | 33 | Modification of description in (3) During communication at same potential (CSI mode) |
| | | 34 | Modification of description in (4) During communication at same potential (CSI mode) |
| | | 36 | Modification of table and Note 2 in (5) During communication at same potential (simplified I$^2$C mode) |
| | | 38, 39 | Modification of table and Notes 1 to 9 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) |
| | | 40 | Modification of Remarks 1 to 3 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) |
| | | 41 | Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) |
| | | 42 | Modification of Caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) |
| | | 43 | Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3) |
| | | 44 | Modification of table and Notes 1 and 2 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3) |
| | | 45 | Modification of table, Note 1, and Caution 1 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3) |
| | | 47 | Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) |
| | | 50 | Modification of table, Note 1, and Caution 1 in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I$^2$C mode) |
| | | 52 | Modification of Remark in 2.5.2 Serial interface IICA |
| | | 53 | Addition of table to 2.6.1 A/D converter characteristics |
| | | 53 | Modification of description in 2.6.1 (1) |
| | | 54 | Modification of Notes 3 to 5 in 2.6.1 (1) |
| | | 54 | Modification of description and Notes 2 to 4 in 2.6.1 (2) |

## NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.