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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f103a8asp-v0

1.3.2 On-chip oscillator characteristics

(1) High-speed on-chip oscillator oscillation frequency of the R5F102 products

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	$T_A = -20$ to $+85$ °C	-1.0	+1.0	%
	$T_A = -40$ to -20 °C	-1.5	+1.5	
	$T_A = +85$ to $+105$ °C	-2.0	+2.0	

(2) High-speed on-chip oscillator oscillation frequency of the R5F103 products

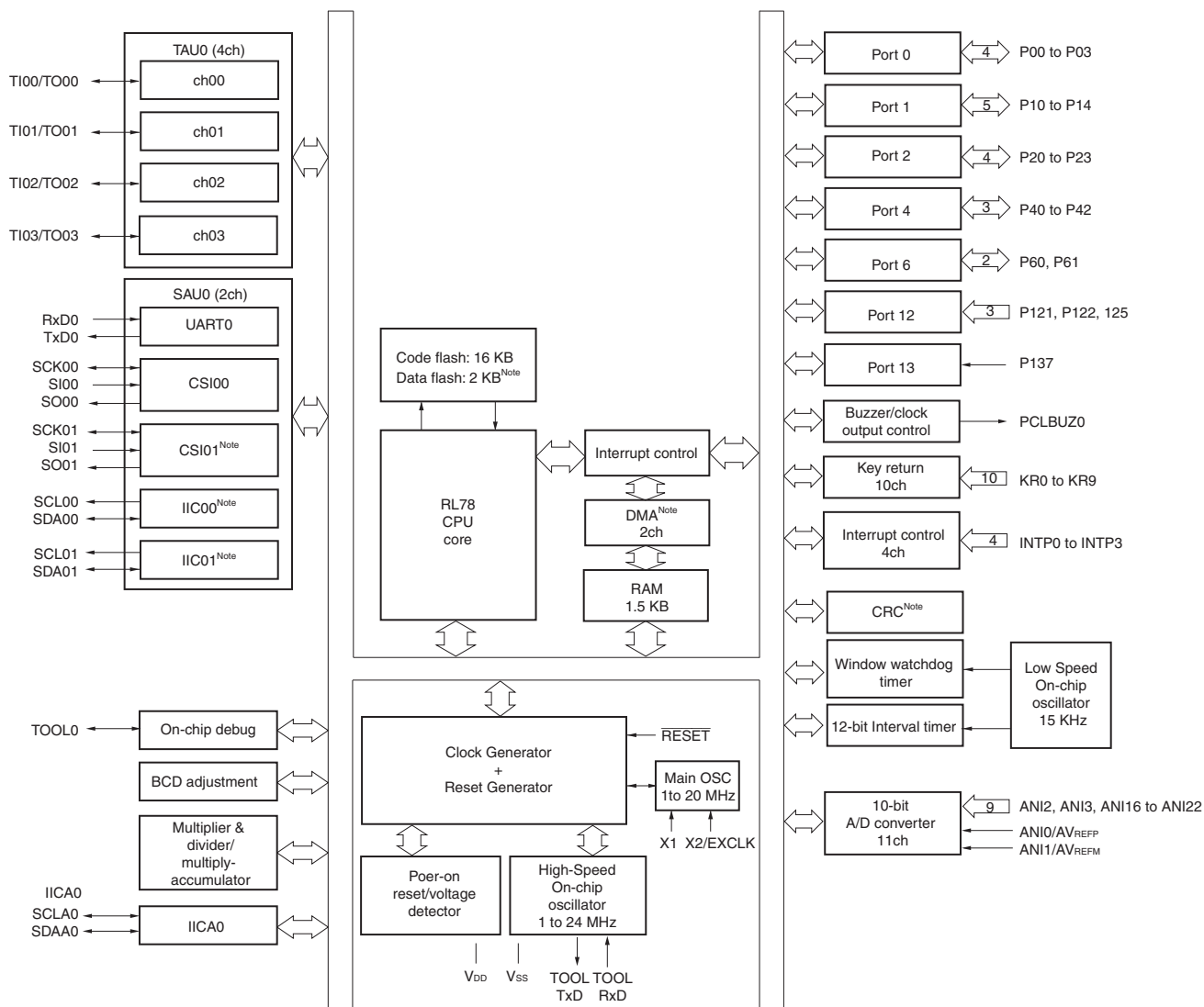
Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	$T_A = -40$ to $+85$ °C	-5.0	+5.0	%

1.3.3 Peripheral Functions

The following are differences in peripheral functions between the R5F102 products and the R5F103 products.

RL78/G12		R5F102 product		R5F103 product	
		20, 24 pin product	30 pin product	20, 24 pin product	30 pin product
Serial interface	UART	1 channel	3 channels	1 channel	
	CSI	2 channels	3 channels	1 channel	
	Simplified I ² C	2 channels	3 channels	None	
DMA function		2 channels		None	
Safety function	CRC operation	Yes		None	
	RAM guard	Yes		None	
	SFR guard	Yes		None	

1.6.2 24-pin products



Note Provided only in the R5F102 products.

1.7 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

<R>

Item		20-pin		24-pin		30-pin	
		R5F1026x	R5F1036x	R5F1027x	R5F1037x	R5F102Ax	R5F103Ax
Code flash memory		2 to 16 KB ^{Note 1}		4 to 16 KB			
Data flash memory		2 KB	–	2 KB	–	2 KB	–
RAM		256 B to 1.5 KB		512 B to 1.5 KB		512 B to 2KB	
Address space		1 MB					
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode : 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode : 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode : 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V)					
	High-speed on-chip oscillator clock	HS (High-speed main) mode : 1 to 24 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode : 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode : 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V)					
Low-speed on-chip oscillator clock		15 kHz (TYP)					
General-purpose register		(8-bit register × 8) × 4 banks					
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f _{IH} = 24 MHz operation)					
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)					
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.					
I/O port	Total	18		22		26	
	CMOS I/O	12 (N-ch O.D. I/O [V _{DD} withstand voltage]: 4)		16 (N-ch O.D. I/O [V _{DD} withstand voltage]: 5)		21 (N-ch O.D. I/O [V _{DD} withstand voltage]: 9)	
	CMOS input	4		4		3	
	N-ch open-drain I/O (6 V tolerance)	2					
Timer	16-bit timer	4 channels				8 channels	
	Watchdog timer	1 channel					
	12-bit Interval timer	1 channel					
	Timer output	4 channels (PWM outputs: 3 ^{Note 3})				8 channels (PWM outputs: 7 ^{Note 3} , ^{Note 2})	

Notes 1. The self-programming function cannot be used in the R5F10266 and R5F10366.

2. The maximum number of channels when PIOR0 is set to 1.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). (See **6.9.3 Operation as multiple PWM output function.**)

Caution When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

(1) 20-, 24-pin products

 $(T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	I _{DD2} ^{Note 2}	HALT mode	HS (High-speed main) mode ^{Note 6}	f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		440	1210	μA	
					V _{DD} = 3.0 V		440	1210		
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		400	950	μA	
					V _{DD} = 3.0 V		400	950		
				LS (Low-speed main) mode ^{Note 6}	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V		270	542	μA
						V _{DD} = 2.0 V		270	542	
			HS (High-speed main) mode ^{Note 6}	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		280	1000	μA	
					Resonator connection		450	1170		
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		280	1000	μA	
					Resonator connection		450	1170		
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		190	590	μA	
					Resonator connection		260	660		
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		190	590	μA	
					Resonator connection		260	660		
			LS (Low-speed main) mode ^{Note 6}	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		110	360	μA	
					Resonator connection		150	416		
				f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input		110	360	μA	
					Resonator connection		150	416		
	I _{DD3} ^{Note 5}	STOP mode	T _A = −40°C					0.19	0.50	μA
			T _A = +25°C					0.24	0.50	
			T _A = +50°C					0.32	0.80	
			T _A = +70°C					0.48	1.20	
			T _A = +85°C					0.74	2.20	

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator clock is stopped.
 4. When high-speed system clock is stopped.
 5. Not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.
 HS(High speed main) mode: $V_{DD} = 2.7\text{ V}$ to 5.5 V @ 1 MHz to 24 MHz
 $V_{DD} = 2.4\text{ V}$ to 5.5 V @ 1 MHz to 16 MHz
 LS(Low speed main) mode: $V_{DD} = 1.8\text{ V}$ to 5.5 V @ 1 MHz to 8 MHz

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : high-speed on-chip oscillator clock frequency
 3. Except temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$, other than STOP mode

(2) 30-pin products

 $(T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	I _{DD2} ^{Note 2}	HALT mode	HS (High-speed main) mode ^{Note 6}	f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		440	1280	μA	
					V _{DD} = 3.0 V		440	1280		
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		400	1000	μA	
					V _{DD} = 3.0 V		400	1000		
				LS (Low-speed main) mode ^{Note 6}	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V		260	530	μA
						V _{DD} = 2.0 V		260	530	
			HS (High-speed main) mode ^{Note 6}	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		280	1000	μA	
					Resonator connection		450	1170		
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		280	1000	μA	
					Resonator connection		450	1170		
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		190	600	μA	
					Resonator connection		260	670		
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		190	600	μA	
					Resonator connection		260	670		
			LS (Low-speed main) mode ^{Note 6}	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380		
				f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input		95	330	μA	
					Resonator connection		145	380		
	I _{DD3} ^{Note 5}	STOP mode	T _A = −40°C					0.18	0.50	μA
			T _A = +25°C					0.23	0.50	
			T _A = +50°C					0.30	1.10	
			T _A = +70°C					0.46	1.90	
			T _A = +85°C					0.75	3.30	

Notes 1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator clock is stopped.

4. When high-speed system clock is stopped.

5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD} = 2.7\text{ V}$ to 5.5 V @ 1 MHz to 24 MHz

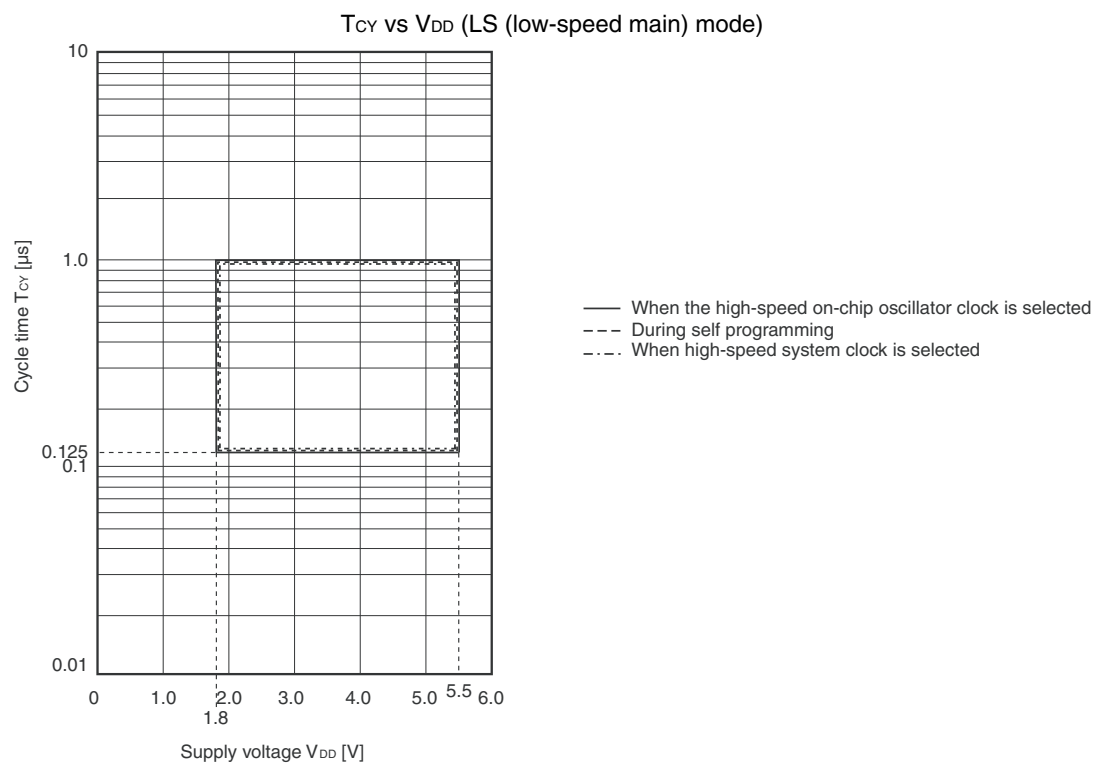
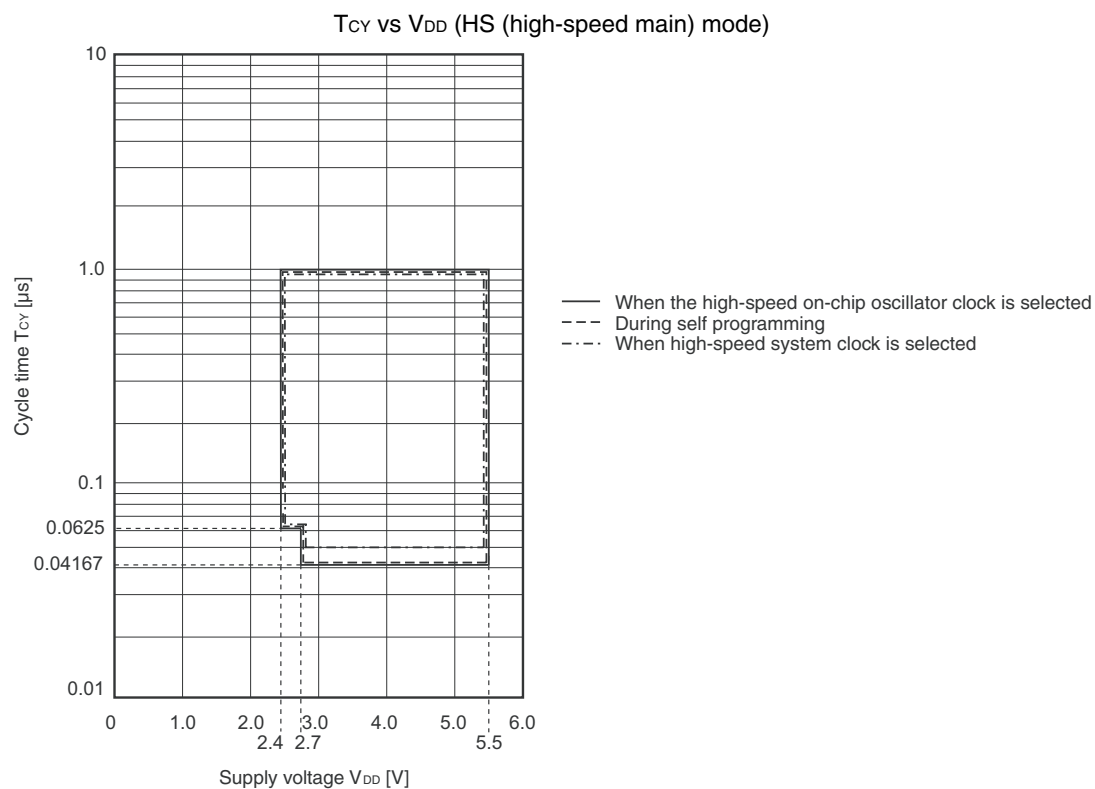
$V_{DD} = 2.4\text{ V}$ to 5.5 V @ 1 MHz to 16 MHz

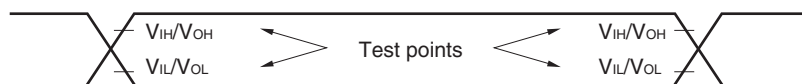
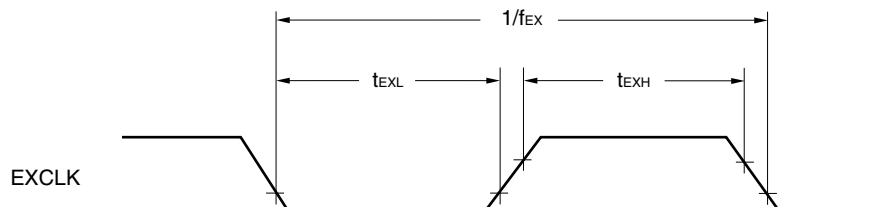
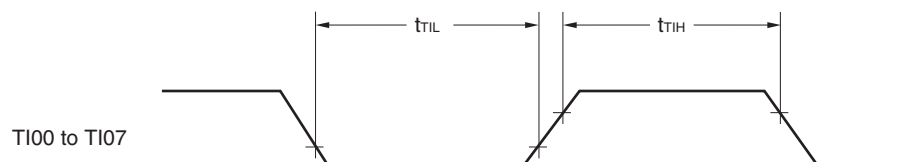
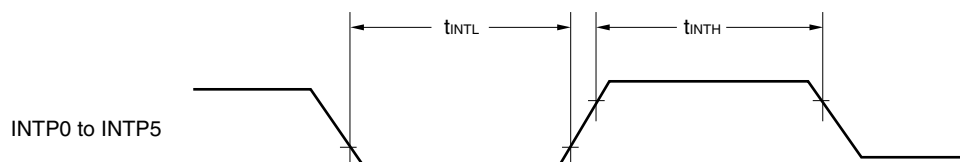
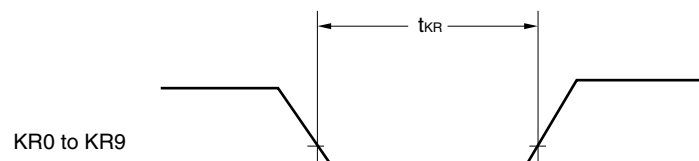
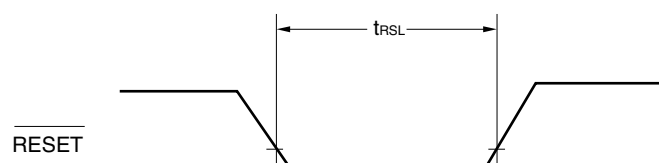
LS (Low speed main) mode: $V_{DD} = 1.8\text{ V}$ to 5.5 V @ 1 MHz to 8 MHz

Remarks 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH} : high-speed on-chip oscillator clock frequency

3. Except STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$.

Minimum Instruction Execution Time during Main System Clock Operation

AC Timing Test Point**External Main System Clock Timing****TI/TO Timing****Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

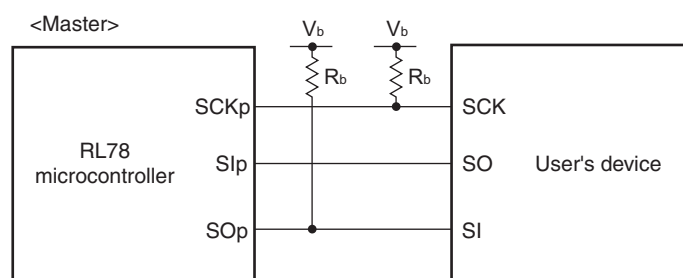
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	44		110		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	44		110		ns
		$1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note 2} , $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	110		110		ns
Slp hold time (from SCKp↓) ^{Note 1}	t_{KSI1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	19		19		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	19		19		ns
		$1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note 2} , $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	19		19		ns
Delay time from SCKp↑ to SOp output ^{Note 1}	t_{KSO1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		25		25	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		25		25	ns
		$1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note 2} , $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.2. Use it with $V_{DD} \geq V_b$.**Cautions** 1. Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

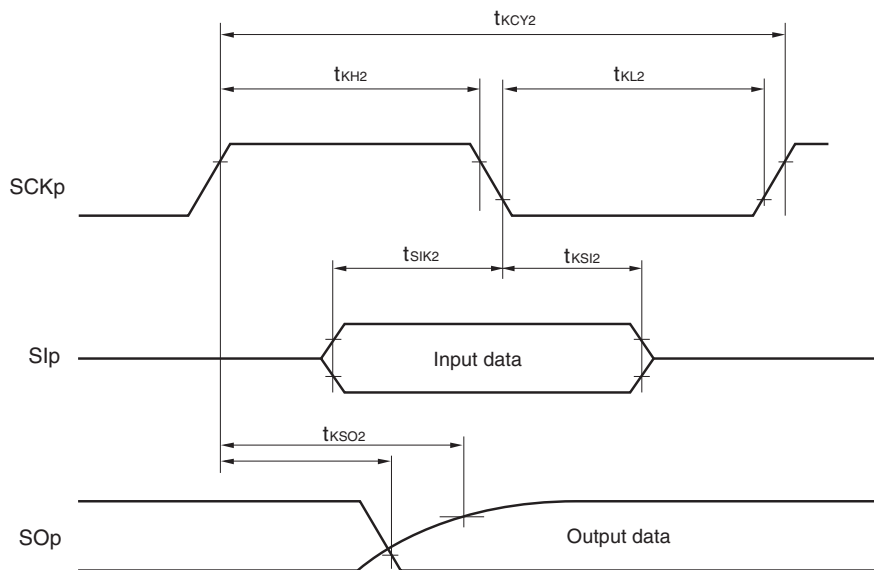
2. CSI01 and CSI11 cannot communicate at different potential.

Remarks 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

CSI mode connection diagram (during communication at different potential)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

2.5.2 Serial interface IICA

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode LS (low-speed main) mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz			0	400	kHz
		Normal mode: f _{CLK} ≥ 1 MHz	0	100			kHz
Setup time of restart condition	t _{SU:STA}		4.7		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}		4.0		0.6		μs
Hold time when SCLA0 = “L”	t _{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t _{HIGH}		4.0		0.6		μs
Data setup time (reception)	t _{SU:DAT}		250		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		0	3.45	0	0.9	μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		μs
Bus-free time	t _{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

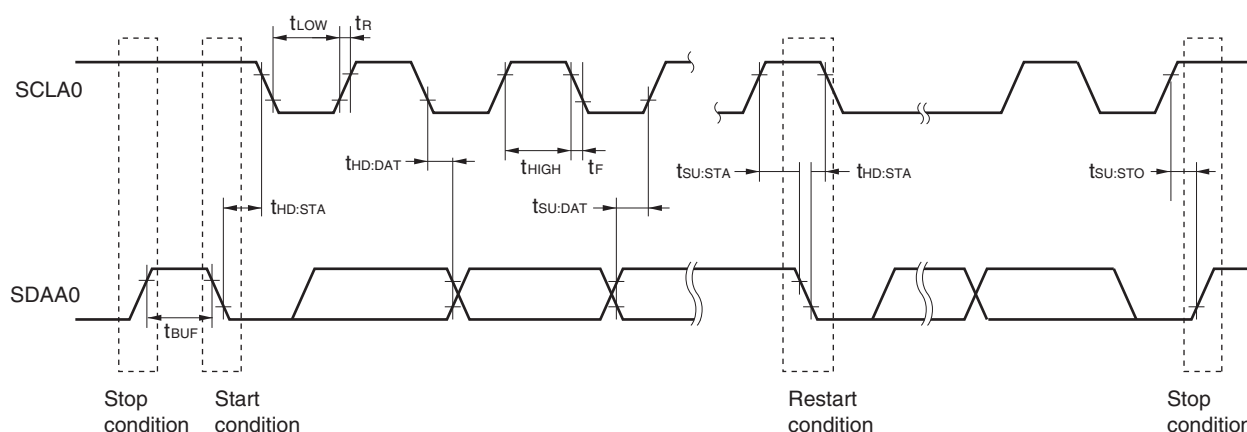
Caution Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-) = AV_{REFM}
ANI0 to ANI3	Refer to 28.6.1 (1) .	Refer to 28.6.1 (3) .	Refer to 28.6.1 (4) .
ANI16 to ANI22	Refer to 28.6.1 (2) .		
Internal reference voltage Temperature sensor output voltage	Refer to 28.6.1 (1) .		—

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}			1.2	± 3.5	LSB
					1.2	± 7.0 ^{Note 4}	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2, ANI3	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
				57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 0.25	%FSR
						± 0.50 ^{Note 4}	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 0.25	%FSR
						± 0.50 ^{Note 4}	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 2.5	LSB
						± 5.0 ^{Note 4}	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}				± 1.5	LSB
						± 2.0 ^{Note 4}	LSB
Analog input voltage	V_{AIN}	ANI2, ANI3		0		AV_{REFP}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} ^{Note 5}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TMPS25} ^{Note 5}			V

(Notes are listed on the next page.)

2.9 Dedicated Flash Memory Programmer Communication (UART)

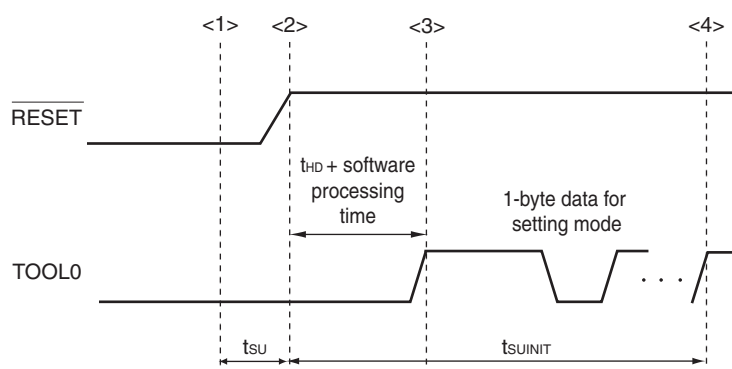
($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUNIT}	POR and LVD reset are released before external reset release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset are released before external reset release	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset are released before external reset release	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUNIT} : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**(3/4)**

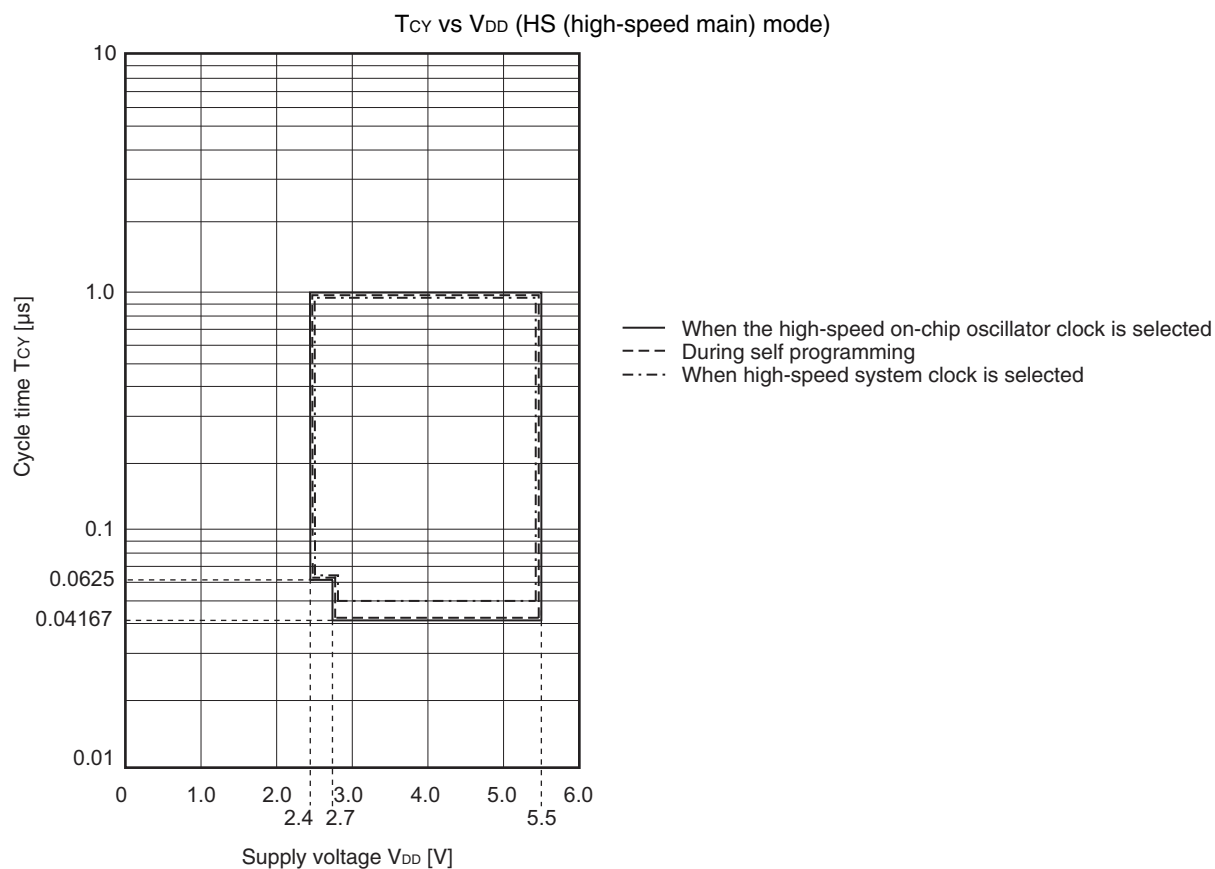
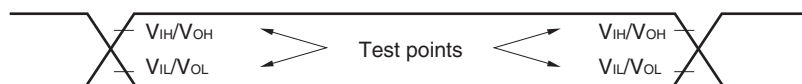
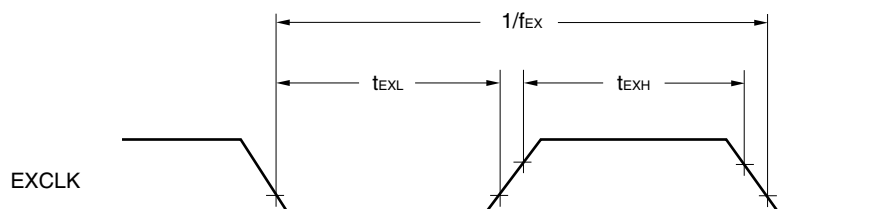
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Normal input buffer 20-, 24-pin products: P00 to P03 ^{Note 2} , P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	$0.8V_{DD}$		V_{DD}	V
	V_{IH2}	TTL input buffer 20-, 24-pin products: P10, P11 30-pin products: P01, P10, P11, P13 to P17	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.2	V_{DD}	V
			$3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	2.0	V_{DD}	V
			$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$	1.5	V_{DD}	V
	V_{IH3}	Normal input buffer P20 to P23	$0.7V_{DD}$		V_{DD}	V
	V_{IH4}	P60, P61	$0.7V_{DD}$		6.0	V
	V_{IH5}	P121, P122, P125 ^{Note 1} , P137, EXCLK, RESET	$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL1}	Normal input buffer 20-, 24-pin products: P00 to P03 ^{Note 2} , P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	0		$0.2V_{DD}$	V
	V_{IL2}	TTL input buffer 20-, 24-pin products: P10, P11 30-pin products: P01, P10, P11, P13 to P17	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0	0.8	V
			$3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	0	0.5	V
			$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$	0	0.32	V
	V_{IL3}	P20 to P23	0		$0.3V_{DD}$	V
	V_{IL4}	P60, P61	0		$0.3V_{DD}$	V
	V_{IL5}	P121, P122, P125 ^{Note 1} , P137, EXCLK, RESET	0		$0.2V_{DD}$	V
Output voltage, high	V_{OH1}	20-, 24-pin products: P00 to P03 ^{Note 2} , P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$	$V_{DD}-0.7$		V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -2.0\text{ mA}$	$V_{DD}-0.6$		V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -1.5\text{ mA}$	$V_{DD}-0.5$		V
	V_{OH2}	P20 to P23	$I_{OH2} = -100\text{ }\mu\text{A}$	$V_{DD}-0.5$		V

Notes 1. 20, 24-pin products only.

2. 24-pin products only.

Caution The maximum value of V_{IH} of pins P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products is V_{DD} even in N-ch open-drain mode. High level is not output in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

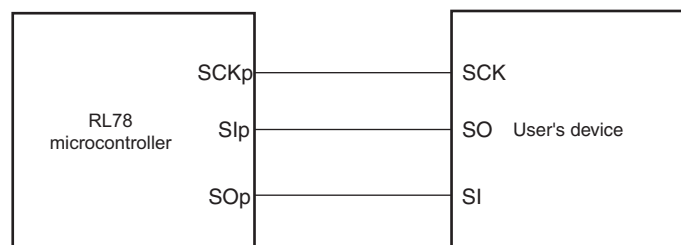
Minimum Instruction Execution Time during Main System Clock Operation**AC Timing Test Point****External Main System Clock Timing**

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 4}	t_{KCY2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$20\text{ MHz} < f_{MCK}$	$16/f_{MCK}$		ns
			$f_{MCK} \leq 20\text{ MHz}$	$12/f_{MCK}$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$16\text{ MHz} < f_{MCK}$	$16/f_{MCK}$		ns
			$f_{MCK} \leq 16\text{ MHz}$	$12/f_{MCK}$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$12/f_{MCK}$ and 1000		ns
SCKp high-/low-level width	t_{KH2} , t_{KL2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-14$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-16$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2-36$		ns
Slp setup time (to SCKp \uparrow) ^{Note 1}	t_{SIK2}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 40$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 60$		ns
Slp hold time (from SCKp \uparrow) ^{Note 2}	t_{KSI2}			$1/f_{MCK} + 62$		ns
Delay time from SCKp \downarrow to SOp output ^{Note 3}	t_{KSO2}	$C = 30\text{ pF}$ ^{Note 4}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$2/f_{MCK} + 66$	ns
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$2/f_{MCK} + 113$	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp \uparrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the Slp and SCKp pins and the normal output mode for the SOp pin by selecting port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

CSI mode connection diagram (during communication at same potential)

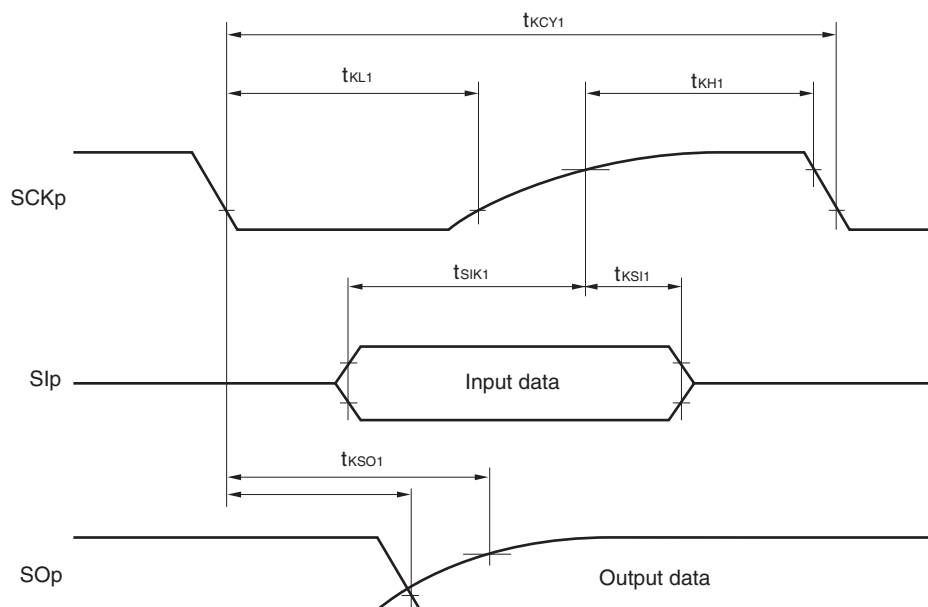
(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate <small>Note 4</small>		Reception	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		f _{MCK} /12 <small>Note 1</small>	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} <small>Note 2</small>		2.0	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		f _{MCK} /12 <small>Note 1</small>	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} <small>Note 2</small>		2.0	Mbps
		Transmission	2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		f _{MCK} /12 <small>Note 1</small>	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} <small>Note 2</small>		2.0	Mbps
			4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		Note 3	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V		2.0 <small>Note 4</small>	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		Note 5	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V		1.2 <small>Note 6</small>	Mbps
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		Notes 2, 7	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V		0.43 <small>Note 8</small>	Mbps

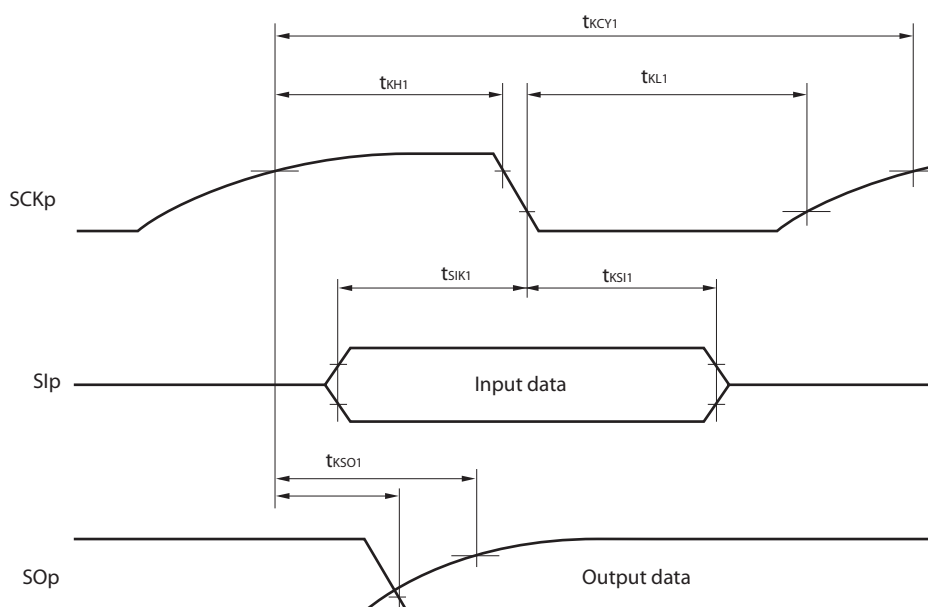
Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.**2.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)**3.** The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \quad [\text{bps}]$$

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 1}	t_{KCY2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$	$24/f_{MCK}$		ns
			$8\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$20/f_{MCK}$		ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$16/f_{MCK}$		ns
			$f_{MCK} \leq 4\text{ MHz}$	$12/f_{MCK}$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$	$32/f_{MCK}$		ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$28/f_{MCK}$		ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$24/f_{MCK}$		ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$16/f_{MCK}$		ns
			$f_{MCK} \leq 4\text{ MHz}$	$12/f_{MCK}$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$	$72/f_{MCK}$		ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$64/f_{MCK}$		ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$52/f_{MCK}$		ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$32/f_{MCK}$		ns
			$f_{MCK} \leq 4\text{ MHz}$	$20/f_{MCK}$		ns
SCKp high-/low-level width	t_{KH2} , t_{KL2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$		$t_{KCY2}/2 - 24$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$		$t_{KCY2}/2 - 36$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$		$t_{KCY2}/2 - 100$		ns
Slp setup time (to SCKp \uparrow) ^{Note 2}	t_{SIK2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_{DD} \leq 4.0\text{ V}$		$1/f_{MCK} + 40$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$		$1/f_{MCK} + 40$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_{DD} \leq 2.0\text{ V}$		$1/f_{MCK} + 60$		ns
Slp hold time (from SCKp \uparrow) ^{Note 3}	t_{KSI2}			$1/f_{MCK} + 62$		ns
Delay time from SCKp \downarrow to SOp output ^{Note 4}	t_{KSO2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$			$2/f_{MCK} + 240$	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$			$2/f_{MCK} + 428$	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$			$2/f_{MCK} + 1146$	ns

Notes 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes "to SCKp \downarrow " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from SCKp \downarrow " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp \uparrow " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

- Cautions**
1. Select the TTL input buffer for the Slp and SCKp pins and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.**
 2. CSI01 and CSI11 cannot communicate at different potential.

3.6.2 Temperature sensor/internal reference voltage characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

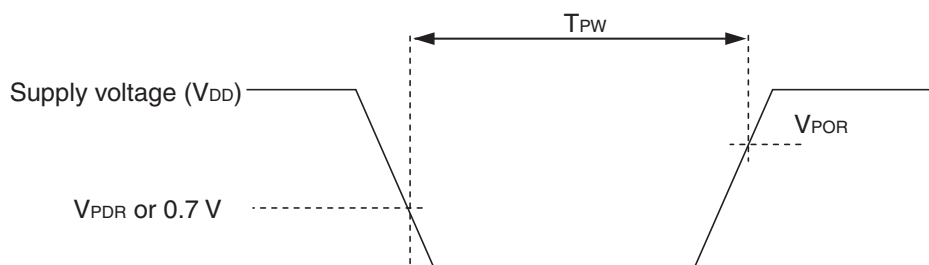
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F_{VTMS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/ $^\circ\text{C}$
Operation stabilization wait time	t_{AMP}		5			μs

3.6.3 POR circuit characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width ^{Note}	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode**($T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	V_{LVD0}	Power supply rise time	3.90	4.06	4.22	V
		Power supply fall time	3.83	3.98	4.13	V
	V_{LVD1}	Power supply rise time	3.60	3.75	3.90	V
		Power supply fall time	3.53	3.67	3.81	V
	V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
		Power supply fall time	2.94	3.06	3.18	V
	V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
		Power supply fall time	2.85	2.96	3.07	V
	V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
		Power supply fall time	2.75	2.86	2.97	V
	V_{LVD5}	Power supply rise time	2.70	2.81	2.92	V
		Power supply fall time	2.64	2.75	2.86	V
	V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
		Power supply fall time	2.55	2.65	2.75	V
	V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
		Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width	t_{LW}		300			μs
Detection delay time					300	μs