What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
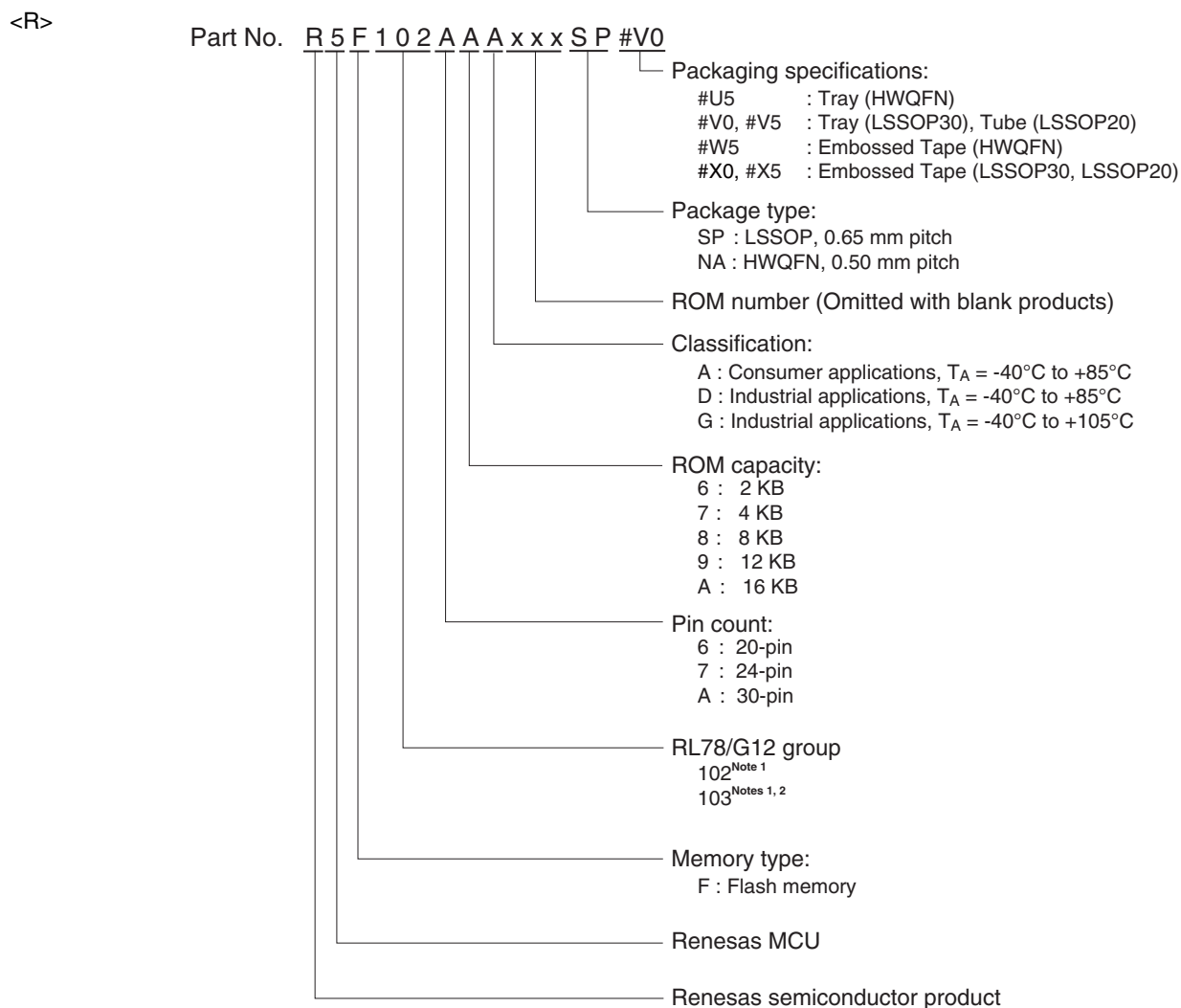
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f103a8asp-x0

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G12

<R>

Part No.   R 5 F 1 0 2 A A A x x x S P #V0

Packaging specifications:
  #U5   : Tray (HWQFN)
  #V0, #V5 : Tray (LSSOP30), Tube (LSSOP20)
  #W5   : Embossed Tape (HWQFN)
  #X0, #X5 : Embossed Tape (LSSOP30, LSSOP20)

Package type:
  SP : LSSOP, 0.65 mm pitch
  NA : HWQFN, 0.50 mm pitch

ROM number (Omitted with blank products)

Classification:
  A : Consumer applications, T_A = -40°C to +85°C
  D : Industrial applications, T_A = -40°C to +85°C
  G : Industrial applications, T_A = -40°C to +105°C

ROM capacity:
  6 : 2 KB
  7 : 4 KB
  8 : 8 KB
  9 : 12 KB
  A : 16 KB

Pin count:
  6 : 20-pin
  7 : 24-pin
  A : 30-pin

RL78/G12 group
  102[Note 1]
  103[Notes 1, 2]

Memory type:
  F : Flash memory

Renesas MCU

Renesas semiconductor product

Notes 1. For details about the differences between the R5F102 products and the R5F103 products of RL78/G12, see **1.1 Differences between the R5F102 Products and the R5F103 Products**.

   2. Products only for "A: Consumer applications (T_A = -40 to +85°C)" and "D: Industrial applications (T_A = -40 to +85°C)"

1.3.2 On-chip oscillator characteristics

(1) High-speed on-chip oscillator oscillation frequency of the R5F102 products

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = -20 to +85 °C	-1.0	+1.0	%
	T_A = -40 to -20 °C	-1.5	+1.5	
	T_A = +85 to +105 °C	-2.0	+2.0	

(2) High-speed on-chip oscillator oscillation frequency of the R5F103 products

Oscillator	Condition	MIN	MAX	Unit
High-speed on-chip oscillator oscillation frequency accuracy	T_A = -40 to + 85 °C	-5.0	+5.0	%

1.3.3 Peripheral Functions

The following are differences in peripheral functions between the R5F102 products and the R5F103 products.

RL78/G12		R5F102 product		R5F103 product	
		20, 24 pin product	30 pin product	20, 24 pin product	30 pin product
Serial interface	UART	1 channel	3 channels	1 channel	
	CSI	2 channels	3 channels	1 channel	
	Simplified I²C	2 channels	3 channels	None	
DMA function		2 channels		None	
Safety function	CRC operation	Yes		None	
	RAM guard	Yes		None	
	SFR guard	Yes		None	

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1.4 Pin Configuration (Top View)

1.4.1 20-pin products

- 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)
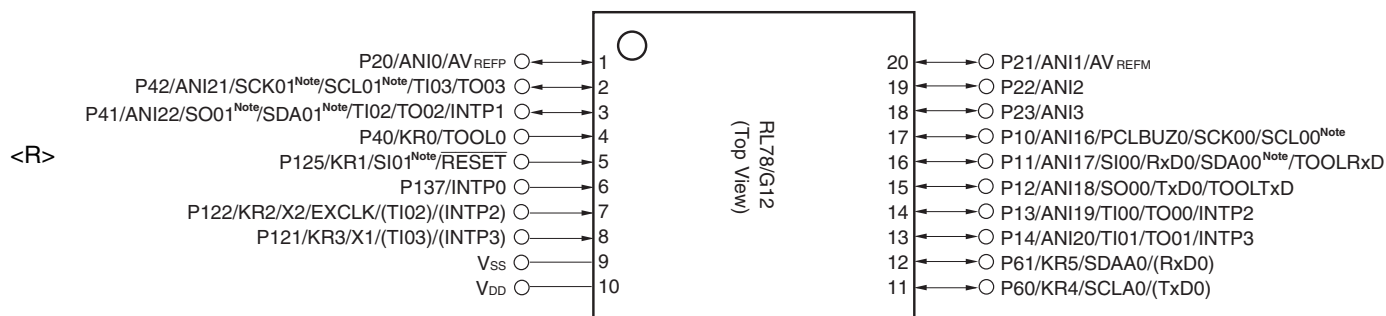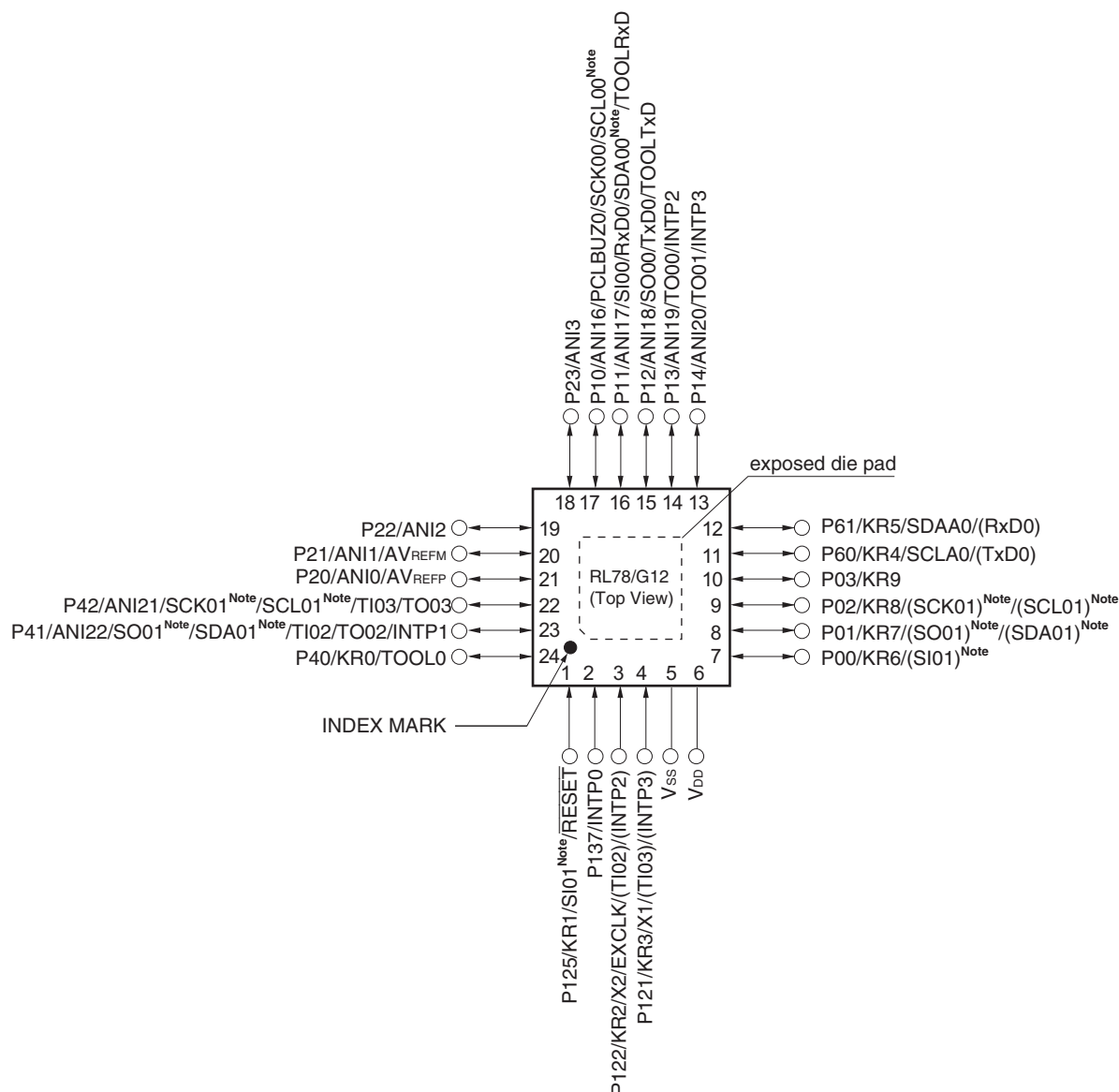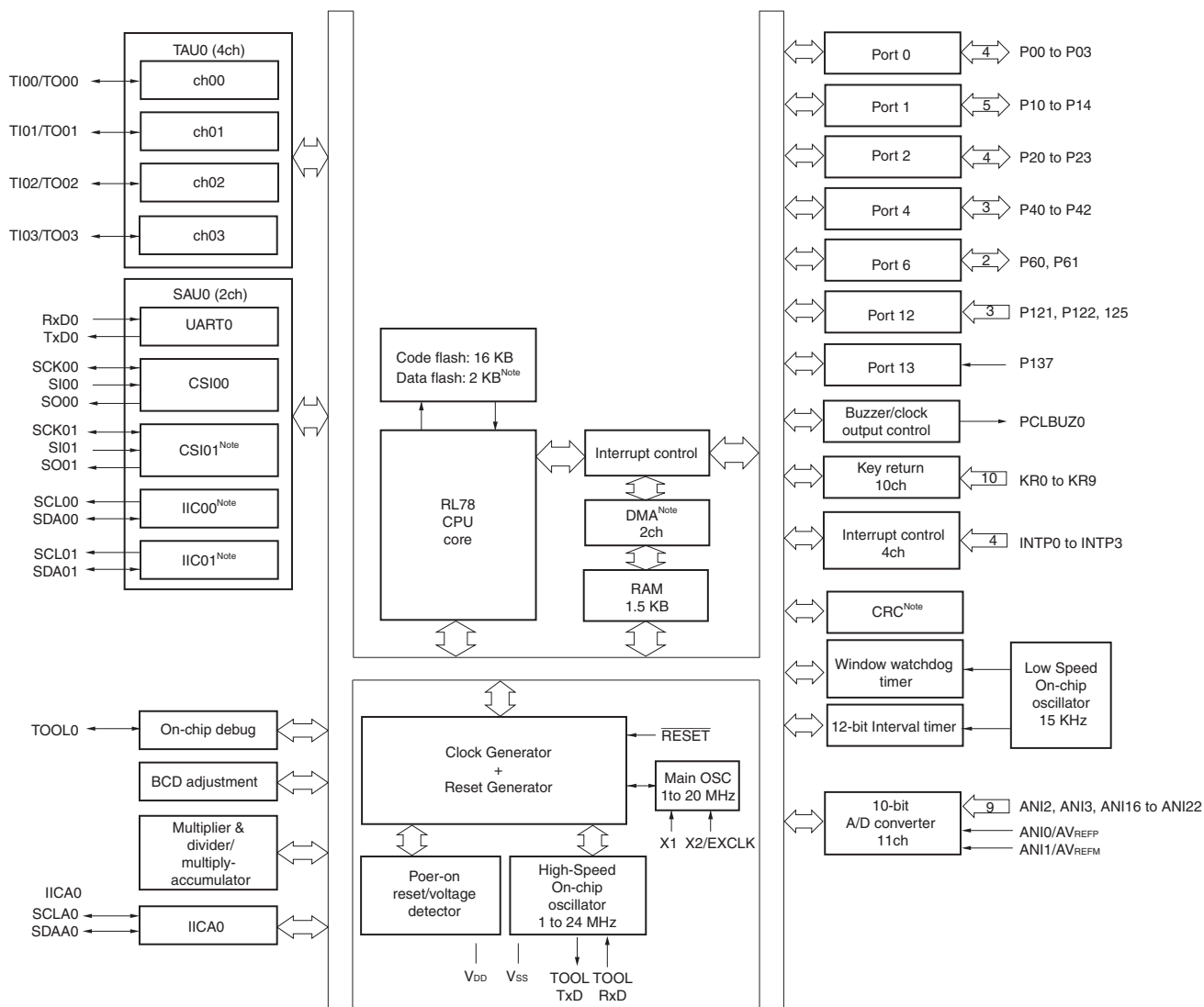
<R>

Note   Provided only in the R5F102 products.

Remarks 1. For pin identification, see **1.5 Pin Identification**.

   2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

1.4.2 24-pin products

<R>   •   24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)

Note   Provided only in the R5F102 products.

Remarks 1. For pin identification, see **1.5 Pin Identification**.

     2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

     3. It is recommended to connect an exposed die pad to Vss.

1.6.2 24-pin products

TAU0 (4ch)
- ch00 — TI00/TO00
- ch01 — TI01/TO01
- ch02 — TI02/TO02
- ch03 — TI03/TO03

SAU0 (2ch)
- UART0 — RxD0, TxD0
- CSI00 — SCK00, SI00, SO00
- CSI01[Note] — SCK01, SI01, SO01
- IIC00[Note] — SCL00, SDA00
- IIC01[Note] — SCL01, SDA01

TOOL0 — On-chip debug
BCD adjustment
Multiplier & divider/ multiply-accumulator
IICA0 — SCLA0, SDAA0, IICA0

Code flash: 16 KB
Data flash: 2 KB[Note]

RL78 CPU core

Interrupt control

DMA[Note] 2ch

RAM 1.5 KB

Clock Generator + Reset Generator — RESET

Main OSC 1to 20 MHz — X1 X2/EXCLK

Poer-on reset/voltage detector — V_DD V_SS

High-Speed On-chip oscillator 1 to 24 MHz — TOOL TxD TOOL RxD

Port 0 — 4 — P00 to P03
Port 1 — 5 — P10 to P14
Port 2 — 4 — P20 to P23
Port 4 — 3 — P40 to P42
Port 6 — 2 — P60, P61
Port 12 — 3 — P121, P122, 125
Port 13 — P137
Buzzer/clock output control — PCLBUZ0
Key return 10ch — 10 — KR0 to KR9
Interrupt control 4ch — 4 — INTP0 to INTP3
CRC[Note]
Window watchdog timer
12-bit Interval timer
Low Speed On-chip oscillator 15 KHz

10-bit A/D converter 11ch — 9 — ANI2, ANI3, ANI16 to ANI22, ANI0/AV_REFP, ANI1/AV_REFM

Note   Provided only in the R5F102 products.

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)   **(3/4)**

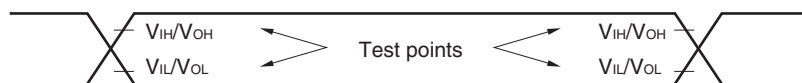| Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	Normal input buffer 20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147		0.8V$_{DD}$		V$_{DD}$	V
	V$_{IH2}$	TTL input buffer	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	2.2		V$_{DD}$	V
		20-, 24-pin products: P10, P11	3.3 V ≤ V$_{DD}$ < 4.0 V	2.0		V$_{DD}$	V
		30-pin products: P01, P10, P11, P13 to P17	1.8 V ≤ V$_{DD}$ < 3.3 V	1.5		V$_{DD}$	V
	V$_{IH3}$	P20 to P23		0.7V$_{DD}$		V$_{DD}$	V
	V$_{IH4}$	P60, P61		0.7V$_{DD}$		6.0	V
	V$_{IH5}$	P121, P122, P125[Note 1], P137, EXCLK, $\overline{RESET}$		0.8V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	Normal input buffer 20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147		0		0.2V$_{DD}$	V
	V$_{IL2}$	TTL input buffer	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	0		0.8	V
		20-, 24-pin products: P10, P11	3.3 V ≤ V$_{DD}$ < 4.0 V	0		0.5	V
		30-pin products: P01, P10, P11, P13 to P17	1.8 V ≤ V$_{DD}$ < 3.3 V	0		0.32	V
	V$_{IL3}$	P20 to P23		0		0.3V$_{DD}$	V
	V$_{IL4}$	P60, P61		0		0.3V$_{DD}$	V
	V$_{IL5}$	P121, P122, P125[Note 1], P137, EXCLK, $\overline{RESET}$		0		0.2V$_{DD}$	V
Output voltage, high	V$_{OH1}$	20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH1}$ = −10.0 mA	V$_{DD}$−1.5			V
			4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH1}$ = −3.0 mA	V$_{DD}$−0.7			V
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH1}$ = −2.0 mA	V$_{DD}$−0.6			V
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH1}$ = −1.5 mA	V$_{DD}$−0.5			V
	V$_{OH2}$	P20 to P23	I$_{OH2}$ = −100 μA	V$_{DD}$−0.5			V

Notes 1. 20, 24-pin products only.

2. 24-pin products only.

Caution The maximum value of V$_{IH}$ of pins P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products is V$_{DD}$ even in N-ch open-drain mode. High level is not output in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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2.5 Peripheral Functions Characteristics

AC Timing Test Point

2.5.1 Serial array unit

(1) During communication at same potential (UART mode)
(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1				f$_{MCK}$/6		f$_{MCK}$/6	bps
		Theoretical value of the maximum transfer rate f$_{CLK}$ = f$_{MCK}$Note2		4.0		1.3	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f$_{CLK}$) are:
 HS (high-speed main) mode: 24 MHz (2.7 V ≤ V$_{DD}$ ≤ 5.5 V)
 16 MHz (2.4 V ≤ V$_{DD}$ ≤ 5.5 V)
 LS (low-speed main) mode: 8 MHz (1.8 V ≤ V$_{DD}$ ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)
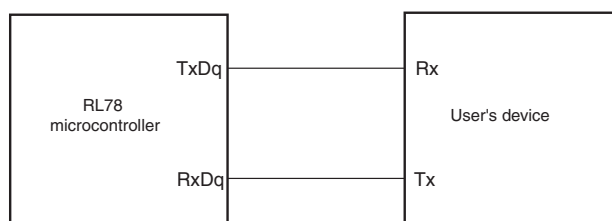
UART mode bit width (during communication at same potential) (reference)
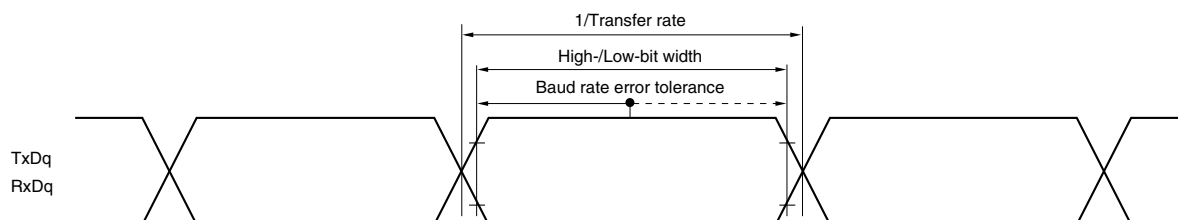
Remarks 1. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

2. f$_{MCK}$: Serial array unit operation clock frequency
 (Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(2) During communication at same potential (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)

(T$_A$ = −40 to +85°C, 2.7 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCK00 cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 2/f$_{CLK}$	83.3		250		ns
SCK00 high-/low-level width	t$_{KH1}$, t$_{KL1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	t$_{KCY1}$/2–7		t$_{KCY1}$/2–50		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V	t$_{KCY1}$/2–10		t$_{KCY1}$/2–50		ns
SI00 setup time (to SCK00↑) [Note 1]	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	23		110		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V	33		110		ns
SI00 hold time (from SCK00↑) [Note2]	t$_{KSI1}$		10		10		ns
Delay time from SCK00↓ to SO00 output [Note 3]	t$_{KSO1}$	C = 20 pF [Note 4]		10		10	ns

Notes 1. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 setup time becomes "to SCK00↓" when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

2. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 hold time becomes "from SCK00↓" when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

3. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The delay time to SO00 output becomes "from SCK00↑" when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

4. C is the load capacitance of the SCK00 and SO00 output lines.

Caution Select the normal input buffer for the SI00 pin and the normal output mode for the SO00 and SCK00 pins by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).

Remarks 1. This specification is valid only when CSI00's peripheral I/O redirect function is not used.

2. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS00 bit of serial mode register 00 (SMR00).)

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(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
					MIN.	MAX.	MIN.	MAX.	
Transfer rate [Note4]		Reception	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V			f$_{MCK}$/6 [Note1]		f$_{MCK}$/6 [Note1]	bps
				Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note3]		4.0		1.3	Mbps
			2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V			f$_{MCK}$/6 [Note1]		f$_{MCK}$/6 [Note1]	bps
				Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note3]		4.0		1.3	Mbps
			1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V			f$_{MCK}$/6 [Notes1, 2]		f$_{MCK}$/6 [Notes1, 2]	bps
				Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$ [Note3]		4.0		1.3	Mbps
		Transmission	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V			**Note4**		**Note4**	bps
				Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 1.4 kΩ, V$_b$ = 2.7 V		2.8 [Note5]		2.8 [Note5]	Mbps
			2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V,			**Note6**		**Note6**	bps
				Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 2.7 kΩ, V$_b$ = 2.3 V		1.2 [Note7]		1.2 [Note7]	Mbps
			1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V			**Notes 2, 8**		**Notes 2, 8**	bps
				Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 5.5 kΩ, V$_b$ = 1.6 V		0.43 [Note9]		0.43 [Note9]	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

     2. Use it with V$_{DD}$ ≥ V$_b$.

     3. The maximum operating frequencies of the CPU/peripheral hardware clock (f$_{CLK}$) are:

        HS (high-speed main) mode: 24 MHz (2.7 V ≤ V$_{DD}$ ≤ 5.5 V)

                                 16 MHz (2.4 V ≤ V$_{DD}$ ≤ 5.5 V)

        LS (low-speed main) mode: 8 MHz (1.8 V ≤ V$_{DD}$ ≤ 5.5 V)

     4. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

        Expression for calculating the transfer rate when 4.0 V ≤ V$_{DD}$ ≤ 5.5 V and 2.7 V ≤ V$_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

       * This value is the theoretical value of the relative difference between the transmission and reception sides.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)

(T$_A$ = −40 to +85°C, 2.7 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCK00 cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 2/f$_{CLK}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ	200		1150		ns
			2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ	300		1150		ns
SCK00 high-level width	t$_{KH1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2− 50		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 120		t$_{KCY1}$/2 − 120		ns
SCK00 low-level width	t$_{KL1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		t$_{KCY1}$/2 − 7		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 10		t$_{KCY1}$/2 − 50		ns
SI00 setup time (to SCK00↑) [Note 1]	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		58		479		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		121		479		ns
SI00 hold time (from SCK00↑) [Note 1]	t$_{KSI1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		10		10		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		10		10		ns
Delay time from SCK00↓ to SO00 output [Note 1]	t$_{KSO1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ			60		60	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ			130		130	ns
SI00 setup time (to SCK00↓) [Note 2]	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		23		110		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		33		110		ns
SI00 hold time (from SCK00↓) [Note 2]	t$_{KSI1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		10		10		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		10		10		ns
Delay time from SCK00↑ to SO00 output [Note 2]	t$_{KSO1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ			10		10	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ			10		10	ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

Notes 1. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1

    2. When DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

Caution Select the TTL input buffer for the SI00 pin and the N-ch open drain output (V_{DD} tolerance) mode for the SO00 pin and SCK00 pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remarks 1. R_b [Ω]:Communication line (SCK00, SO00) pull-up resistance, C_b [F]: Communication line (SCK00, SO00) load capacitance, V_b [V]: Communication line voltage

    2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS00 bit of serial mode register 00 (SMR00).)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	81		479		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	177		479		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	479		479		ns
SIp hold time (from SCKp↑) [Note 1]	t$_{KSI1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	19		19		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	19		19		ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	19		19		ns
Delay time from SCKp↓ to SOp output [Note 1]	t$_{KSO1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		100		100	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		195		195	ns
		1.8 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		483		483	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

    2. Use it with V$_{DD}$ ≥ V$_b$.

(**Cautions** and **Remarks** are listed on the next page.)

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV$_{REFP}$ Reference voltage (−) = AV$_{REFM}$	Reference voltage (+) = V$_{DD}$ Reference voltage (−) = V$_{SS}$	Reference voltage (+) = V$_{BGR}$ Reference voltage (−) = AV$_{REFM}$
ANI0 to ANI3	Refer to **28.6.1 (1)**.	Refer to **28.6.1 (3)**.	Refer to **28.6.1 (4)**.
ANI16 to ANI22	Refer to **28.6.1 (2)**.		
Internal reference voltage	Refer to **28.6.1 (1)**.		−
Temperature sensor output voltage			

(1) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage

(T$_A$ = −40 to +85°C, 1.8 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (−) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]			1.2	±3.5	LSB
					1.2	±7.0 [Note 4]	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI2, ANI3	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
				57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]				±0.25	%FSR
						±0.50 [Note 4]	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]				±0.25	%FSR
						±0.50 [Note 4]	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]				±2.5	LSB
						±5.0 [Note 4]	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]				±1.5	LSB
						±2.0 [Note 4]	LSB
Analog input voltage	V$_{AIN}$	ANI2, ANI3		0		AV$_{REFP}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{BGR}$ [Note 5]		V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{TMPS25}$ [Note 5]		V

(**Notes** are listed on the next page.)

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)   **(4/4)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V$_{OL1}$	20-, 24-pin products: P00 to P03^{Note}, P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 8.5 mA			0.7	V
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 3.0 mA			0.6	V
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 1.5 mA			0.4	V
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 0.6 mA			0.4	V
	V$_{OL2}$	P20 to P23	I$_{OL2}$ = 400 μA			0.4	V
	V$_{OL3}$	P60, P61	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 15.0 mA			2.0	V
			4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 5.0 mA			0.4	V
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 3.0 mA			0.4	V
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL1}$ = 2.0 mA			0.4	V
Input leakage current, high	I$_{LIH1}$	Other than P121, P122	V$_I$ = V$_{DD}$			1	μA
	I$_{LIH2}$	P121, P122 (X1, X2/EXCLK)	V$_I$ = V$_{DD}$	Input port or external clock input			1	μA
				When resonator connected			10	μA
Input leakage current, low	I$_{LIL1}$	Other than P121, P122	V$_I$ = V$_{SS}$			−1	μA
	I$_{LIL2}$	P121, P122 (X1, X2/EXCLK)	V$_I$ = V$_{SS}$	Input port or external clock input			−1	μA
				When resonator connected			−10	μA
On-chip pull-up resistance	R$_U$	20-, 24-pin products: P00 to P03^{Note}, P10 to P14, P40 to P42, P125, $\overline{RESET}$ 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	V$_I$ = V$_{SS}$, input port	10	20	100	kΩ

Note   24-pin products only.

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
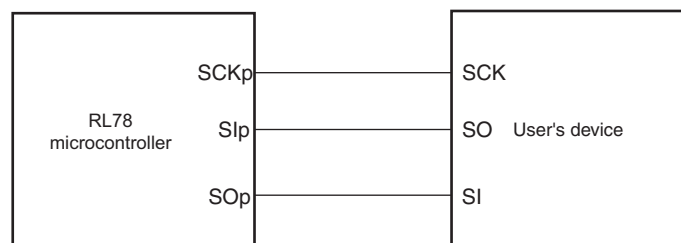
(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time [Note4]	t$_{KCY2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	20 MHz < f$_{MCK}$	16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 20 MHz	12/f$_{MCK}$		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V	16 MHz < f$_{MCK}$	16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 16 MHz	12/f$_{MCK}$		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		12/f$_{MCK}$ and 1000		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2−14		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2−16		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY2}$/2−36		ns
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK2}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$ + 40		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		1/f$_{MCK}$ + 60		ns
SIp hold time (from SCKp↑) [Note 2]	t$_{KSI2}$			1/f$_{MCK}$ + 62		ns
Delay time from SCKp↓ to SOp output [Note 3]	t$_{KSO2}$	C = 30 pF [Note4]	2.7 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{MCK}$ + 66	ns
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{MCK}$ + 113	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

CSI mode connection diagram (during communication at same potential)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)

(T_A = −40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) [Note]	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	162		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	354		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	958		ns
SIp hold time (from SCKp↑) [Note]	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output [Note]	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		200	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		390	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		966	ns

Note   When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

(**Cautions** and **Remarks** are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^{2}C mode)

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ		100[Note1]	kHz
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ		100[Note1]	kHz
		2.4 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ		100[Note1]	kHz
Hold time when SCLr = "L"	t$_{LOW}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	4600		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	4600		ns
		2.4 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t$_{HIGH}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	2700		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	2400		ns
		2.4 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1830		ns
Data setup time (reception)	t$_{SU:DAT}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	1/f$_{MCK}$ + 760 [Note3]		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 760 [Note3]		ns
		2.4 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1/f$_{MCK}$ + 570 [Note3]		ns
Data hold time (transmission)	t$_{HD:DAT}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	0	1420	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	0	1420	ns
		2.4 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	0	1215	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

      2. Set t$_{SU:DAT}$ so that it will not exceed the hold time when SCLr = "L" or SCLr = "H".

Cautions 1. Select the TTL input buffer and the N-ch open drain output (V$_{DD}$ tolerance) mode for the SDAr pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the SCLr pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

        2. IIC01 and IIC11 cannot communicate at different potential.

(**Remarks** are listed on the next page.)

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV$_{REFP}$ < V$_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

4. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22

(T$_A$ = –40 to +105°C, 2.4 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (–) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$			8		10	bit
Overall error [Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]			1.2	±5.0	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target ANI pin: ANI16 to ANI22	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error [Notes 1, 2]	EZS	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]				±0.35	%FSR
Full-scale error [Notes 1, 2]	EFS	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]				±0.35	%FSR
Integral linearity error [Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]				±3.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]				±2.0	LSB
Analog input voltage	V$_{AIN}$	ANI16 to ANI22		0		AV$_{REFP}$ and V$_{DD}$	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV$_{REFP}$ ≤ V$_{DD}$, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (−) = AVREFM (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22

(TA = −40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = VBGR$^{Note\,3}$, Reference voltage (−) = AVREFM $^{Note\,4}$= 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		bit
Conversion time	tCONV	8-bit resolution	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	8-bit resolution			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution			±1.0	LSB
Analog input voltage	VAIN		0		VBGR[Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).
    2. This value is indicated as a ratio (%FSR) to the full-scale value.
    3. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.
    4. When reference voltage (−) = VSS, the MAX. values are as follows.
        Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AVREFM.
        Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AVREFM.
   Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AVREFM.

4. PACKAGE DRAWINGS

4.1 20-pin products

R5F1026AASP, R5F10269ASP, R5F10268ASP, R5F10267ASP, R5F10266ASP
R5F1036AASP, R5F10369ASP, R5F10368ASP, R5F10367ASP, R5F10366ASP
R5F1026ADSP, R5F10269DSP, R5F10268DSP, R5F10267DSP, R5F10266DSP
R5F1036ADSP, R5F10369DSP, R5F10368DSP, R5F10367DSP, R5F10366DSP
<R>   R5F1026AGSP, R5F10269GSP, R5F10268GSP, R5F10267GSP, R5F10266GSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1

detail of lead end
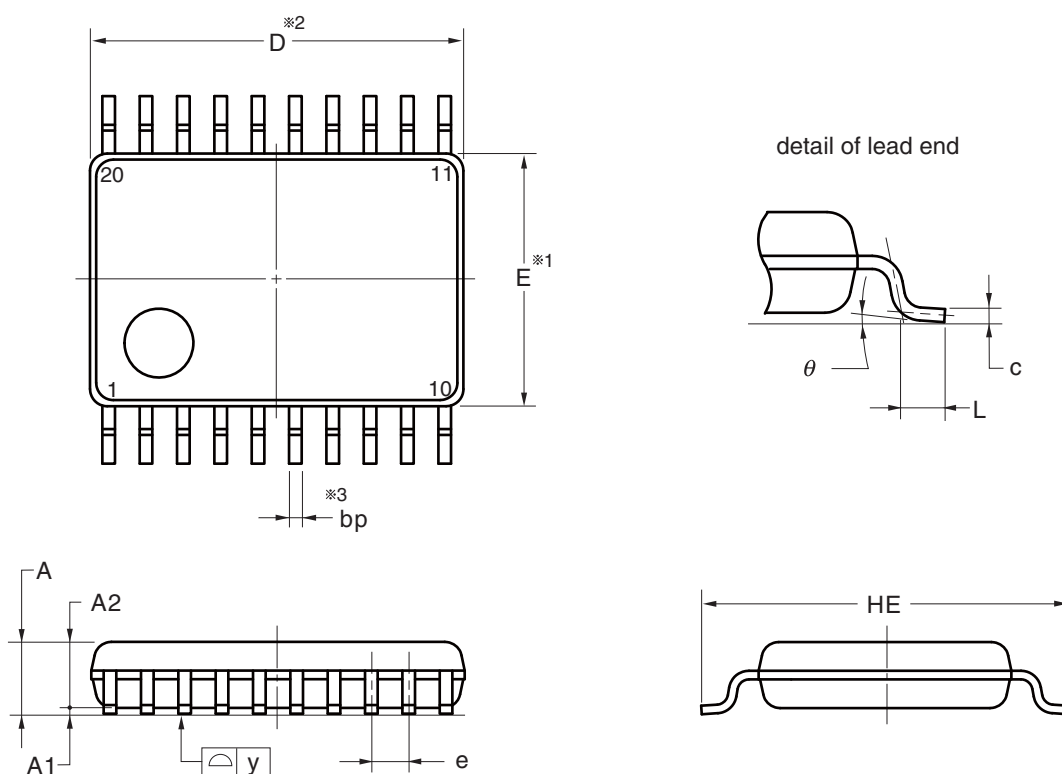
NOTE

1. Dimensions "※1" and "※2" do not include mold flash.

2. Dimension "※3" does not include trim offset.

(UNIT:mm)

ITEM	DIMENSIONS
D	6.50±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.45 MAX.
A1	0.10±0.10
A2	1.15
e	0.65±0.12
bp	$0.22 ^{+0.10} _{-0.05}$
c	$0.15 ^{+0.05} _{-0.02}$
L	0.50±0.20
y	0.10
θ	0° to 10°