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What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f103a8dsp-v0

Table 1-1. List of Ordering Part Numbers

	Pin count	Package	Data flash	Fields of Application	Part Number
<R>	20 pins	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)	Mounted	A	R5F1026AASP#V5, R5F10269ASP#V5, R5F10268ASP#V5, R5F10267ASP#V5, R5F10266ASP#V5 R5F1026AASP#X5, R5F10269ASP#X5, R5F10268ASP#X5, R5F10267ASP#X5, R5F10266ASP#X5
				D	R5F1026ADSP#V5, R5F10269DSP#V5, R5F10268DSP#V5, R5F10267DSP#V5, R5F10266DSP#V5 R5F1026ADSP#X5, R5F10269DSP#X5, R5F10268DSP#X5, R5F10267DSP#X5, R5F10266DSP#X5
				G	R5F1026AGSP#V5, R5F10269GSP#V5, R5F10268GSP#V5, R5F10267GSP#V5, R5F10266GSP#V5 R5F1026AGSP#X5, R5F10269GSP#X5, R5F10268GSP#X5, R5F10267GSP#X5, R5F10266GSP#X5
			Not mounted	A	R5F1036AASP#V5, R5F10369ASP#V5, R5F10368ASP#V5, R5F10367ASP#V5, R5F10366ASP#V5 R5F1036AASP#X5, R5F10369ASP#X5, R5F10368ASP#X5, R5F10367ASP#X5, R5F10366ASP#X5
				D	R5F1036ADSP#V5, R5F10369DSP#V5, R5F10368DSP#V5, R5F10367DSP#V5, R5F10366DSP#V5 R5F1036ADSP#X5, R5F10369DSP#X5, R5F10368DSP#X5, R5F10367DSP#X5, R5F10366DSP#X5
<R>	24 pins	24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)	Mounted	A	R5F1027AANA#U5, R5F10279ANA#U5, R5F10278ANA#U5, R5F10277ANA#U5 R5F1027AANA#W5, R5F10279ANA#W5, R5F10278ANA#W5, R5F10277ANA#W5
				D	R5F1027ADNA#U5, R5F10279DNA#U5, R5F10278DNA#U5, R5F10277DNA#U5 R5F1027ADNA#W5, R5F10279DNA#W5, R5F10278DNA#W5, R5F10277DNA#W5
				G	R5F1027AGNA#U5, R5F10279GNA#U5, R5F10278GNA#U5, R5F10277GNA#U5 R5F1027AGNA#W5, R5F10279GNA#W5, R5F10278GNA#W5, R5F10277GNA#W5
			Not mounted	A	R5F1037AANA#V5, R5F10379ANA#V5, R5F10378ANA#V5, R5F10377ANA#V5 R5F1037AANA#X5, R5F10379ANA#X5, R5F10378ANA#X5, R5F10377ANA#X5
				D	R5F1037ADNA#V5, R5F10379DNA#V5, R5F10378DNA#V5, R5F10377DNA#V5 R5F1037ADNA#X5, R5F10379DNA#X5, R5F10378DNA#X5, R5F10377DNA#X5
	30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A	R5F102AAASP#V0, R5F102A9ASP#V0, R5F102A8ASP#V0, R5F102A7ASP#V0 R5F102AAASP#X0, R5F102A9ASP#X0, R5F102A8ASP#X0, R5F102A7ASP#X0
				D	R5F102AADSP#V0, R5F102A9DSP#V0, R5F102A8DSP#V0, R5F102A7DSP#V0 R5F102AADSP#X0, R5F102A9DSP#X0, R5F102A8DSP#X0, R5F102A7DSP#X0
				G	R5F102AAGSP#V0, R5F102A9GSP#V0, R5F102A8GSP#V0, R5F102A7GSP#V0 R5F102AAGSP#X0, R5F102A9GSP#X0, R5F102A8GSP#X0, R5F102A7GSP#X0
			Not mounted	A	R5F103AAASP#V0, R5F103A9ASP#V0, R5F103A8ASP#V0, R5F103A7ASP#V0 R5F103AAASP#X0, R5F103A9ASP#X0, R5F103A8ASP#X0, R5F103A7ASP#X0
				D	R5F103AADSP#V0, R5F103A9DSP#V0, R5F103A8DSP#V0, R5F103A7DSP#V0 R5F103AADSP#X0, R5F103A9DSP#X0, R5F103A8DSP#X0, R5F103A7DSP#X0

Note　For fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G12**.

Caution　The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Differences between the R5F102 Products and the R5F103 Products

The following are differences between the R5F102 products and the R5F103 products.

○ Whether the data flash memory is mounted or not

○ High-speed on-chip oscillator oscillation frequency accuracy

○ Number of channels in serial interface

○ Whether the DMA function is mounted or not

○ Whether a part of the safety functions are mounted or not

1.3.1 Data Flash

The data flash memory of 2 KB is mounted on the R5F102 products, but not on the R5F103 products.

Product	Data Flash
R5F102 products R5F1026A, R5F1027A, R5F102AA, R5F10269, R5F10279, R5F102A9, R5F10268, R5F10278, R5F102A8, R5F10267, R5F10277, R5F102A7, R5F10266 ^{Note}	2KB
R5F103 products R5F1036A, R5F1037A, R5F103AA, R5F10369, R5F10379, R5F103A9, R5F10368, R5F10378 R5F103A8, R5F10367, R5F10377, R5F103A7, R5F10366	Not mounted

Note The RAM in the R5F10266 has capacity as small as 256 bytes. Depending on the customer's program specification, the stack area to execute the data flash library may not be kept and data may not be written to or erased from the data flash memory.

Caution When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.

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1.4.2 24-pin products

<R> • 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)
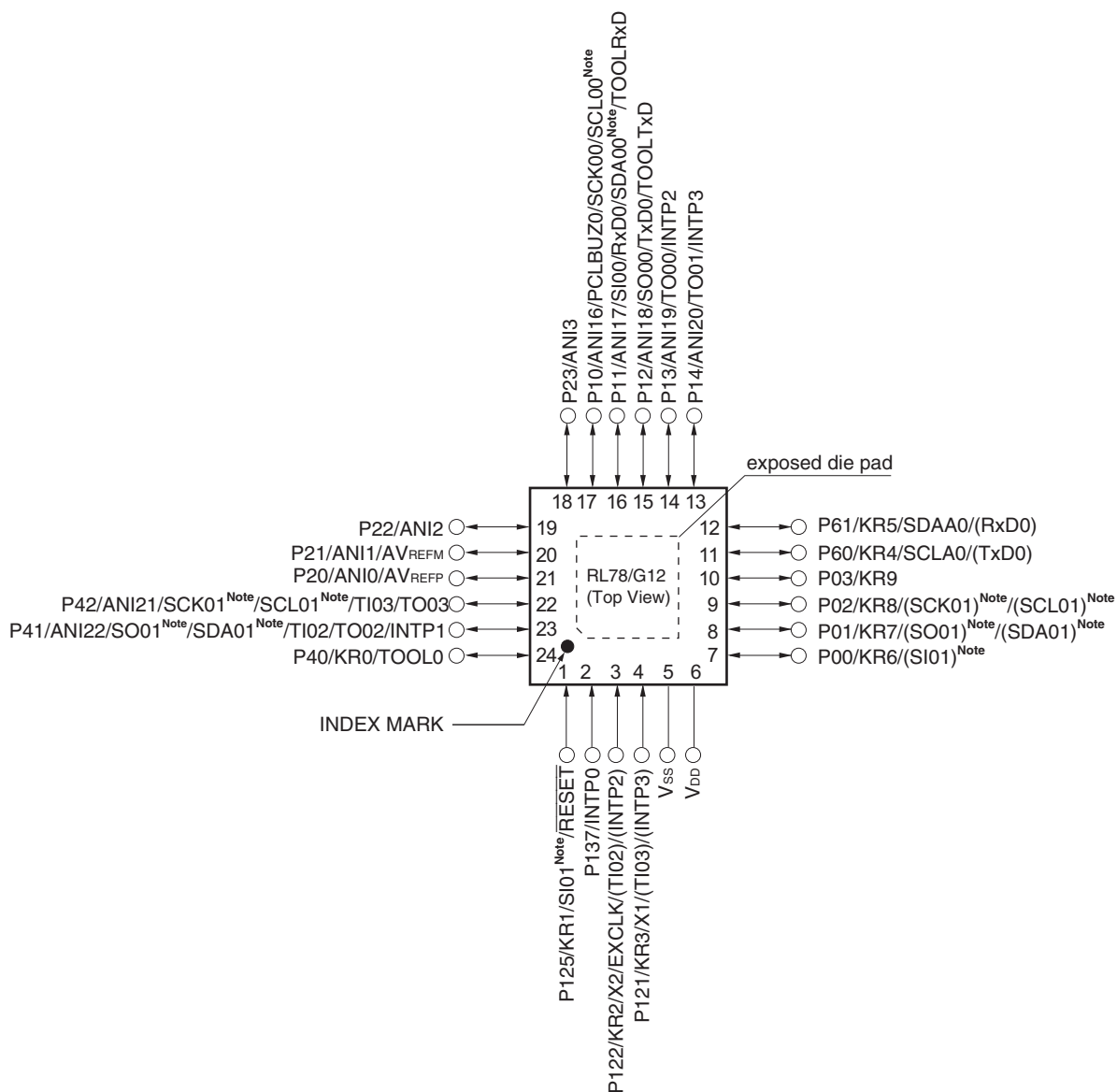
Note Provided only in the R5F102 products.

Remarks 1. For pin identification, see **1.5 Pin Identification**.

     2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)**.

     3. It is recommended to connect an exposed die pad to Vss.

(2) 30-pin products

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)   **(1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD1}$	Operating mode	HS (High-speed main) mode[Note 4]	f$_{IH}$ = 24 MHz[Note 3]	Basic operation	V$_{DD}$ = 5.0 V		1.5		mA
						V$_{DD}$ = 3.0 V		1.5		
					Normal operation	V$_{DD}$ = 5.0 V		3.7	5.5	mA
						V$_{DD}$ = 3.0 V		3.7	5.5	
				f$_{IH}$ = 16 MHz[Note 3]		V$_{DD}$ = 5.0 V		2.7	4.0	mA
						V$_{DD}$ = 3.0 V		2.7	4.0	
			LS (Low-speed main) mode[Note 4]	f$_{IH}$ = 8 MHz[Note 3]		V$_{DD}$ = 3.0 V		1.2	1.8	mA
						V$_{DD}$ = 2.0 V		1.2	1.8	
			HS (High-speed main) mode[Note 4]	f$_{MX}$ = 20 MHz[Note 2], V$_{DD}$ = 5.0 V		Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f$_{MX}$ = 20 MHz[Note 2], V$_{DD}$ = 3.0 V		Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f$_{MX}$ = 10 MHz[Note 2], V$_{DD}$ = 5.0 V		Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
				f$_{MX}$ = 10 MHz[Note 2], V$_{DD}$ = 3.0 V		Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
			LS (Low-speed main) mode[Note 4]	f$_{MX}$ = 8 MHz[Note 2], V$_{DD}$ = 3.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f$_{MX}$ = 8 MHz[Note 2], V$_{DD}$ = 2.0 V		Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	

Notes 1. Total current flowing into V$_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$ or V$_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.

3. When high-speed system clock is stopped

4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: V$_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz

V$_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS(Low speed main) mode: V$_{DD}$ = 1.8 V to 5.5 V @1 MHz to 8 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: high-speed on-chip oscillator clock frequency

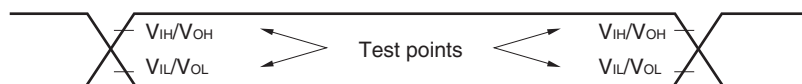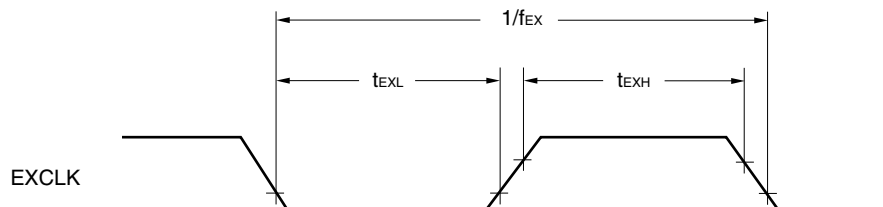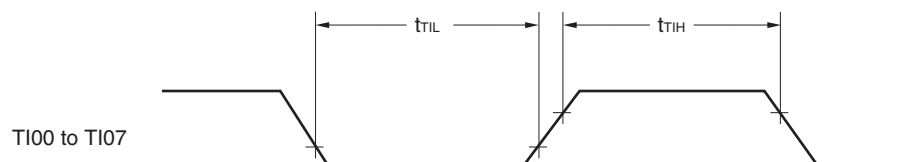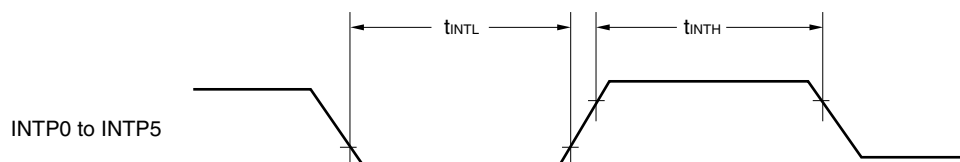**3.** Temperature condition of the TYP. value is T$_A$ = 25°C.

2.4 AC Characteristics

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T$_{CY}$	Main system clock (f$_{MAIN}$) operation	HS (High-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.125		1	μs
		During self programming	HS (High-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.125		1	μs
External main system clock frequency	f$_{EX}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V$_{DD}$ < 2.4 V			1.0		8.0	MHz
External main system clock input high-level width, low-level width	t$_{EXH}$, t$_{EXL}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			24			ns
		2.4 V ≤ V$_{DD}$ < 2.7 V			30			ns
		1.8 V ≤ V$_{DD}$ < 2.4 V			60			ns
TI00 to TI07 input high-level width, low-level width	t$_{TIH}$, t$_{TIL}$				1/f$_{MCK}$ + 10			ns
TO00 to TO07 output frequency	f$_{TO}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V					12	MHz
		2.7 V ≤ V$_{DD}$ < 4.0 V					8	MHz
		1.8 V ≤ V$_{DD}$ < 2.7 V					4	MHz
PCLBUZ0, or PCLBUZ1 output frequency	f$_{PCL}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V					16	MHz
		2.7 V ≤ V$_{DD}$ < 4.0 V					8	MHz
		1.8 V ≤ V$_{DD}$ < 2.7 V					4	MHz
INTP0 to INTP5 input high-level width, low-level width	t$_{INTH}$, t$_{INTL}$				1			μs
KR0 to KR9 input available width	t$_{KR}$				250			ns
$\overline{\text{RESET}}$ low-level width	t$_{RSL}$				10			μs

Remark   f$_{MCK}$: Timer array unit operation clock frequency

(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

AC Timing Test Point

V$_{IH}$/V$_{OH}$ V$_{IH}$/V$_{OH}$
V$_{IL}$/V$_{OL}$ Test points   V$_{IL}$/V$_{OL}$

External Main System Clock Timing

1/f$_{EX}$

t$_{EXL}$ t$_{EXH}$

EXCLK

TI/TO Timing

t$_{TIL}$ t$_{TIH}$

TI00 to TI07

1/f$_{TO}$

TO00 to TO07

Interrupt Request Input Timing

t$_{INTL}$ t$_{INTH}$

INTP0 to INTP5

Key Interrupt Input Timing

t$_{KR}$

KR0 to KR9
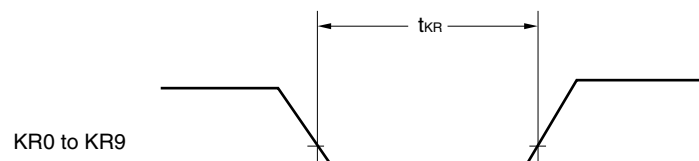
$\overline{\text{RESET}}$ Input Timing

t$_{RSL}$

$\overline{\text{RESET}}$
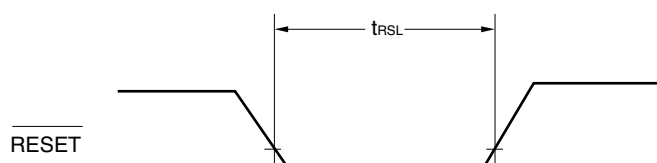
(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 4/f$_{CLK}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	167		500		ns
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	250		500		ns
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	–		500		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY1}$/2–12		t$_{KCY1}$/2–50		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY1}$/2–18		t$_{KCY1}$/2–50		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		t$_{KCY1}$/2–38		t$_{KCY1}$/2–50		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		–		t$_{KCY1}$/2–50		ns
SIp setup time (to SCKp↑) Note 1	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V		44		110		ns
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V		44		110		ns
		2.4 V ≤ V$_{DD}$ ≤ 5.5 V		75		110		ns
		1.8 V ≤ V$_{DD}$ ≤ 5.5 V		–		110		ns
SIp hold time (from SCKp↑) Note 2	t$_{KSI1}$			19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t$_{KSO1}$	C = 30 pF Note4			25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).

Remarks 1. p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products)

    2. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: "1, 3" is only for the R5F102 products.))

CSI mode connection diagram (during communication at same potential)
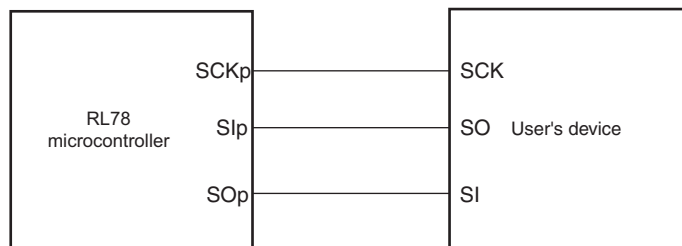
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
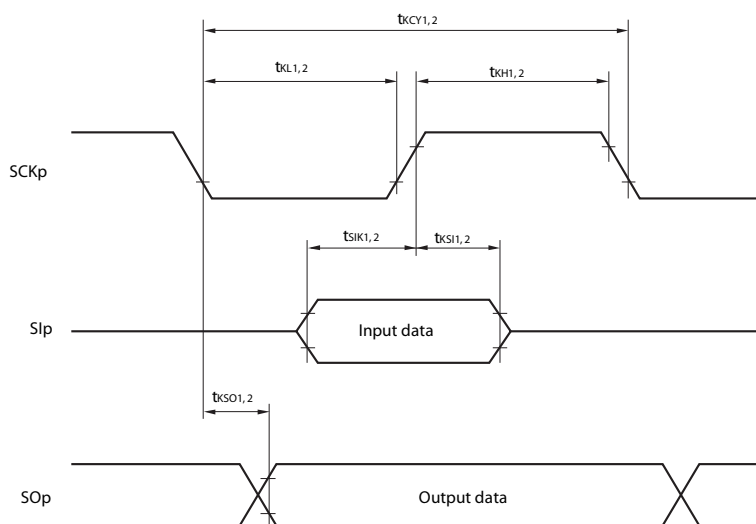
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
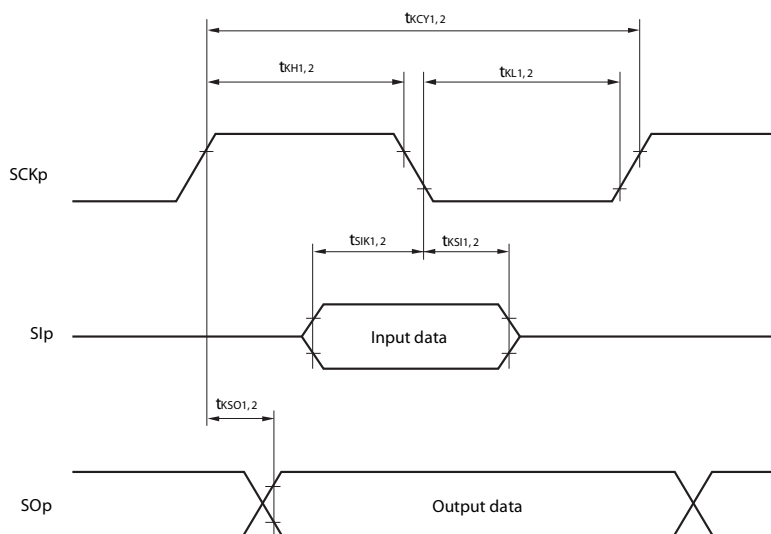
(**Remarks** are listed on the next page.)
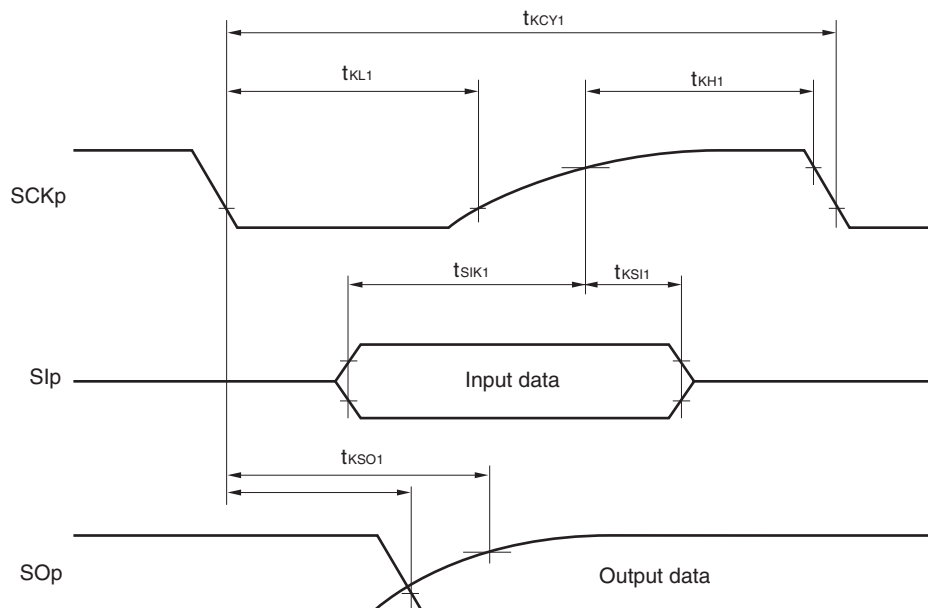
Notes 1. When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1

   2. When DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

Caution Select the TTL input buffer for the SI00 pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the SO00 pin and SCK00 pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). **For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

Remarks 1. R$_b$ [Ω]:Communication line (SCK00, SO00) pull-up resistance, C$_b$ [F]: Communication line (SCK00, SO00) load capacitance, V$_b$ [V]: Communication line voltage

   2. f$_{MCK}$: Serial array unit operation clock frequency
   (Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS00 bit of serial mode register 00 (SMR00).)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)

t_{KCY1}

t_{KL1}

t_{KH1}

SCKp

t_{SIK1} t_{KSI1}

SIp

Input data

t_{KSO1}

SOp

Output data

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

t_{KCY1}

t_{KH1}

t_{KL1}

SCKp

t_{SIK1} t_{KSI1}

SIp

Input data

t_{KSO1}

SOp

Output data

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2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (−) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (−) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (−) = AV_{REFM}
ANI0 to ANI3	Refer to **28.6.1 (1)**.	Refer to **28.6.1 (3)**.	Refer to **28.6.1 (4)**.
ANI16 to ANI22	Refer to **28.6.1 (2)**.		
Internal reference voltage	Refer to **28.6.1 (1)**.		−
Temperature sensor output voltage			

(1) When reference voltage (+) = AV_REFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV_REFM/ANI1 (ADREFM = 1), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage

(T_A = −40 to +85°C, 1.8 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (−) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD} [Note 3]			1.2	±3.5	LSB
					1.2	±7.0 [Note 4]	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2, ANI3	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
				57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±0.25	%FSR
						±0.50 [Note 4]	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±0.25	%FSR
						±0.50 [Note 4]	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±2.5	LSB
						±5.0 [Note 4]	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±1.5	LSB
						±2.0 [Note 4]	LSB
Analog input voltage	V_{AIN}	ANI2, ANI3		0		AV_{REFP}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)			V_{BGR} [Note 5]		V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)			V_{TMPS25} [Note 5]		V

(**Notes** are listed on the next page.)

2.6.2 Temperature sensor/internal reference voltage characteristics

(T$_A$ = −40 to +85°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V$_{TMPS25}$	Setting ADS register = 80H, T$_A$ = +25°C		1.05		V
Internal reference voltage	V$_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F$_{VTMPS}$	Temperature sensor output voltage that depends on the temperature		−3.6		mV/°C
Operation stabilization wait time	t$_{AMP}$		5			μs

2.6.3 POR circuit characteristics

(T$_A$ = −40 to +85°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V$_{POR}$	Power supply rise time	1.47	1.51	1.55	V
	V$_{PDR}$	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width [Note]	T$_{PW}$		300			μs

Note Minimum time required for a POR reset when V$_{DD}$ exceeds below V$_{PDR}$. This is also the minimum time required for a POR reset from when V$_{DD}$ exceeds below 0.7 V to when V$_{DD}$ exceeds V$_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).
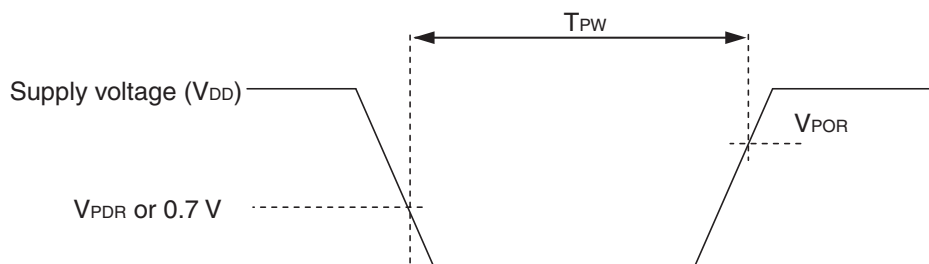
LVD detection voltage of interrupt & reset mode

(T$_A$ = −40 to +85°C, V$_{PDR}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V$_{LVDB0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 0, 1, falling reset voltage			1.80	1.84	1.87	V
	V$_{LVDB1}$	LVIS1, LVIS0 = 1, 0	Rising reset release voltage		1.94	1.98	2.02	V
			Falling interrupt voltage		1.90	1.94	1.98	V
	V$_{LVDB2}$	LVIS1, LVIS0 = 0, 1	Rising reset release voltage		2.05	2.09	2.13	V
			Falling interrupt voltage		2.00	2.04	2.08	V
	V$_{LVDB3}$	LVIS1, LVIS0 = 0, 0	Rising reset release voltage		3.07	3.13	3.19	V
			Falling interrupt voltage		3.00	3.06	3.12	V
	V$_{LVDC0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 1, 0, falling reset voltage			2.40	2.45	2.50	V
	V$_{LVDC1}$	LVIS1, LVIS0 = 1, 0	Rising reset release voltage		2.56	2.61	2.66	V
			Falling interrupt voltage		2.50	2.55	2.60	V
	V$_{LVDC2}$	LVIS1, LVIS0 = 0, 1	Rising reset release voltage		2.66	2.71	2.76	V
			Falling interrupt voltage		2.60	2.65	2.70	V
	V$_{LVDC3}$	LVIS1, LVIS0 = 0, 0	Rising reset release voltage		3.68	3.75	3.82	V
			Falling interrupt voltage		3.60	3.67	3.74	V
	V$_{LVDD0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC1}$ = 0, 1, 1, falling reset voltage			2.70	2.75	2.81	V
	V$_{LVDD1}$	LVIS1, LVIS0 = 1, 0	Rising reset release voltage		2.86	2.92	2.97	V
			Falling interrupt voltage		2.80	2.86	2.91	V
	V$_{LVDD2}$	LVIS1, LVIS0 = 0, 1	Rising reset release voltage		2.96	3.02	3.08	V
			Falling interrupt voltage		2.90	2.96	3.02	V
	V$_{LVDD3}$	LVIS1, LVIS0 = 0, 0	Rising reset release voltage		3.98	4.06	4.14	V
			Falling interrupt voltage		3.90	3.98	4.06	V

2.6.5 Power supply voltage rising slope characteristics

(T$_A$ = −40 to +85°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S$_{VDD}$				54	V/ms

Caution   Make sure to keep the internal reset state by the LVD circuit or an external reset until V$_{DD}$ reaches the operating voltage range shown in 28.4 AC Characteristics.

<R>   2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T$_A$ = −40 to +85°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V$_{DDDR}$		1.46 [Note]		5.5	V

<R>   **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.
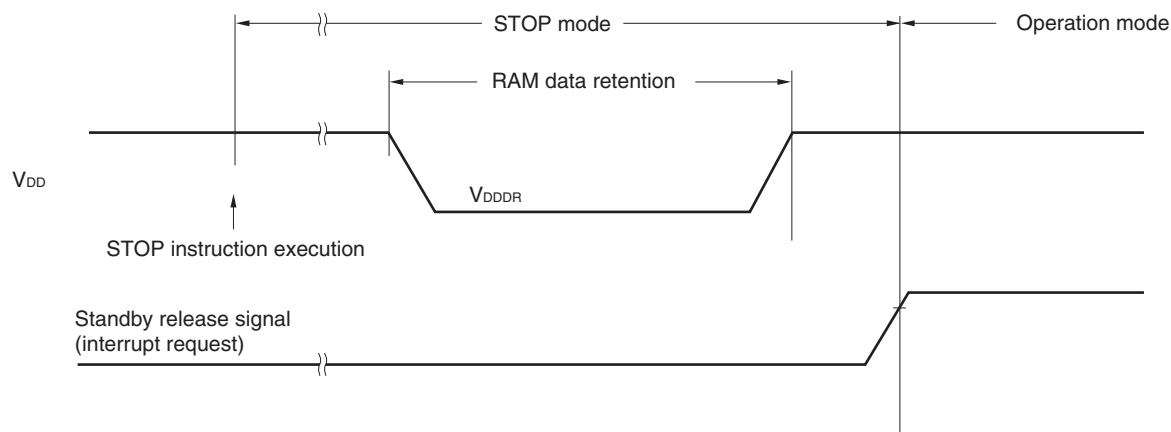
2.8 Flash Memory Programming Characteristics

(T$_A$ = −40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f$_{CLK}$		1		24	MHz
Code flash memory rewritable times [Notes 1, 2, 3]	C$_{erwr}$	Retained for 20 years T$_A$ = 85°C	1,000			Times
Data flash memory rewritable times [Notes 1, 2, 3]		Retained for 1 year T$_A$ = 25°C		1,000,000		
		Retained for 5 years T$_A$ = 85°C	100,000			
		Retained for 20 years T$_A$ = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

   2. When using flash memory programmer and Renesas Electronics self programming library

   3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V) **(3/4)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	Normal input buffer 20-, 24-pin products: P00 to P03**Note 2**, P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147		0.8V$_{DD}$		V$_{DD}$	V
	V$_{IH2}$	TTL input buffer 20-, 24-pin products: P10, P11 30-pin products: P01, P10, P11, P13 to P17	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	2.2		V$_{DD}$	V
			3.3 V ≤ V$_{DD}$ < 4.0 V	2.0		V$_{DD}$	V
			2.4 V ≤ V$_{DD}$ < 3.3 V	1.5		V$_{DD}$	V
	V$_{IH3}$	Normal input buffer P20 to P23		0.7V$_{DD}$		V$_{DD}$	V
	V$_{IH4}$	P60, P61		0.7V$_{DD}$		6.0	V
	V$_{IH5}$	P121, P122, P125**Note 1**, P137, EXCLK, $\overline{RESET}$		0.8V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	Normal input buffer 20-, 24-pin products: P00 to P03**Note 2**, P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147		0		0.2V$_{DD}$	V
	V$_{IL2}$	TTL input buffer 20-, 24-pin products: P10, P11 30-pin products: P01, P10, P11, P13 to P17	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	0		0.8	V
			3.3 V ≤ V$_{DD}$ < 4.0 V	0		0.5	V
			2.4 V ≤ V$_{DD}$ < 3.3 V	0		0.32	V
	V$_{IL3}$	P20 to P23		0		0.3V$_{DD}$	V
	V$_{IL4}$	P60, P61		0		0.3V$_{DD}$	V
	V$_{IL5}$	P121, P122, P125**Note 1**, P137, EXCLK, $\overline{RESET}$		0		0.2V$_{DD}$	V
Output voltage, high	V$_{OH1}$	20-, 24-pin products: P00 to P03**Note 2**, P10 to P14, P40 to P42 30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH1}$ = −3.0 mA	V$_{DD}$−0.7			V
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH1}$ = −2.0 mA	V$_{DD}$−0.6			V
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH1}$ = −1.5 mA	V$_{DD}$−0.5			V
	V$_{OH2}$	P20 to P23	I$_{OH2}$ = −100 μA	V$_{DD}$−0.5			V

Notes 1. 20, 24-pin products only.

2. 24-pin products only.

Caution The maximum value of V$_{IH}$ of pins P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products is V$_{DD}$ even in N-ch open-drain mode. High level is not output in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) 30-pin products

(TA = –40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V)   (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	IDD1	Operating mode	HS (High-speed main) mode[Note 4]	fIH = 24 MHz[Note 3]	Basic operation	VDD = 5.0 V		1.5		mA
						VDD = 3.0 V		1.5		
					Normal operation	VDD = 5.0 V		3.7	5.8	mA
						VDD = 3.0 V		3.7	5.8	
				fIH = 16 MHz[Note 3]		VDD = 5.0 V		2.7	4.2	mA
						VDD = 3.0 V		2.7	4.2	
				fMX = 20 MHz[Note 2], VDD = 5.0 V		Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	
				fMX = 20 MHz[Note 2], VDD = 3.0 V		Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	
				fMX = 10 MHz[Note 2], VDD = 5.0 V		Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	
				fMX = 10 MHz[Note 2], VDD = 3.0 V		Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	

Notes 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator clock is stopped.

3. When high-speed system clock is stopped

4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS(High speed main) mode: VDD = 2.7 V to 5.5 V @1 MHz to 24 MHz

VDD = 2.4 V to 5.5 V @1 MHz to 16 MHz

Remarks 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. fIH: high-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is TA = 25°C.

(3) Peripheral functions (Common to all products)

(T$_A$ = –40 to +105°C, 2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed onchip oscillator operating current	I$_{FIL}$ [Note 1]				0.20		μA
12-bit interval timer operating current	I$_{TMKA}$ [Notes 1, 2, 3]				0.02		μA
Watchdog timer operating current	I$_{WDT}$ [Notes 1, 2, 4]	f$_{IL}$ = 15 kHz			0.22		μA
A/D converter operating current	I$_{ADC}$ [Notes 1, 5]	When conversion at maximum speed	Normal mode, AV$_{REFP}$ = V$_{DD}$ = 5.0 V		1.30	1.70	mA
			Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		0.50	0.70	mA
A/D converter reference voltage operating current	I$_{ADREF}$ [Note 1]				75.0		μA
Temperature sensor operating current	I$_{TMPS}$ [Note 1]				75.0		μA
LVD operating current	I$_{LVD}$ [Notes 1, 6]				0.08		μA
Self-programming operating current	I$_{FSP}$ [Notes 1, 8]				2.00	12.20	mA
BGO operating current	I$_{BGO}$ [Notes 1, 7]				2.00	12.20	mA
SNOOZE operating current	I$_{SNOZ}$ [Note 1]	ADC operation	The mode is performed [Note 9]		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		1.20	2.04	mA
		CSI/UART operation			0.70	1.54	mA

Notes 1. Current flowing to the V$_{DD}$.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$, and I$_{FIL}$ and I$_{TMKA}$ when the 12-bit interval timer operates.

4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{WDT}$ when the watchdog timer operates.

5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I$_{DD1}$ or I$_{DD2}$ and I$_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

6. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{LVD}$ when the LVD circuit operates.

7. Current flowing only during data flash rewrite.

8. Current flowing only during self programming.

9. For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode**.

Remarks 1. f$_{IL}$: Low-speed on-chip oscillator clock frequency

2. Temperature condition of the TYP. value is T$_A$ = 25°C

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (−) = AV$_{REFM}$ (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = V$_{BGR}$ [Note 3], Reference voltage (−) = AV$_{REFM}$ [Note 4] = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$			8		bit
Conversion time	t$_{CONV}$	8-bit resolution	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	8-bit resolution			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution			±1.0	LSB
Analog input voltage	V$_{AIN}$		0		V$_{BGR}$ [Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **29.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (−) = V$_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AV$_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

3.9 Dedicated Flash Memory Programmer Communication (UART)

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.10 Timing of Entry to Flash Memory Programming Modes

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t$_{SUINIT}$	POR and LVD reset are released before external release			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t$_{SU}$	POR and LVD reset are released before external release	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t$_{HD}$	POR and LVD reset are released before external release	1			ms
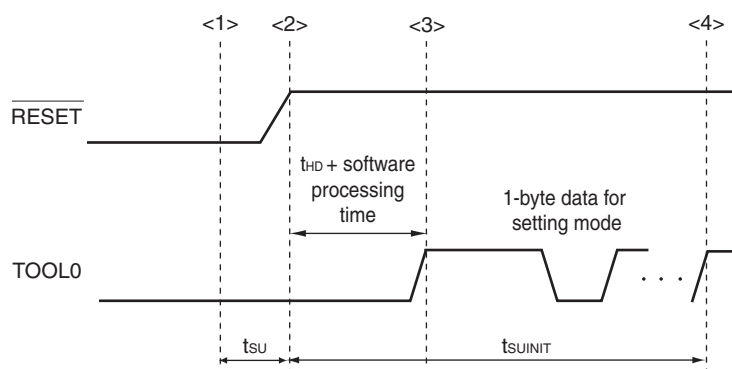
<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t$_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t$_{SU}$:   Time to release the external reset after the TOOL0 pin is set to the low level

t$_{HD}$:   Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

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