Microchip Technology - ATXMEGA16A4-AUR Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16a4-aur

9. Event System

9.1 Features

- **Inter-peripheral communication and signalling with minimum latency**
- **CPU and DMA independent operation**
- **8 Event Channels allow for up to 8 signals to be routed at the same time**
- **Events can be generated by**
  - **TImer/Counters (TCxn)**
  - **Real Time Counter (RTC)**
  - **Analog to Digital Converters (ADCx)**
  - **Analog Comparators (ACx)**
  - **Ports (PORTx)**
  - **System Clock (Clk$_{SYS}$)**
  - **Software (CPU)**
- **Events can be used by**
  - **TImer/Counters (TCxn)**
  - **Analog to Digital Converters (ADCx)**
  - **Digital to Analog Converters (DACx)**
  - **Ports (PORTx)**
  - **DMA Controller (DMAC)**
  - **IR Communication Module (IRCOM)**
- **The same event can be used by multiple peripherals for synchronized timing**
- **Advanced Features**
  - **Manual Event Generation from software (CPU)**
  - **Quadrature Decoding**
  - **Digital Filtering**
- **Functions in Active and Idle mode**

9.2 Overview

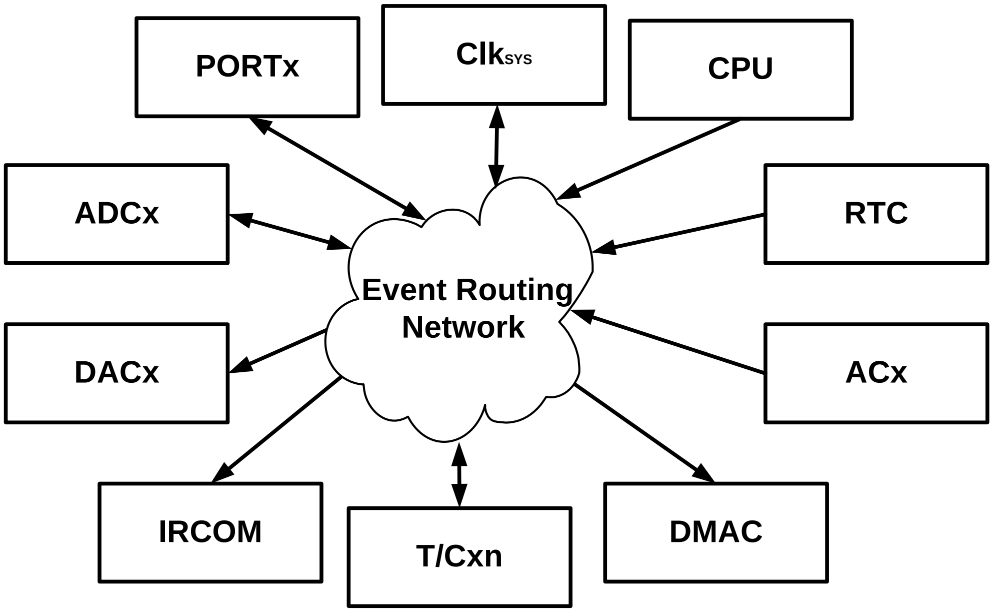
The Event System is a set of features for inter-peripheral communication. It enables the possibility for a change of state in one peripheral to automatically trigger actions in one or more peripherals. Whose changes in a peripheral that will trigger actions in other peripherals are configurable by software. It is a simple, but powerful system as it allows for autonomous control of peripherals without any use of interrupts, CPU or DMA resources.

The indication of a change in a peripheral is referred to as an event, and is usually the same as the interrupt conditions for that peripheral. Events are passed between peripherals using a dedicated routing network called the Event Routing Network. Figure 9-1 on page 17 shows a basic block diagram of the Event System with the Event Routing Network and the peripherals to which it is connected. This highly flexible system can be used for simple routing of signals, pin functions or for sequencing of events.

The maximum latency is two CPU clock cycles from when an event is generated in one peripheral, until the actions are triggered in one or more other peripherals.

The Event System is functional in both Active and Idle modes.

Figure 9-1. Event System Block Diagram



The Event Routing Network can directly connect together ADCs, DACs, Analog Comparators (ACx), I/O ports (PORTx), the Real-time Counter (RTC), Timer/Counters (T/C) and the IR Communication Module (IRCOM). Events can also be generated from software (CPU).

All events from all peripherals are always routed into the Event Routing Network. This consist of eight multiplexers where each can be configured in software to select which event to be routed into that event channel. All eight event channels are connected to the peripherals that can use events, and each of these peripherals can be configured to use events from one or more event channels to automatically trigger a software selectable action.

12. System Control and Reset

12.1 Features

- **Multiple reset sources for safe operation and device reset**
  - **Power-On Reset**
  - **External Reset**
  - **Watchdog Reset**
    The Watchdog Timer runs from separate, dedicated oscillator
  - **Brown-Out Reset**
    Accurate, programmable Brown-Out levels
  - **PDI reset**
  - **Software reset**
- **Asynchronous reset**
  - **No running clock in the device is required for reset**
- **Reset status register**

12.2 Resetting the AVR

During reset, all I/O registers are set to their initial values. The SRAM content is not reset. Application execution starts from the Reset Vector. The instruction placed at the Reset Vector should be an Absolute Jump (JMP) instruction to the reset handling routine. By default the Reset Vector address is the lowest Flash program memory address, ‘0’, but it is possible to move the Reset Vector to the first address in the Boot Section.

The I/O ports of the AVR are immediately tri-stated when a reset source goes active.

The reset functionality is asynchronous, so no running clock is required to reset the device.

After the device is reset, the reset source can be determined by the application by reading the Reset Status Register.

12.3 Reset Sources

12.3.1 Power-On Reset

The MCU is reset when the supply voltage VCC is below the Power-on Reset threshold voltage.

12.3.2 External Reset

The MCU is reset when a low level is present on the RESET pin.

12.3.3 Watchdog Reset

The MCU is reset when the Watchdog Timer period expires and the Watchdog Reset is enabled. The Watchdog Timer runs from a dedicated oscillator independent of the System Clock. For more details see ”WDT - Watchdog Timer” on page 24.

12.3.4 Brown-Out Reset

The MCU is reset when the supply voltage VCC is below the Brown-Out Reset threshold voltage and the Brown-out Detector is enabled. The Brown-out threshold voltage is programmable.

14. PMIC - Programmable Multi-level Interrupt Controller

14.1 Features

- **Separate interrupt vector for each interrupt**
- **Short, predictable interrupt response time**
- **Programmable Multi-level Interrupt Controller**
  - **3 programmable interrupt levels**
  - **Selectable priority scheme within low level interrupts (round-robin or fixed)**
  - **Non-Maskable Interrupts (NMI)**
- **Interrupt vectors can be moved to the start of the Boot Section**

14.2 Overview

XMEGA A4 has a Programmable Multi-level Interrupt Controller (PMIC). All peripherals can define three different priority levels for interrupts; high, medium or low. Medium level interrupts may interrupt low level interrupt service routines. High level interrupts may interrupt both low- and medium level interrupt service routines. Low level interrupts have an optional round robin scheme to make sure all interrupts are serviced within a certain amount of time.

The built in oscillator failure detection mechanism can issue a Non-Maskable Interrupt (NMI).

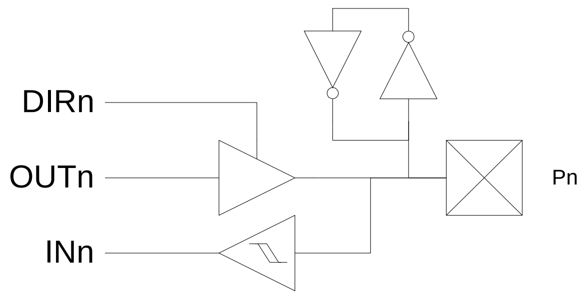
14.3 Interrupt vectors

When an interrupt is serviced, the program counter will jump to the interrupt vector address. The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the XMEGA A4 devices are shown in Table 14-1. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA A manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 14-1. The program address is the word address.

Table 14-1. Reset and Interrupt Vectors

Program Address (Base Address)	Source	Interrupt Description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal Oscillator Failure Interrupt vector (NMI)
0x004	PORTC_INT_base	Port C Interrupt base
0x008	PORTR_INT_base	Port R Interrupt base
0x00C	DMA_INT_base	DMA Controller Interrupt base
0x014	RTC_INT_base	Real Time Counter Interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C Interrupt base
0x01C	TCC0_INT_base	Timer/Counter 0 on port C Interrupt base
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x038	USARTC1_INT_base	USART 1 on port C Interrupt base
0x03E	AES_INT_vect	AES Interrupt vector

Figure 15-4. I/O configuration - Totem-pole with bus-keeper



15.3.5 Others

Figure 15-5. Output configuration - Wired-OR with optional pull-down

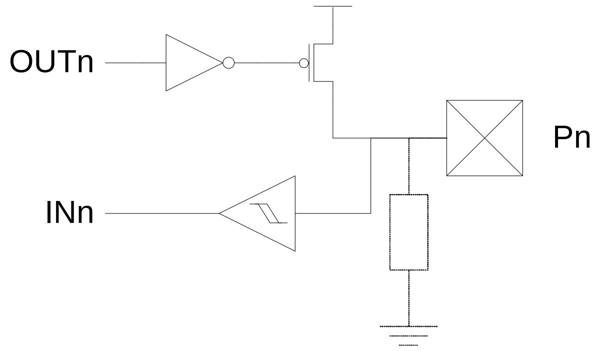
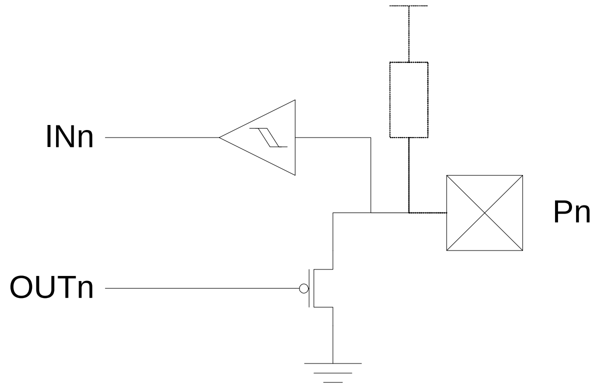


Figure 15-6. I/O configuration - Wired-AND with optional pull-up

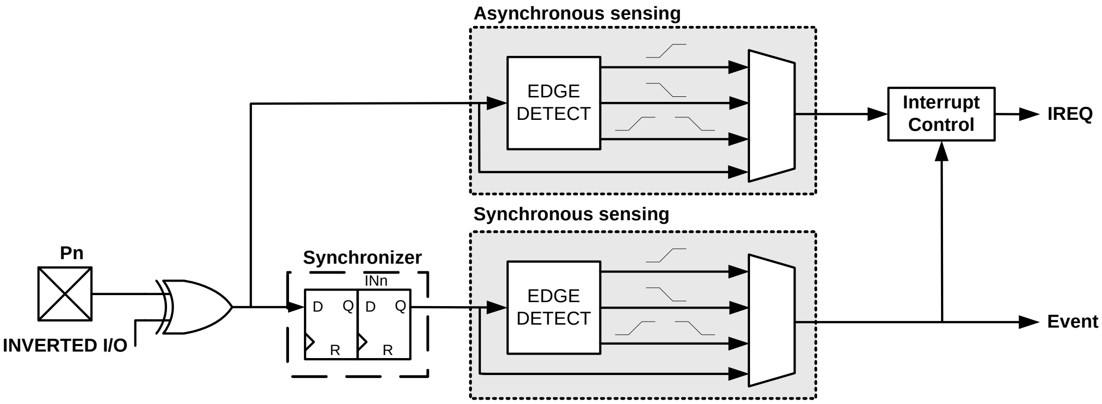


15.4 Input sensing

- **Sense both edges**
- **Sense rising edges**
- **Sense falling edges**
- **Sense low level**

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 15-7 on page 30.

Figure 15-7. Input sensing system overview



When a pin is configured with inverted I/O, the pin value is inverted before the input sensing.

15.5 Port Interrupt

Each port has two interrupts with separate priority and interrupt vector. All pins on the port can be individually selected as source for each of the interrupts. The interrupts are then triggered according to the input sense configuration for each pin configured as source for the interrupt.

15.6 Alternate Port Functions

In addition to the input/output functions on all port pins, most pins have alternate functions. This means that other modules or peripherals connected to the port can use the port pins for their functions, such as communication or pulse-width modulation. ”Pinout and Pin Functions” on page 49 shows which modules on peripherals that enable alternate functions on a pin, and which alternate function is available on a pin.

19. RTC - 16-bit Real-Time Counter

19.1 Features

- **16-bit Timer**
- **Flexible Tick resolution ranging from 1 Hz to 32.768 kHz**
- **One Compare register**
- **One Period register**
- **Clear timer on Overflow or Compare Match**
- **Overflow or Compare Match event and interrupt generation**

19.2 Overview

The XMEGA A4 includes a 16-bit Real-time Counter (RTC). The RTC can be clocked from an accurate 32.768 kHz Crystal Oscillator, the 32.768 kHz Calibrated Internal Oscillator, or from the 32 kHz Ultra Low Power Internal Oscillator. The RTC includes both a Period and a Compare register. For details, see Figure 19-1.

A wide range of Resolution and Time-out periods can be configured using the RTC. With a maximum resolution of 30.5 µs, time-out periods range up to 2000 seconds. With a resolution of 1 second, the maximum time-out period is over 18 hours (65536 seconds).

Figure 19-1. Real Time Counter overview

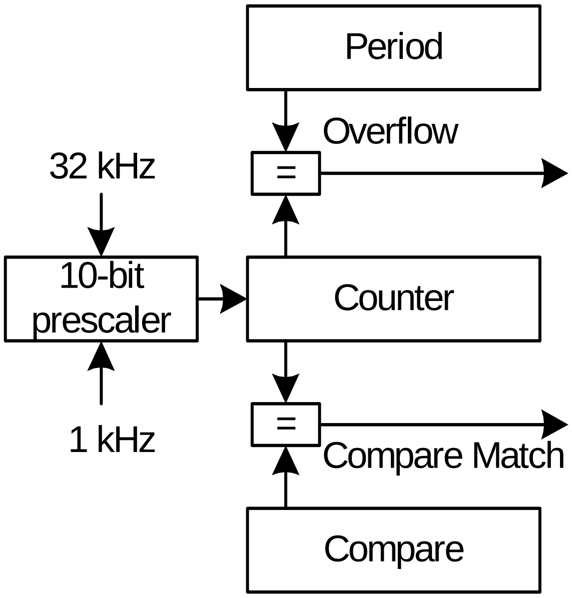


Table 30-4. Port D - Alternate functions

PORTD	PIN #	INTERRUPT	TCD0	TCD1	USARTD0	USARTD1	SPID	CLOCKOUT	EVENTOUT
GND	18								
VCC	19								
PD0	20	SYNC	OC0A						
PD1	21	SYNC	OC0B		XCK0				
PD2	22	SYNC/ASYNC	OC0C		RXD0				
PD3	23	SYNC	OC0D		TXD0				
PD4	24	SYNC		OC1A			$\overline{\text{SS}}$		
PD5	25	SYNC		OC1B		XCK1	MOSI		
PD6	26	SYNC				RXD1	MISO		
PD7	27	SYNC				TXD1	SCK	CLKOUT	EVOUT

Table 30-5. Port E - Alternate functions

PORT E	PIN #	INTERRUPT	TCE0	USARTE0	TWIE
PE0	28	SYNC	OC0A		SDA
PE1	29	SYNC	OC0B	XCK0	SCL
GND	30				
VCC	31				
PE2	32	SYNC/ASYNC	OC0C	RXD0	
PE3	33	SYNC	OC0D	TXD0	

Table 30-6. Port R - Alternate functions

PORTR	PIN #	XTAL	PDI	TOSC
PDI	34		PDI_DATA	
$\overline{\text{RESET}}$	35		PDI_CLK	
PR0	36	XTAL2		TOSC2
PR1	37	XTAL1		TOSC1

32. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	Rd ← Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd ← Rd + Rr + C	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	Rd ← Rd + 1:Rd + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	Rd ← Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd ← Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd ← Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd ← Rd - K - C	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	Rd + 1:Rd ← Rd + 1:Rd - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	Rd ← Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd ← Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd ← Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd ← Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd ← Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One’s Complement	Rd ← $FF - Rd	Z,C,N,V,S	1
NEG	Rd	Two’s Complement	Rd ← $00 - Rd	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FFh - K)	Z,N,V,S	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V,S	1
DEC	Rd	Decrement	Rd ← Rd - 1	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V,S	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V,S	1
SER	Rd	Set Register	Rd ← $FF	None	1
MUL	Rd,Rr	Multiply Unsigned	R1:R0 ← Rd x Rr (UU)	Z,C	2
MULS	Rd,Rr	Multiply Signed	R1:R0 ← Rd x Rr (SS)	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr (SU)	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	R1:R0 ← Rd x Rr<<1 (UU)	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	R1:R0 ← Rd x Rr<<1 (SS)	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← Rd x Rr<<1 (SU)	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 ← Encrypt(R15:R0, K) else if (H = 1) then R15:R0 ← Decrypt(R15:R0, K)		1/2
Branch Instructions					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2
EIJMP		Extended Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	2
JMP	k	Jump	PC ← k	None	3
RCALL	k	Relative Call Subroutine	PC ← PC + k + 1	None	2 / 3(1)
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2 / 3(1)
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	3(1)

34.6 DAC Characteristics

Table 34-7. DAC Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
INL	Integral Non-Linearity	V_{CC} = 1.6-3.6V	VREF = Ext. ref		±5		LSB
DNL	Differential Non-Linearity	V_{CC} = 1.6-3.6V	VREF = Ext. ref		<±1		
			VREF= AV_{CC}				
F_{clk}	Conversion rate					1000	ksps
AREF	External reference voltage			1.1		AV_{CC}-0.6	V
	Reference input impedance				>10		MΩ
	Max output voltage	R_{load}=100kΩ			AV_{CC}*0.98		V
	Min output voltage	R_{load}=100kΩ			<0.030		
	Offset factory calibration accuracy	Continues mode, V_{CC}=3.0V, VREF = Int 1.00V, T=85°C			±0.5		LSB
	Gain factory calibration accuracy				±2.5		

34.7 Analog Comparator Characteristics

Table 34-8. Analog Comparator Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
V_{off}	Input Offset Voltage	V_{CC} = 1.6 - 3.6V			< ±10		mV
I_{lk}	Input Leakage Current	V_{CC} = 1.6 - 3.6V			< 1000		pA
V_{hys1}	Hysteresis, No	V_{CC} = 1.6 - 3.6V			0		mV
V_{hys2}	Hysteresis, Small	V_{CC} = 1.6 - 3.6V	mode = HS		20		mV
V_{hys3}	Hysteresis, Large	V_{CC} = 1.6 - 3.6V	mode = HS		40		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C	mode = HS		90		ns
		V_{CC} = 1.6 - 3.6V	mode = LP		175		

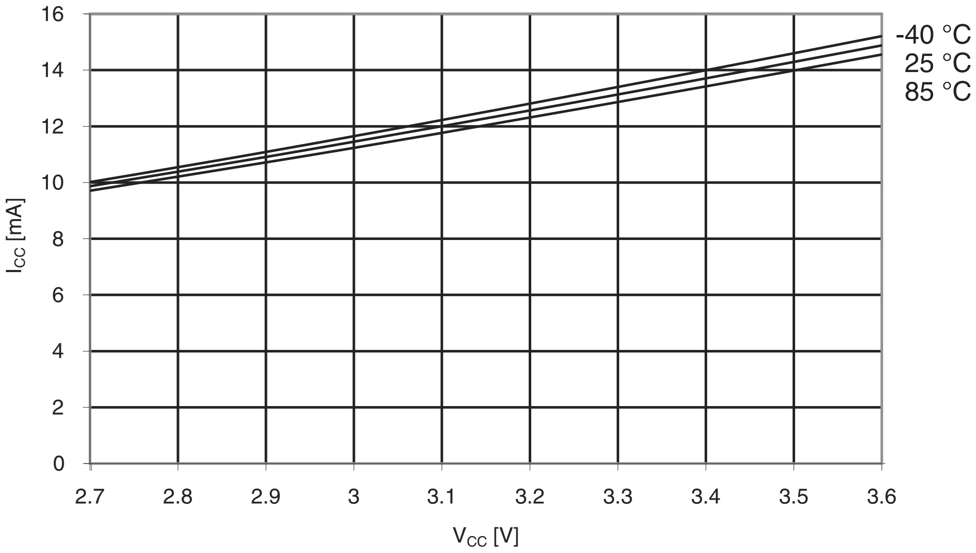
34.8 Bandgap Characteristics

Table 34-9. Bandgap Voltage Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Bandgap Startup Time	As reference to ADC or DAC	1 Clk_PER + 2.5µs			µs
		As input to AC or ADC		1.5		
	Bandgap voltage			1.1		V
	ADC/DAC ref	T= 85°C, After calibration	0.99	1	1.01	
				1		
	Variation over voltage and temperature	V_{CC} = 1.6 - 3.6V, T_A = -40°C to 85°C		±2		%

Figure 35-7. Active Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC.



35.2 Idle Supply Current

Figure 35-8. Idle Supply Current vs. Frequency

f_{SYS} = 0 - 1.0 MHz, T = 25°C.

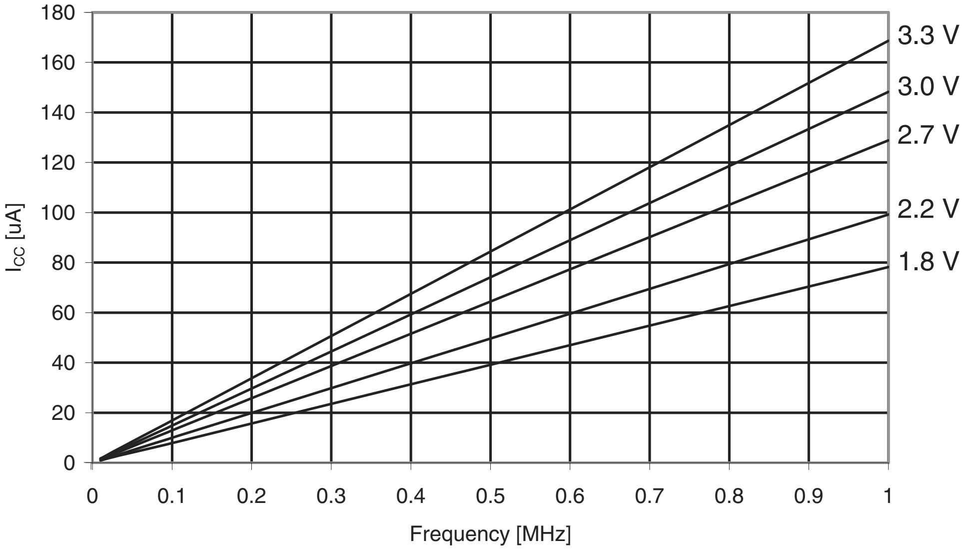


Figure 35-13. Idle Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC prescaled to 8 MHz.

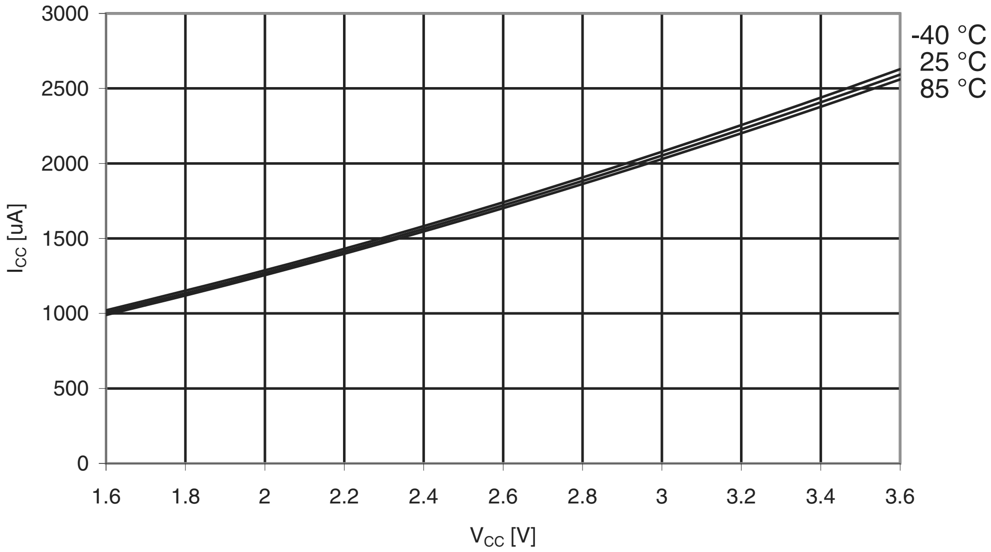
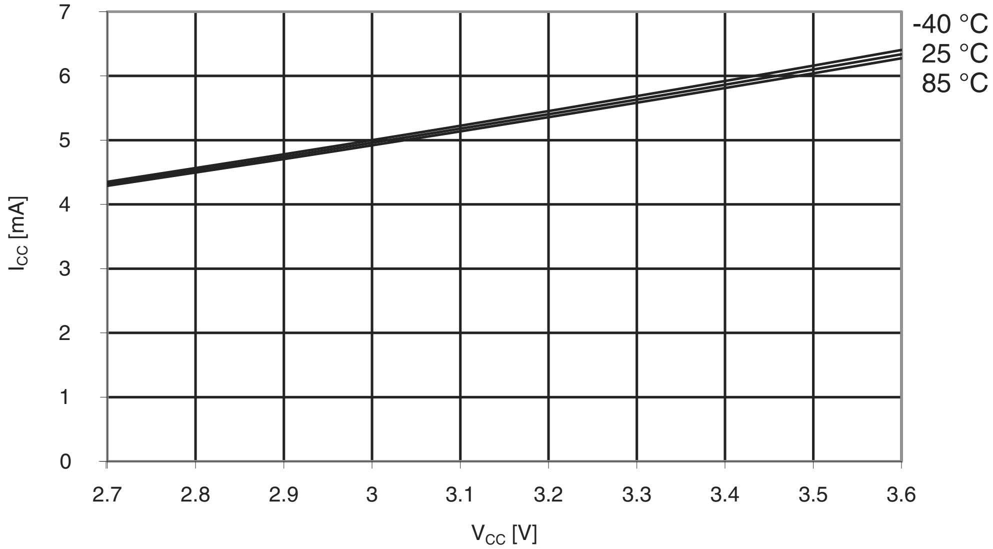


Figure 35-14. Idle Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC.



35.3 Power-down Supply Current

Figure 35-15. Power-down Supply Current vs. Temperature

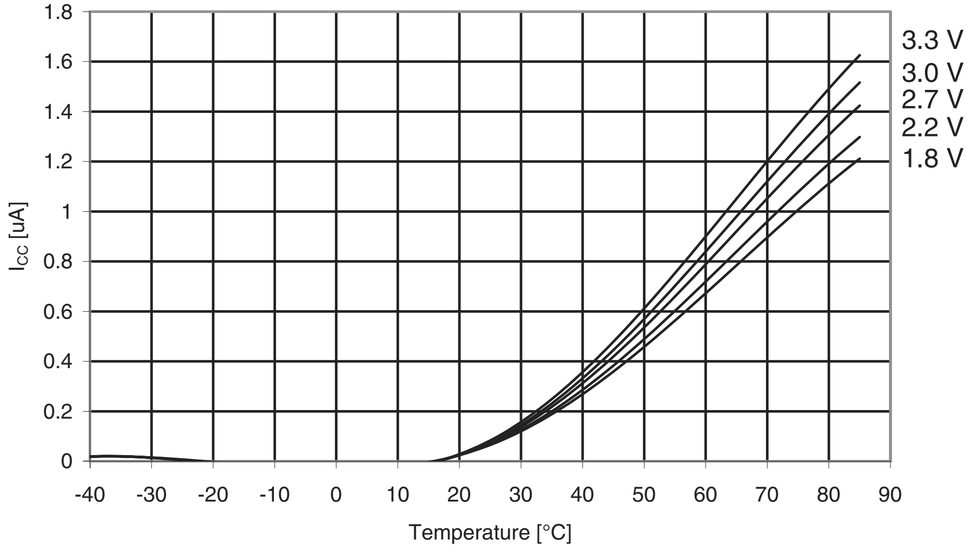


Figure 35-16. Power-down Supply Current vs. Temperature

With WDT and sampled BOD enabled.

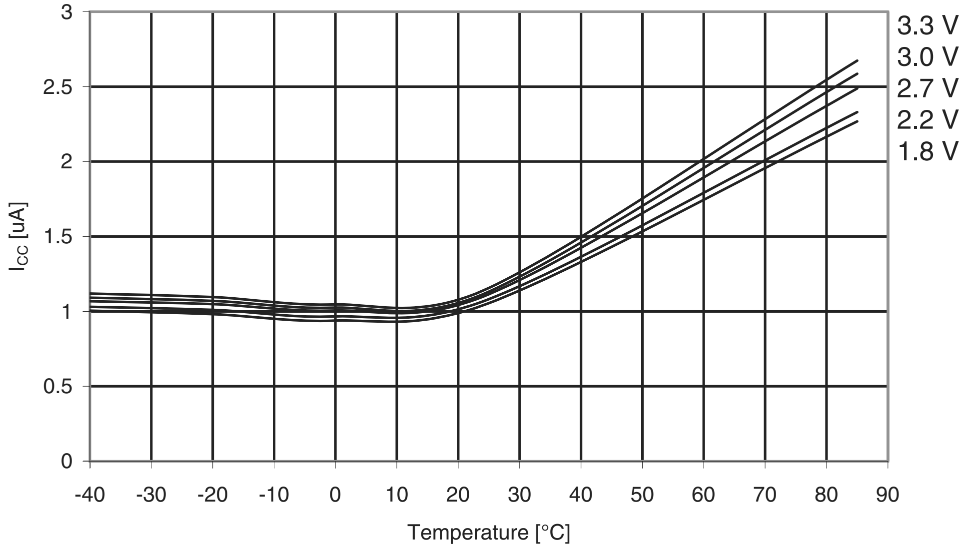


Figure 35-29. I/O Pin Input Hysteresis vs. $V_{CC.}$

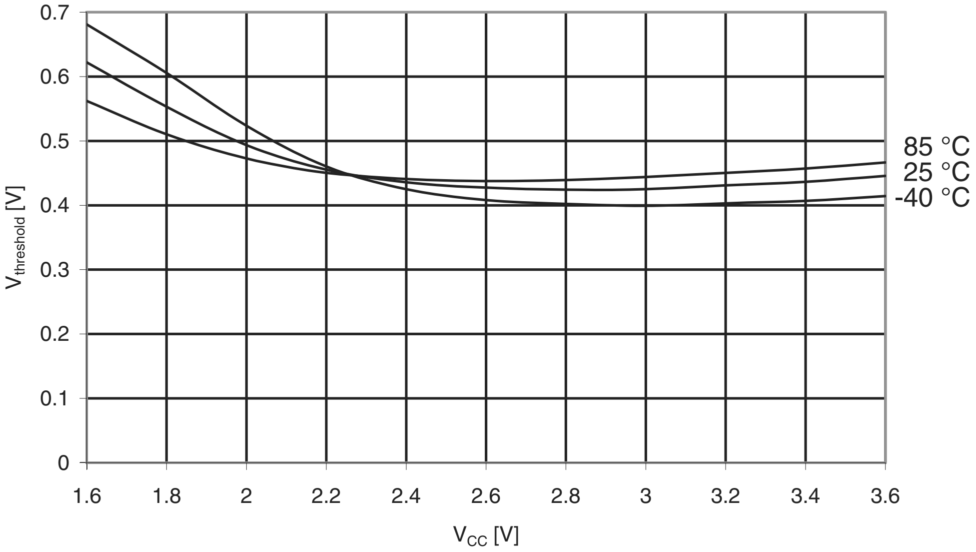


Figure 35-30. Reset Input Threshold Voltage vs. V_{CC}

V_{IH} - I/O Pin Read as “1”.

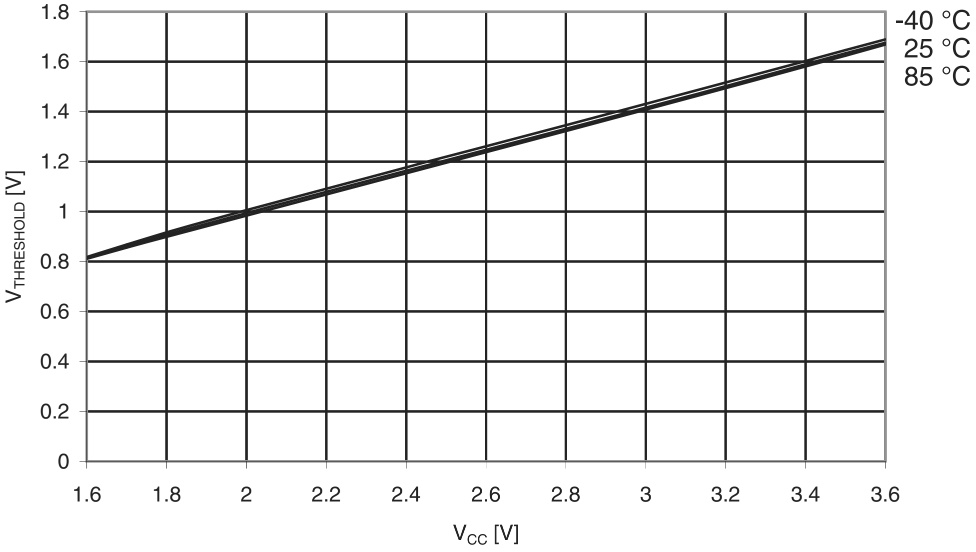
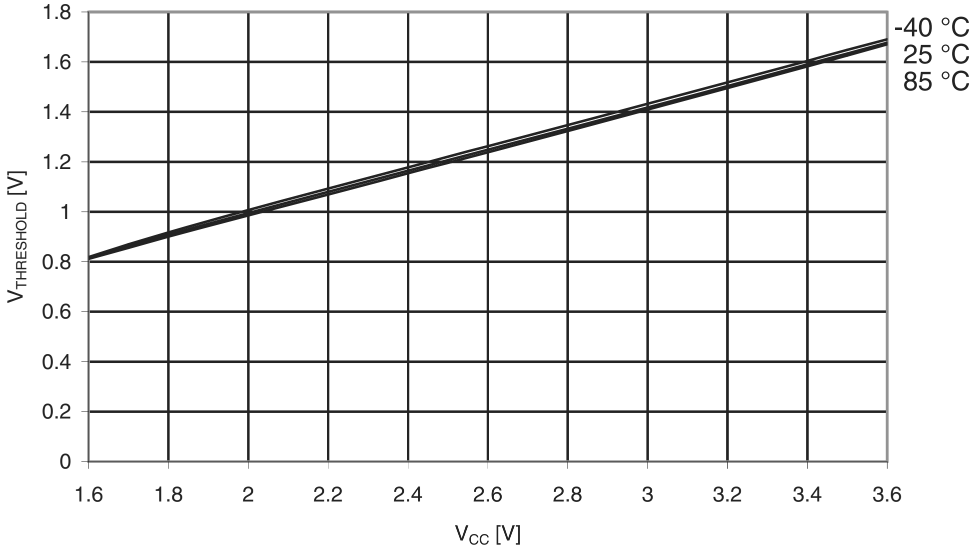


Figure 35-31. Reset Input Threshold Voltage vs. V_{CC}

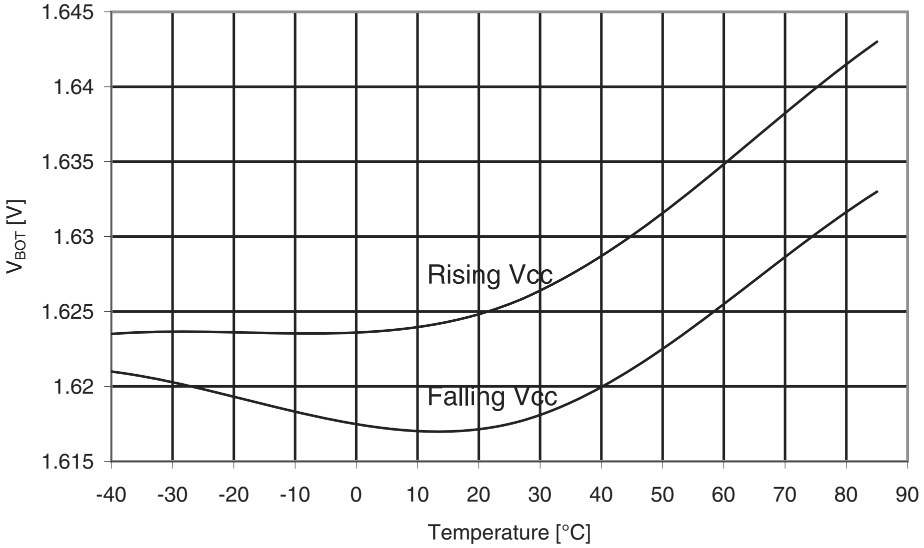
V_{IL} - I/O Pin Read as “0”.



35.8 Bod Thresholds

Figure 35-32. BOD Thresholds vs. Temperature

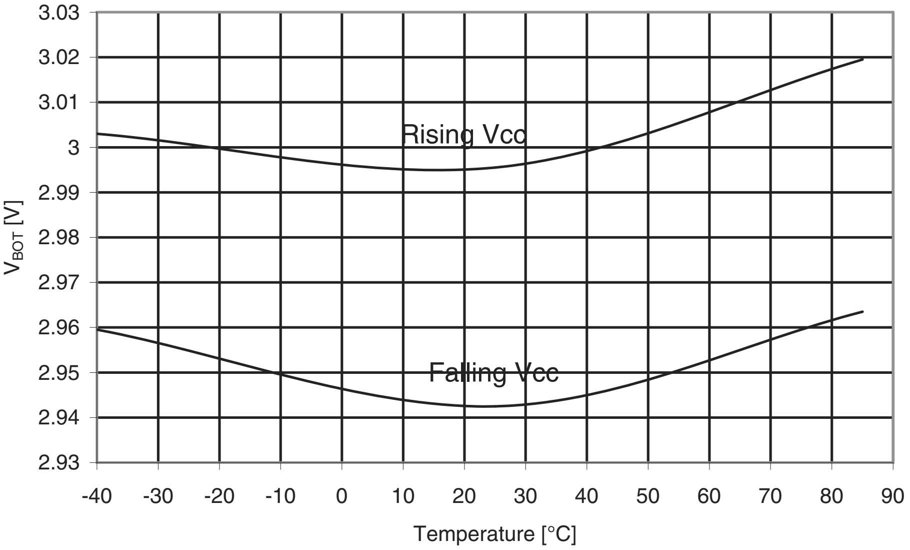
BOD Level = 1.6V.



Not recommended for new designs - Use XMEGA A4U series

Figure 35-33. BOD Thresholds vs. Temperature

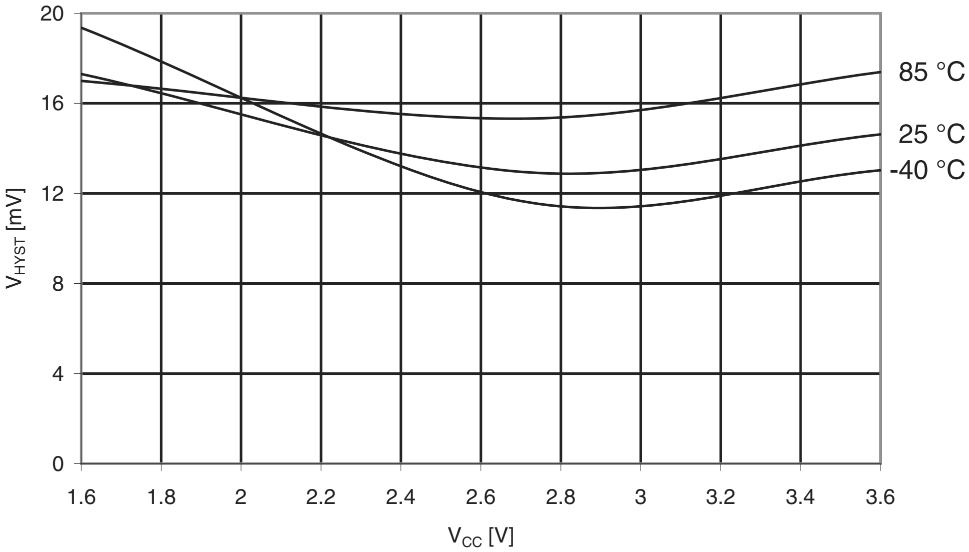
BOD Level = 2.9V.



35.9 Analog Comparator

Figure 35-34. Analog Comparator Hysteresis vs. V_{CC}

High-speed, Small hysteresis.



36. Errata

36.1 ATxmega16A4, ATxmega32A4

36.1.1 rev. A/B

- **Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously**
- **VCC voltage scaler for AC is non-linear**
- **ADC has increased INL error for some operating conditions**
- **ADC gain stage output range is limited to 2.4 V**
- **ADC Event on compare match non-functional**
- **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**
- **Accuracy lost on first three samples after switching input to ADC gain stage**
- **Configuration of PGM and CWCM not as described in XMEGA A Manual**
- **PWM is not restarted properly after a fault in cycle-by-cycle mode**
- **BOD: BOD will be enabled at any reset**
- **Sampled BOD in Active mode will cause noise when bandgap is used as reference**
- **DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V**
- **DAC has increased INL or noise for some operating conditions**
- **EEPROM page buffer always written when NVM DATA0 is written**
- **Pending full asynchronous pin change interrupts will not wake the device**
- **Pin configuration does not affect Analog Comparator Output**
- **NMI Flag for Crystal Oscillator Failure automatically cleared**
- **Flash Power Reduction Mode can not be enabled when entering sleep**
- **Crystal start-up time required after power-save even if crystal is source for RTC**
- **RTC Counter value not correctly read after sleep**
- **Pending asynchronous RTC-interrupts will not wake up device**
- **TWI Transmit collision flag not cleared on repeated start**
- **Clearing TWI Stop Interrupt Flag may lock the bus**
- **TWI START condition at bus timeout will cause transaction to be dropped**
- **TWI Data Interrupt Flag (DIF) erroneously read as set**
- **WDR instruction inside closed window will not issue reset**

1. **Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously**

   If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1 µs and could potentially give a wrong comparison result.

   Problem fix/Workaround

   If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. **VCC voltage scaler for AC is non-linear**

   The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4 V in order to get a correct result, or keep ADC voltage reference below 2.4 V.

5. **ADC Event on compare match non-functional**

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/Workaround

Enable and use interrupt on compare match when using the compare function.

6. **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**

The ADC can not be used to do bandgap measurements when VCC is below 2.7V.

Problem fix/Workaround

None.

7. **Accuracy lost on first three samples after switching input to ADC gain stage**

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

8. **Configuration of PGM and CWCM not as described in XMEGA A Manual**

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 36-1. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

9. **PWM is not restarted properly after a fault in cycle-by-cycle mode**

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

10. **BOD will be enabled after any reset**

If any reset source goes active, the BOD will be enabled and keep the device in reset if the VCC voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until VCC is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

11. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC, DAC and Analog Comparator.

Problem fix/Workaround

If the bandgap is used as reference for either the ADC, DAC or the Analog Comparator, the BOD must not be set in sampled mode.

12. DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V

Using the DAC with a reference voltage above 2.4V or VCC - 0.6V will give inaccurate output when converting codes that give below 0.75V output:

– ±10 LSB for continuous mode

– ±200 LSB for Sample and Hold mode

Problem fix/Workaround

None.

13. DAC has increased INL or noise for some operating conditions

Some DAC configurations or operating condition will result in increased output error.

– Continous mode: ±5 LSB

– Sample and hold mode: ±15 LSB

– Sample and hold mode for reference above 2.0v: up to ±100 LSB

Problem fix/Workaround

None.

14. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

15. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

16. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.

Problem fix/Workaround

None for Output/Pull configuration.

For inverted I/O, configure the Analog Comparator to give an inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

17. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

18. Flash Power Reduction Mode can not be enabled when entering sleep

If Flash Power Reduction Mode is enabled when entering Power-save or Extended Standby sleep mode, the device will only wake up on every fourth wake-up request. If Flash Power Reduction Mode is enabled when entering Idle sleep mode, the wake-up time will vary with up to 16 CPU clock cycles.

Problem fix/Workaround

Disable Flash Power Reduction mode before entering sleep mode.

19. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768 kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA A Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

20. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

21. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

22. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.