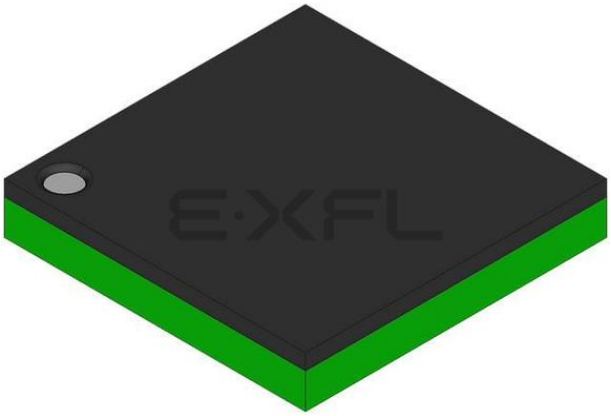

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | AVR |
| Core Size | 8/16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 34 |
| Program Memory Size | 16KB (8K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 3.6V |
| Data Converters | A/D 12x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 49-VFBGA |
| Supplier Device Package | 49-VFBGA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/atmel/atxmega16a4-cu |

# 1. Ordering Information

| Ordering Code | Flash | $E^2$ | SRAM | Speed (MHz) | Power Supply | Package[1][2][3] | Temp |
|---|---|---|---|---|---|---|---|
| ATxmega128A4-AU | 128 KB + 8 KB | 2 KB | 8 KB | 32 | 1.6 - 3.6V | 44A | -40°C - 85°C |
| ATxmega64A4-AU | 64 KB + 4 KB | 2 KB | 4 KB | 32 | 1.6 - 3.6V | | |
| ATxmega32A4-AU | 32 KB + 4 KB | 1 KB | 4 KB | 32 | 1.6 - 3.6V | | |
| ATxmega16A4-AU | 16 KB + 4 KB | 1 KB | 2 KB | 32 | 1.6 - 3.6V | | |
| ATxmega128A4-MH | 128 KB + 8 KB | 2 KB | 8 KB | 32 | 1.6 - 3.6V | 44M1 | |
| ATxmega64A4-MH | 64 KB + 4 KB | 2 KB | 4 KB | 32 | 1.6 - 3.6V | | |
| ATxmega32A4-MH | 32 KB + 4 KB | 1 KB | 4 KB | 32 | 1.6 - 3.6V | | |
| ATxmega16A4-MH | 16 KB + 4 KB | 1 KB | 2 KB | 32 | 1.6 - 3.6V | | |
| ATxmega32A4-CU | 32 KB + 4K | 1 KB | 4 KB | 32 | 1.6 - 3.6V | 49C2 | |
| ATxmega16A4-CU | 16 KB + 4 KB | 1 KB | 2 KB | 32 | 1.6 - 3.6V | | |

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information see ”Packaging information” on page 58.

| Package Type | |
|---|---|
| **44A** | 44-Lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) |
| **44M1** | 44-Pad, 7x7x1 mm Body, Lead Pitch 0.50 mm, 5.20 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad No Lead Package (VQFN) |
| **49C2** | 49-Ball (7 x 7 Array), 0.65 mm Pitch, 5.0 x 5.0 x 1.0 mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA) |

concept enables instructions to be executed in every clock cycle. The program memory is In-System Re-programmable Flash memory.

## 6.3 Register File

The fast-access Register File contains 32 x 8-bit general purpose working registers with single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU cycle, the operation is performed on two Register File operands, and the result is stored back in the Register File.

Six of the 32 registers can be used as three 16-bit address register pointers for data space addressing - enabling efficient address calculations. One of these address pointers can also be used as an address pointer for look up tables in Flash program memory.

## 6.4 ALU - Arithmetic Logic Unit

The high performance Arithmetic Logic Unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed. After an arithmetic or logic operation, the Status Register is updated to reflect information about the result of the operation.

The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Both 8- and 16-bit arithmetic is supported, and the instruction set allows for efficient implementation of 32-bit arithmetic. The ALU also provides a powerful multiplier supporting both signed and unsigned multiplication and fractional format.

## 6.5 Program Flow

When the device is powered on, the CPU starts to execute instructions from the lowest address in the Flash Program Memory ‘0’. The Program Counter (PC) addresses the next instruction to be fetched. After a reset, the PC is set to location ‘0’.

Program flow is provided by conditional and unconditional jump and call instructions, capable of addressing the whole address space directly. Most AVR instructions use a 16-bit word format, while a limited number uses a 32-bit format.

During interrupts and subroutine calls, the return address PC is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. After reset the Stack Pointer (SP) points to the highest address in the internal SRAM. The SP is read/write accessible in the I/O memory space, enabling easy implementation of multiple stacks or stack areas. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR CPU.

# 8. DMAC - Direct Memory Access Controller

## 8.1 Features

- **Allows High-speed data transfer**
  - **From memory to peripheral**
  - **From memory to memory**
  - **From peripheral to memory**
  - **From peripheral to peripheral**
- **4 Channels**
- **From 1 byte and up to 16 M bytes transfers in a single transaction**
- **Multiple addressing modes for source and destination address**
  - **Increment**
  - **Decrement**
  - **Static**
- **1, 2, 4, or 8 bytes Burst Transfers**
- **Programmable priority between channels**

## 8.2 Overview

The XMEGA A4 has a Direct Memory Access (DMA) Controller to move data between memories and peripherals in the data space. The DMA controller uses the same data bus as the CPU to transfer data.

It has 4 channels that can be configured independently. Each DMA channel can perform data transfers in blocks of configurable size from 1 to 64K bytes. A repeat counter can be used to repeat each block transfer for single transactions up to 16M bytes. Each DMA channel can be configured to access the source and destination memory address with incrementing, decrementing or static addressing. The addressing is independent for source and destination address. When the transaction is complete the original source and destination address can automatically be reloaded to be ready for the next transaction.

The DMAC can access all the peripherals through their I/O memory registers, and the DMA may be used for automatic transfer of data to/from communication modules, as well as automatic data retrieval from ADC conversions, data transfer to DAC conversions, or data transfer to or from port pins. A wide range of transfer triggers is available from the peripherals, Event System and software. Each DMA channel has different transfer triggers.

To allow for continuous transfer, two channels can be interlinked so that the second takes over the transfer when the first is finished and vice versa.

The DMA controller can read from memory mapped EEPROM, but it cannot write to the EEPROM or access the Flash.

### 11.3.5 Extended Standby Mode

Extended Standby mode is identical to Power-save mode with the exception that all enabled system clock sources are kept running while the CPU and Peripheral clocks are stopped. This reduces the wake-up time when external crystals or resonators are used.

# 12. System Control and Reset

## 12.1 Features

- **Multiple reset sources for safe operation and device reset**
  - **Power-On Reset**
  - **External Reset**
  - **Watchdog Reset**
    - **The Watchdog Timer runs from separate, dedicated oscillator**
  - **Brown-Out Reset**
    - **Accurate, programmable Brown-Out levels**
  - **PDI reset**
  - **Software reset**
- **Asynchronous reset**
  - **No running clock in the device is required for reset**
- **Reset status register**

## 12.2 Resetting the AVR

During reset, all I/O registers are set to their initial values. The SRAM content is not reset. Application execution starts from the Reset Vector. The instruction placed at the Reset Vector should be an Absolute Jump (JMP) instruction to the reset handling routine. By default the Reset Vector address is the lowest Flash program memory address, ‘0’, but it is possible to move the Reset Vector to the first address in the Boot Section.

The I/O ports of the AVR are immediately tri-stated when a reset source goes active.

The reset functionality is asynchronous, so no running clock is required to reset the device.

After the device is reset, the reset source can be determined by the application by reading the Reset Status Register.

## 12.3 Reset Sources

### 12.3.1 Power-On Reset

The MCU is reset when the supply voltage VCC is below the Power-on Reset threshold voltage.

### 12.3.2 External Reset

The MCU is reset when a low level is present on the RESET pin.

### 12.3.3 Watchdog Reset

The MCU is reset when the Watchdog Timer period expires and the Watchdog Reset is enabled. The Watchdog Timer runs from a dedicated oscillator independent of the System Clock. For more details see ”WDT - Watchdog Timer” on page 24.

### 12.3.4 Brown-Out Reset

The MCU is reset when the supply voltage VCC is below the Brown-Out Reset threshold voltage and the Brown-out Detector is enabled. The Brown-out threshold voltage is programmable.

# 15. I/O Ports

## 15.1 Features

- **Selectable input and output configuration for each pin individually**
- **Flexible pin configuration through dedicated Pin Configuration Register**
- **Synchronous and/or asynchronous input sensing with port interrupts and events**
  - **Sense both edges**
  - **Sense rising edges**
  - **Sense falling edges**
  - **Sense low level**
- **Asynchronous wake-up from all input sensing configurations**
- **Two port interrupts with flexible pin masking**
- **Highly configurable output driver and pull settings:**
  - **Totem-pole**
  - **Pull-up/-down**
  - **Wired-AND**
  - **Wired-OR**
  - **Bus-keeper**
  - **Inverted I/O**
- **Optional Slew rate control**
- **Configuration of multiple pins in a single operation**
- **Read-Modify-Write (RMW) support**
- **Toggle/clear/set registers for Output and Direction registers**
- **Clock output on port pin**
- **Event Channel 0 output on port pin 7**
- **Mapping of port registers (virtual ports) into bit accessible I/O memory space**

## 15.2 Overview

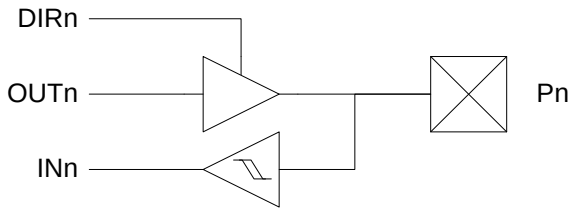
The XMEGA A4 devices have flexible General Purpose I/O Ports. A port consists of up to 8 pins, ranging from pin 0 to pin 7. The ports implement several functions, including synchronous/asynchronous input sensing, pin change interrupts and configurable output settings. All functions are individual per pin, but several pins may be configured in a single operation.

## 15.3 I/O configuration

All port pins (Pn) have programmable output configuration. In addition, all port pins have an inverted I/O function. For an input, this means inverting the signal between the port pin and the pin register. For an output, this means inverting the output signal between the port register and the port pin. The inverted I/O function can be used also when the pin is used for alternate functions.

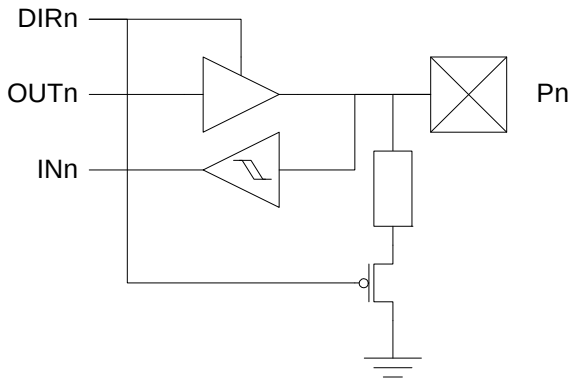
### 15.3.1 Push-pull

**Figure 15-1.** I/O configuration - Totem-pole



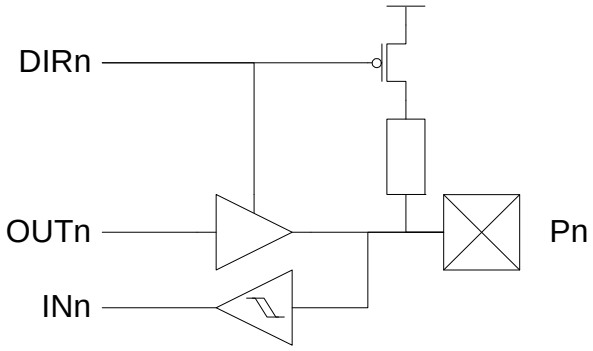

### 15.3.2 Pull-down

**Figure 15-2.** I/O configuration - Totem-pole with pull-down (on input)




### 15.3.3 Pull-up

**Figure 15-3.** I/O configuration - Totem-pole with pull-up (on input)




### 15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

# 24. Crypto Engine

## 24.1 Features

- **Data Encryption Standard (DES) CPU instruction**
- **Advanced Encryption Standard (AES) Crypto module**
- **DES Instruction**
  - **Encryption and Decryption**
  - **Single-cycle DES instruction**
  - **Encryption/Decryption in 16 clock cycles per 8-byte block**
- **AES Crypto Module**
  - **Encryption and Decryption**
  - **Support 128-bit keys**
  - **Support XOR data load mode to the State memory for Cipher Block Chaining**
  - **Encryption/Decryption in 375 clock cycles per 16-byte block**

## 24.2 Overview

The Advanced Encryption Standard (AES) and Data Encryption Standard (DES) are two commonly used encryption standards. These are supported through an AES peripheral module and a DES CPU instruction. All communication interfaces and the CPU can optionally use AES and DES encrypted communication and data storage.

DES is supported by a DES instruction in the AVR XMEGA CPU. The 8-byte key and 8-byte data blocks must be loaded into the Register file, and then DES must be executed 16 times to encrypt/decrypt the data block.

The AES Crypto Module encrypts and decrypts 128-bit data blocks with the use of a 128-bit key. The key and data must be loaded into the key and state memory in the module before encryption/decryption is started. It takes 375 peripheral clock cycles before the encryption/decryption is done and decrypted/encrypted data can be read out, and an optional interrupt can be generated. The AES Crypto Module also has DMA support with transfer triggers when encryption/decryption is done and optional auto-start of encryption/decryption when the state memory is fully loaded.

## 27.3 Input Selection

The Analog comparators have a very flexible input selection and the two comparators grouped in a pair may be used to realize a window function. One pair of analog comparators is shown in Figure 27-1 on page 45.

- **Input selection from pin**
  - **Pin 0, 1, 2, 3, 4, 5, 6 selectable to positive input of analog comparator**
  - **Pin 0, 1, 3, 5, 7 selectable to negative input of analog comparator**
- **Internal signals available on positive analog comparator inputs**
  - **Output from 12-bit DAC**
- **Internal signals available on negative analog comparator inputs**
  - **64-level scaler of the VCC, available on negative analog comparator input**
  - **Bandgap voltage reference**
  - **Output from 12-bit DAC**

## 27.4 Window Function

The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 27-2.

**Figure 27-2.** Analog comparator window function

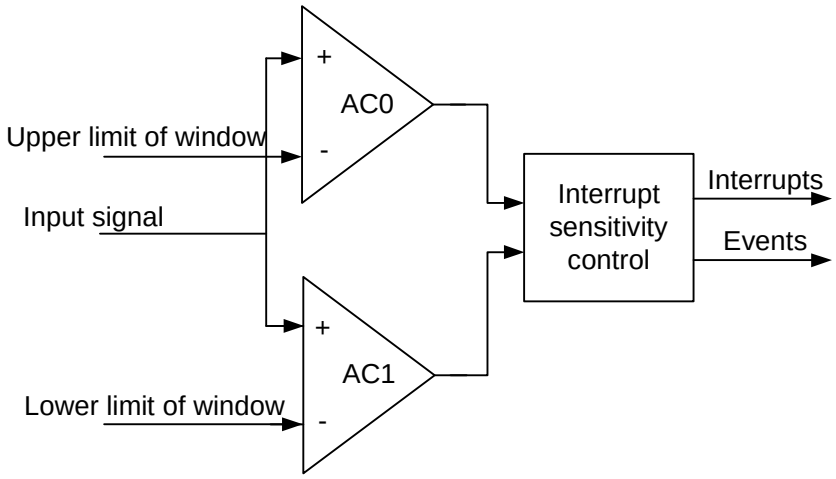


**Table 30-4.** Port D - Alternate functions

| PORTD | PIN # | INTERRUPT | TCD0 | TCD1 | USARTD0 | USARTD1 | SPID | CLOCKOUT | EVENTOUT |
|---|---|---|---|---|---|---|---|---|---|
| **GND** | 18 | | | | | | | | |
| **VCC** | 19 | | | | | | | | |
| **PD0** | 20 | SYNC | OC0A | | | | | | |
| **PD1** | 21 | SYNC | OC0B | | XCK0 | | | | |
| **PD2** | 22 | SYNC/ASYNC | OC0C | | RXD0 | | | | |
| **PD3** | 23 | SYNC | OC0D | | TXD0 | | | | |
| **PD4** | 24 | SYNC | | OC1A | | | $\overline{SS}$ | | |
| **PD5** | 25 | SYNC | | OC1B | | XCK1 | MOSI | | |
| **PD6** | 26 | SYNC | | | | RXD1 | MISO | | |
| **PD7** | 27 | SYNC | | | | TXD1 | SCK | CLKOUT | EVOUT |

**Table 30-5.** Port E - Alternate functions

| PORT E | PIN # | INTERRUPT | TCE0 | USARTE0 | TWIE |
|---|---|---|---|---|---|
| **PE0** | 28 | SYNC | OC0A | | SDA |
| **PE1** | 29 | SYNC | OC0B | XCK0 | SCL |
| **GND** | 30 | | | | |
| **VCC** | 31 | | | | |
| **PE2** | 32 | SYNC/ASYNC | OC0C | RXD0 | |
| **PE3** | 33 | SYNC | OC0D | TXD0 | |

**Table 30-6.** Port R - Alternate functions

| PORTR | PIN # | XTAL | PDI | TOSC |
|---|---|---|---|---|
| **PDI** | 34 | | PDI_DATA | |
| **$\overline{RESET}$** | 35 | | PDI_CLK | |
| **PR0** | 36 | XTAL2 | | TOSC2 |
| **PR1** | 37 | XTAL1 | | TOSC1 |

# 34. Electrical Characteristics

All typical values are measured at T = 25°C unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

## 34.1 Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on any Pin with respect to Ground | -0.5V to $V_{CC}$+0.5V |
| Maximum Operating Voltage | 3.6V |
| DC Current per I/O Pin | 20.0 mA |
| DC Current $V_{CC}$ and GND Pins | 200.0 mA |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 34.2 DC Characteristics

**Table 34-1.** Current Consumption

| Symbol | Parameter | Condition | | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current(1) | Active | 32 kHz, Ext. Clk | $V_{CC}$ = 1.8V | | 30 | | µA |
| | | | | $V_{CC}$ = 3.0V | | 75 | | |
| | | | 1 MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 260 | | |
| | | | | $V_{CC}$ = 3.0V | | 570 | | |
| | | | 2 MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 510 | 690 | |
| | | | | $V_{CC}$ = 3.0V | | 1.1 | 1.49 | mA |
| | | | 32 MHz, Ext. Clk | $V_{CC}$ = 3.0V | | 11.4 | 13 | |
| | | Idle | 32 kHz, Ext. Clk | $V_{CC}$ = 1.8V | | 2.8 | | µA |
| | | | | $V_{CC}$ = 3.0V | | 4.8 | | |
| | | | 1 MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 80 | | |
| | | | | $V_{CC}$ = 3.0V | | 150 | | |
| | | | 2 MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 160 | 225 | |
| | | | | $V_{CC}$ = 3.0V | | 295 | 390 | |
| | | | 32 MHz, Ext. Clk | $V_{CC}$ = 3.0V | | 4.8 | 6 | mA |
| | Power-down mode | All Functions Disabled, T = 25°C | | $V_{CC}$ = 3.0V | | 0.1 | 3 | µA |
| | | All Functions Disabled, T = 85°C | | $V_{CC}$ = 3.0V | | 1.5 | 5 | |
| | | ULP, WDT, Sampled BOD, T = 25°C | | $V_{CC}$ = 1.8V | | 1.1 | 6 | |
| | | | | $V_{CC}$ = 3.0V | | 1.1 | 6 | |
| | | ULP, WDT, Sampled BOD, T= 85°C | | $V_{CC}$ = 3.0V | | 2.6 | 10 | |

**Table 34-1.** Current Consumption (Continued)

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Power-save mode | RTC 1 kHz from Low Power 32 kHz TOSC, T = 25°C | $V_{CC}$ = 1.8V | | 0.5 | 4 | µA |
| | | | $V_{CC}$ = 3.0V | | 0.7 | 4 | |
| | | RTC from Low Power 32 kHz TOSC | $V_{CC}$ = 3.0V | | 1.16 | | |
| | Reset Current Consumption | without Reset pull-up resistor current | $V_{CC}$ = 3.0V | | 505 | | |
| **Module current consumption**(2) | | | | | | | |
| $I_{CC}$ | RC32M | | | | 470 | | µA |
| | RC32M w/DFLL | Internal 32.768 kHz oscillator as DFLL source | | | 600 | | |
| | RC2M | | | | 112 | | |
| | RC2M w/DFLL | Internal 32.768 kHz oscillator as DFLL source | | | 145 | | |
| | RC32K | | | | 30 | | |
| | PLL | Multiplication factor = 10x | | | 225 | | |
| | Watchdog normal mode | | | | 0.9 | | |
| | BOD Continuous mode | | | | 120 | | |
| | BOD Sampled mode | | | | 1 | | |
| | Internal 1.00 V ref | | | | 80 | | |
| | Temperature reference | | | | 80 | | |
| | RTC with int. 32 kHz RC as source | No prescaling | | | 30 | | |
| | RTC with ULP as source | No prescaling | | | 0.9 | | |
| | ADC | 250 kS/s - Int. 1V Ref | | | 2.9 | | mA |
| | DAC Normal Mode | Single channel, Int. 1V Ref | | | 2.4 | | |
| | DAC Low-Power Mode | Single channel, Int. 1V Ref | | | 1.1 | | |
| | AC High-speed | | | | 280 | | µA |
| | AC Low-power | | | | 110 | | |
| | USART | Rx and Tx enabled, 9600 BAUD | | | 5.3 | | |
| | DMA | | | | 95 | | |
| | Timer/Counter | Prescaler DIV1 | | | 19 | | |
| | AES | | | | 140 | | |
| | Flash/EEPROM Programming | Vcc = 2V | | | 13 | | mA |
| | | Vcc = 3V | | | 18 | | |

Note: 1. All Power Reduction Registers set.

2. All parameters measured as the difference in current consumption between module enabled and disabled. All data at $V_{CC}$ = 3.0V, $Clk_{SYS}$ = 1 MHz External clock with no prescaling.

## 34.4 Flash and EEPROM Memory Characteristics

**Table 34-3.** Endurance and Data Retention

| Symbol | Parameter | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| | Flash | Write/Erase cycles | 25°C | 10K | | | Cycle |
| | | | 85°C | 10K | | | |
| | | Data retention | 25°C | 100 | | | Year |
| | | | 55°C | 25 | | | |
| | EEPROM | Write/Erase cycles | 25°C | 80K | | | Cycle |
| | | | 85°C | 30K | | | |
| | | Data retention | 25°C | 100 | | | Year |
| | | | 55°C | 25 | | | |

**Table 34-4.** Programming time

| Symbol | Parameter | Condition | Min | Typ(1) | Max | Units |
|---|---|---|---|---|---|---|
| | Chip Erase | Flash, EEPROM(2) and SRAM Erase | | 40 | | ms |
| | Flash | Page Erase | | 6 | | |
| | | Page Write | | 6 | | |
| | | Page WriteAutomatic Page Erase and Write | | 12 | | |
| | EEPROM | Page Erase | | 6 | | |
| | | Page Write | | 6 | | |
| | | Page WriteAutomatic Page Erase and Write | | 12 | | |

Notes: 1. Programming is timed from the internal 2 MHz oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

## 34.5 ADC Characteristics

**Table 34-5.** ADC Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| RES | Resolution | Programmable: 8/12 | 8 | 12 | 12 | Bits |
| INL | Integral Non-Linearity | 500 ksps | -5 | ±2 | 5 | LSB |
| DNL | Differential Non-Linearity | 500 ksps | | < ±1 | | |
| | Gain Error | | | < ±10 | | mV |
| | Offset Error | | | < ±2 | | |
| $ADC_{clk}$ | ADC Clock frequency | Max is 1/4 of Peripheral Clock | | | 2000 | kHz |
| | Conversion rate | | | | 2000 | ksps |
| | Conversion time (propagation delay) | (RES+2)/2+GAIN<br>RES = 8 or 12, GAIN = 0 or 1 | 5 | 7 | 8 | $ADC_{clk}$ cycles |
| | Sampling Time | 1/2 $ADC_{clk}$ cycle | 0.25 | | | uS |
| | Conversion range | | 0 | | VREF | V |
| AVCC | Analog Supply Voltage | | $V_{cc}$-0.3 | | $V_{cc}$+0.3 | |
| VREF | Reference voltage | | 1.0 | | $V_{cc}$-0.6V | |
| | Input bandwidth | | | | | kHz |
| INT1V | Internal 1.00V reference(1) | | | 1.00 | | V |
| INTVCC | Internal $V_{CC}$/1.6 | | | $V_{CC}$/1.6 | | |
| SCALEDVCC | Scaled internal $V_{CC}$/10 input | | | $V_{CC}$/10 | | |
| $R_{AREF}$ | Reference input resistance | | | > 10 | | MΩ |
| | Start-up time | | | 12 | 24 | $ADC_{clk}$ cycles |
| | Internal input sampling speed | Temp. sensor, $V_{CC}$/10, Bandgap | | | 100 | ksps |

Note: 1. Refer to ”Bandgap Characteristics” on page 66 for more parameter details.

**Table 34-6.** ADC Gain Stage Characteristics

| Symbol | Parameter | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| | Gain error | 1 to 64 gain | | | < ±1 | | % |
| | Offset error | | | | < ±1 | | mV |
| Vrms | Noise level at input | 64x gain | VREF = Int. 1V | | 0.12 | | |
| | | | VREF = Ext. 2V | | 0.06 | | |
| | Clock rate | Same as ADC | | | | 1000 | kHz |

## 35.3 Power-down Supply Current

**Figure 35-15.** Power-down Supply Current vs. Temperature

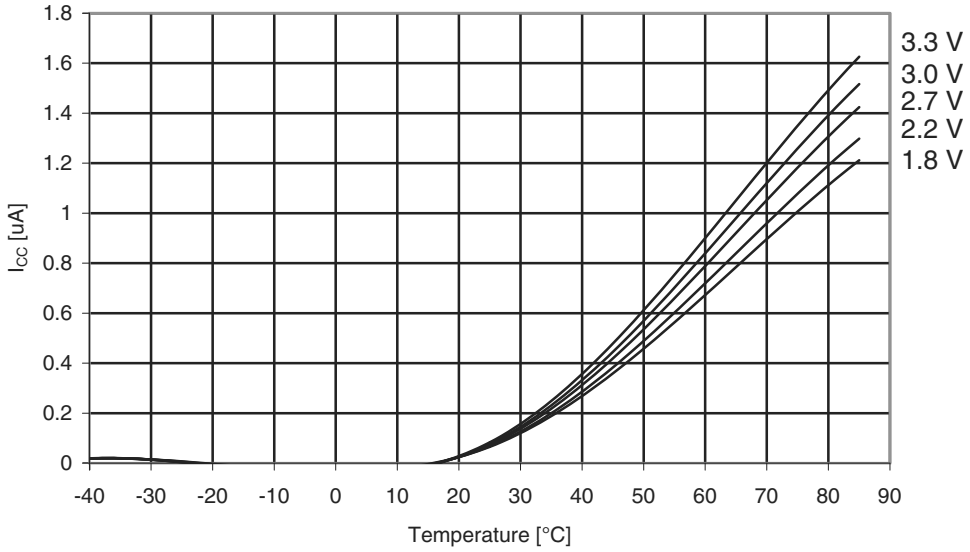



**Figure 35-16.** Power-down Supply Current vs. Temperature

*With WDT and sampled BOD enabled.*

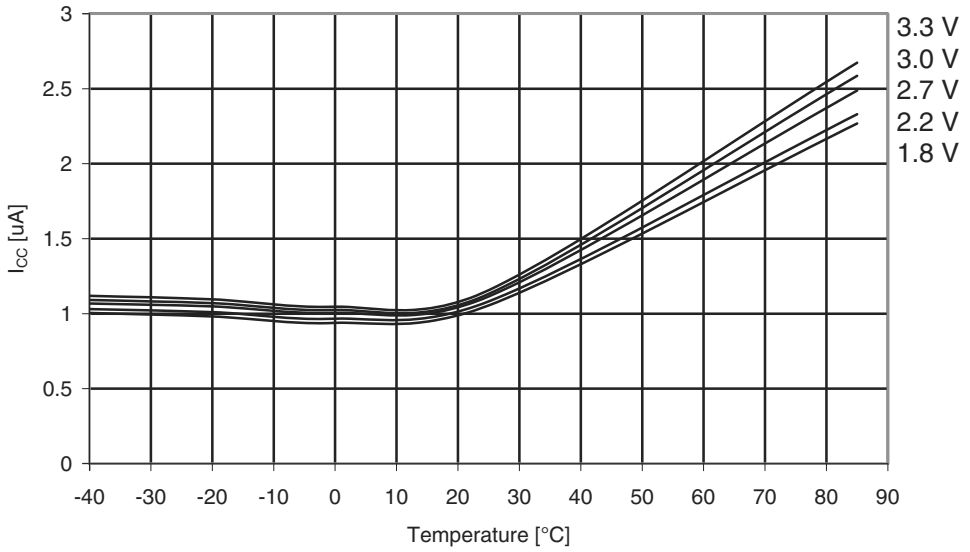


**Figure 35-23.** I/O Pin Output Voltage vs. Source Current

*Vcc = 3.3V.*

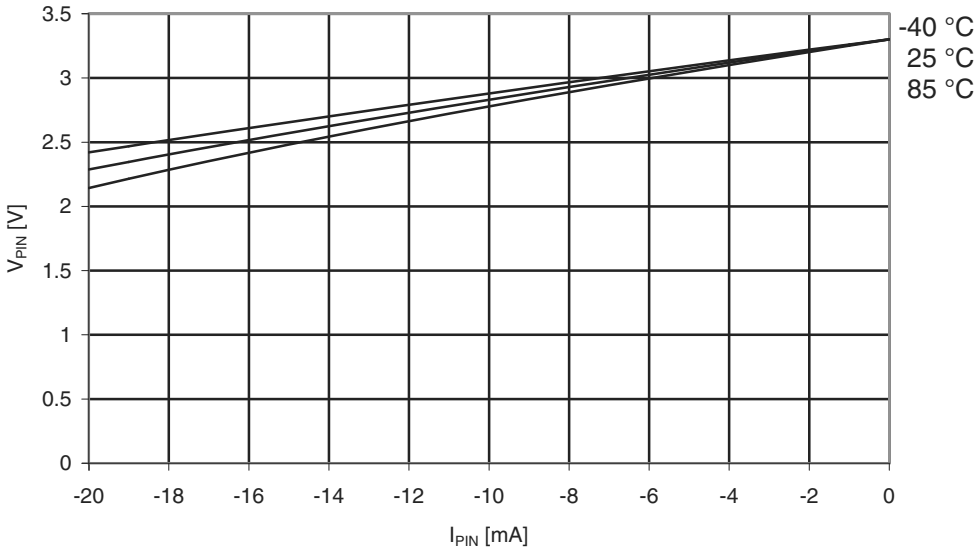
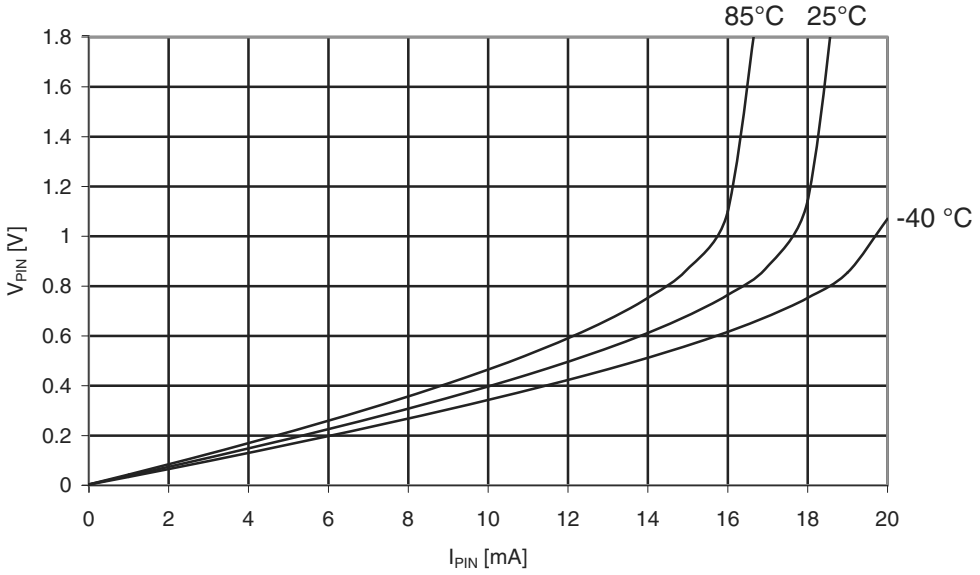



**Figure 35-24.** I/O Pin Output Voltage vs. Sink Current

*Vcc = 1.8V.*



## 35.7 Pin Thresholds and Hysteresis

**Figure 35-27.** I/O Pin Input Threshold Voltage vs. $V_{CC}$

*$V_{IH}$ - I/O Pin Read as "1".*

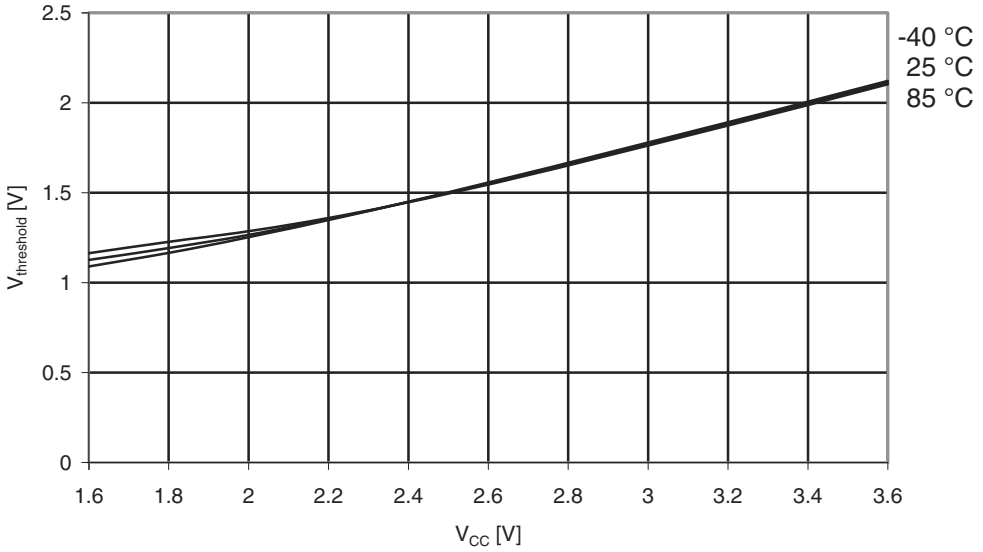



**Figure 35-28.** I/O Pin Input Threshold Voltage vs. $V_{CC}$

*$V_{IL}$ - I/O Pin Read as "0".*

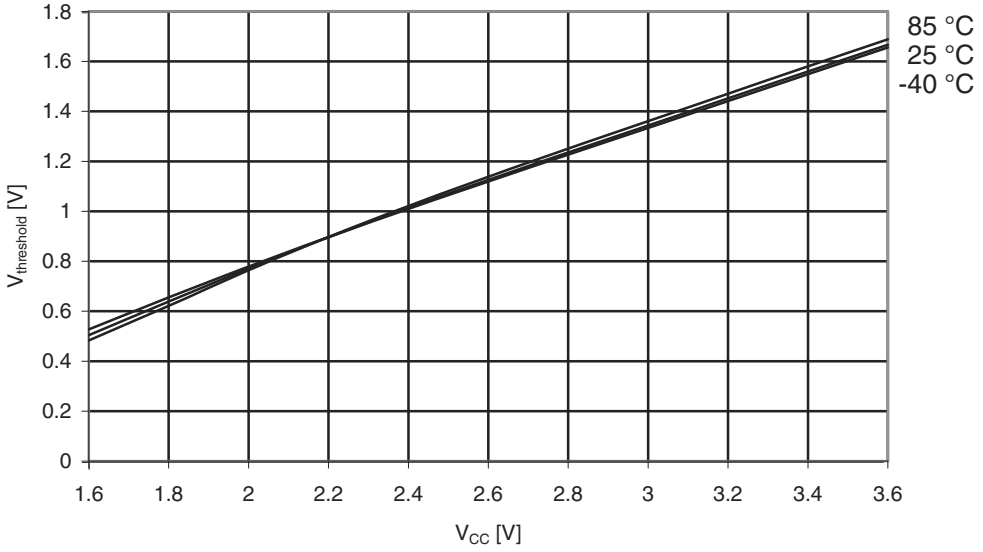
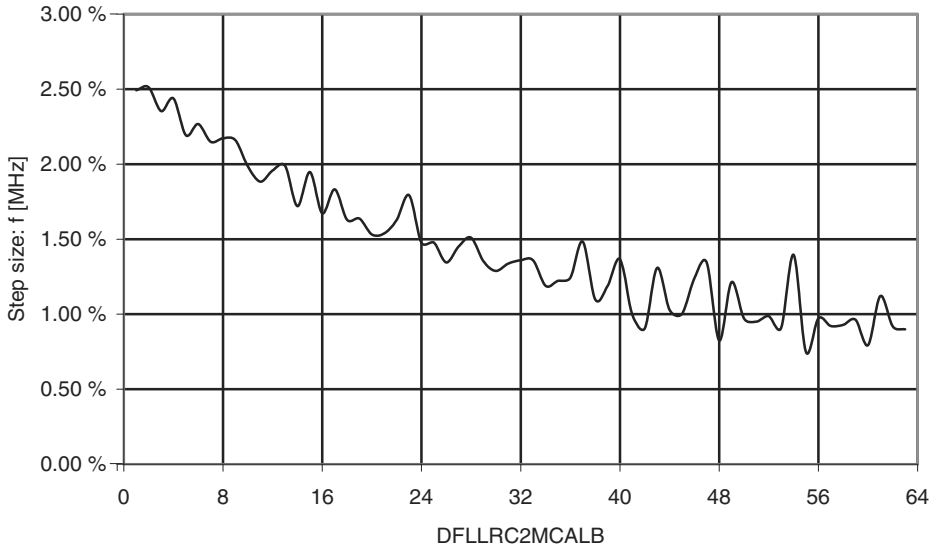


**Figure 35-39.** Internal 2 MHz Oscillator CALB Calibration Step Size

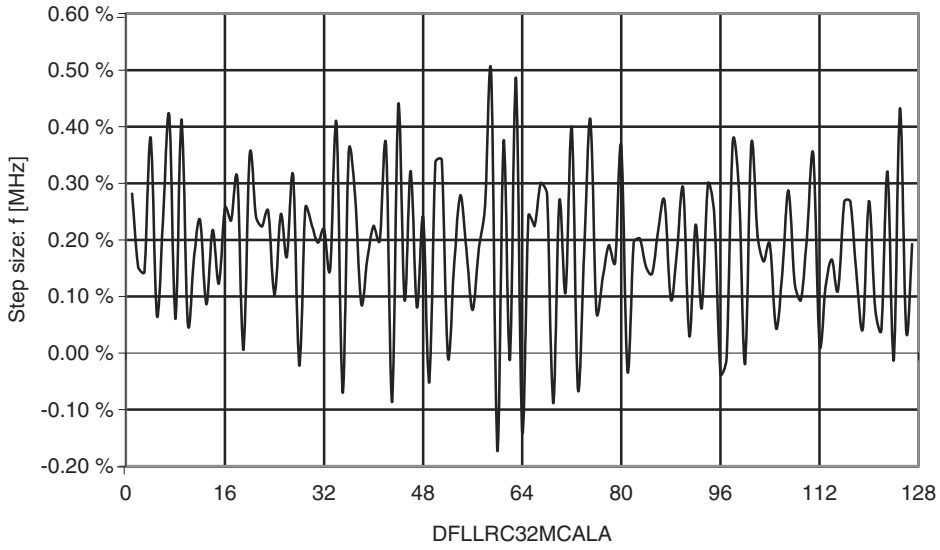
*T = -40 to 85°C, $V_{CC}$ = 3V.*




### 35.10.3 Internal 32 MHZ Oscillator

**Figure 35-40.** Internal 32 MHz Oscillator CALA Calibration Step Size

*T = -40 to 85°C, $V_{CC}$ = 3V.*



# 37. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revisions in this section are referring to the document revision.

## 37.1 8069R – 06/13

1. Not recommended for new designs - Use XMEGA A4U series.

## 37.2 8069Q – 12/10

1. Datasheet status changed to complete: Preliminary removed from the front page.
2. Updated all tables in the “Electrical Characteristics” .
3. Updated ”Packaging information” on page 58.
4. Replaced Table 34-11 on page 67.
5. Replaced Table 34-18 on page 69 and added the figure ”TOSC input capacitance” on page 69.
7. ERRATA A combined with ERRATA B to ERRATA “rev. A/B” .
8. Updated ERRATA for ADC (ADC has increased INL error for some operating conditions).
9. Updated the last page by Atmel new Brand Style Guide.

## 37.3 8069P – 09/10

1. Updated ”Errata” on page 93.

## 37.4 8069O – 08/10

1. Updated the Footnote 3 of ”Ordering Information” on page 2.
2. Updated ”Features” on page 27. Event Channel 0 output on port pin 7.
3. Updated ”DC Characteristics” on page 61 by adding Icc for Flash/EEPROM Programming.
4. Added AVCC in ”ADC Characteristics” on page 65.
5. Updated Start up time in ”ADC Characteristics” on page 65.
6. Updated ”DAC Characteristics” on page 66. Removed DC output impedence.
7. Updated and fixed typo in “Errata” section.