Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16a4-mhr

3. Overview

The Atmel® AVR® XMEGA™A4 is a family of low power, high performance and peripheral rich CMOS 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the XMEGA A4 achieves throughputs approaching 1 Million Instructions Per Second (MIPS) per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The XMEGA A4 devices provide the following features: In-System Programmable Flash with Read-While-Write capabilities, Internal EEPROM and SRAM, four-channel DMA Controller, eight-channel Event System, Programmable Multi-level Interrupt Controller, 34 general purpose I/O lines, 16-bit Real Time Counter (RTC), five flexible 16-bit Timer/Counters with compare modes and PWM, five USARTs, two Two Wire Serial Interfaces (TWIs), two Serial Peripheral Interfaces (SPIs), AES and DES crypto engine, one Twelve-channel, 12-bit ADC with optional differential input with programmable gain, one Two-channel 12-bit DAC, two analog comparators with window mode, programmable Watchdog Timer with separate Internal Oscillator, accurate internal oscillators with PLL and prescaler and programmable Brown-Out Detection.

The Program and Debug Interface (PDI), a fast 2-pin interface for programming and debugging, is available.

The XMEGA A4 devices have five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, DMA Controller, Event System, Interrupt Controller and all peripherals to continue functioning. The Power-down mode saves the SRAM and register contents but stops the oscillators, disabling all other functions until the next TWI or pin-change interrupt, or Reset. In Power-save mode, the asynchronous Real Time Counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In Standby mode, the Crystal/Resonator Oscillator is kept running while the rest of the device is sleeping. This allows very fast start-up from external crystal combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in Active mode and in Idle sleep mode.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The program Flash memory can be reprogrammed in-system through the PDI. A Bootloader running in the device can use any interface to download the application program to the Flash memory. The Bootloader software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8/16-bit RISC CPU with In-System Self-Programmable Flash, the Atmel XMEGA A4 is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

The XMEGA A4 devices are supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

**Not recommended for new designs -
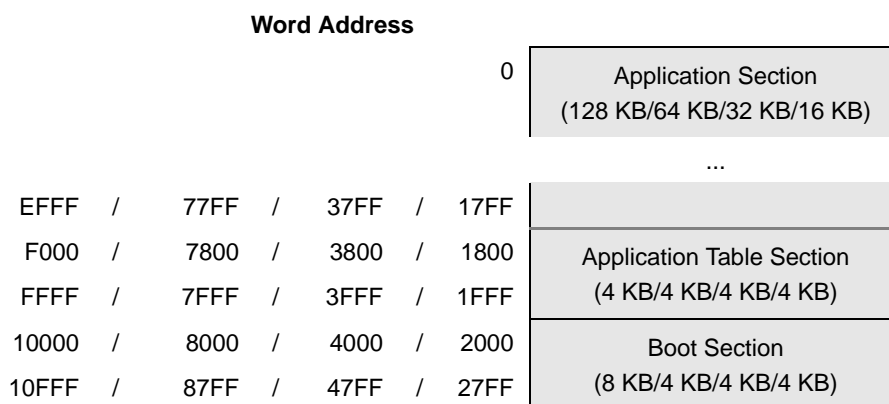Use XMEGA A4U series**

7.3 In-System Programmable Flash Program Memory

The XMEGA A4 devices contain On-chip In-System Programmable Flash memory for program storage, see Figure 7-1 on page 11. Since all AVR instructions are 16- or 32-bits wide, each Flash address location is 16 bits.

The Program Flash memory space is divided into Application and Boot sections. Both sections have dedicated Lock Bits for setting restrictions on write or read/write operations. The Store Program Memory (SPM) instruction must reside in the Boot Section when used to write to the Flash memory.

A third section inside the Application section is referred to as the Application Table section which has separate Lock bits for storage of write or read/write protection. The Application Table section can be used for storing non-volatile data or application software.

Figure 7-1. Flash Program Memory (Hexadecimal address)

Word Address

							0	Application Section (128 KB/64 KB/32 KB/16 KB)
								...
EFFF	/	77FF	/	37FF	/	17FF		
F000	/	7800	/	3800	/	1800		Application Table Section (4 KB/4 KB/4 KB/4 KB)
FFFF	/	7FFF	/	3FFF	/	1FFF		
10000	/	8000	/	4000	/	2000		Boot Section (8 KB/4 KB/4 KB/4 KB)
10FFF	/	87FF	/	47FF	/	27FF		

The Application Table Section and Boot Section can also be used for general application software.

9. Event System

9.1 Features

- **Inter-peripheral communication and signalling with minimum latency**
- **CPU and DMA independent operation**
- **8 Event Channels allow for up to 8 signals to be routed at the same time**
- **Events can be generated by**
    - **TImer/Counters (TCxn)**
    - **Real Time Counter (RTC)**
    - **Analog to Digital Converters (ADCx)**
    - **Analog Comparators (ACx)**
    - **Ports (PORTx)**
    - **System Clock (Clk$_{SYS}$)**
    - **Software (CPU)**
- **Events can be used by**
    - **TImer/Counters (TCxn)**
    - **Analog to Digital Converters (ADCx)**
    - **Digital to Analog Converters (DACx)**
    - **Ports (PORTx)**
    - **DMA Controller (DMAC)**
    - **IR Communication Module (IRCOM)**
- **The same event can be used by multiple peripherals for synchronized timing**
- **Advanced Features**
    - **Manual Event Generation from software (CPU)**
    - **Quadrature Decoding**
    - **Digital Filtering**
- **Functions in Active and Idle mode**

9.2 Overview

The Event System is a set of features for inter-peripheral communication. It enables the possibility for a change of state in one peripheral to automatically trigger actions in one or more peripherals. Whose changes in a peripheral that will trigger actions in other peripherals are configurable by software. It is a simple, but powerful system as it allows for autonomous control of peripherals without any use of interrupts, CPU or DMA resources.

The indication of a change in a peripheral is referred to as an event, and is usually the same as the interrupt conditions for that peripheral. Events are passed between peripherals using a dedicated routing network called the Event Routing Network. Figure 9-1 on page 17 shows a basic block diagram of the Event System with the Event Routing Network and the peripherals to which it is connected. This highly flexible system can be used for simple routing of signals, pin functions or for sequencing of events.

The maximum latency is two CPU clock cycles from when an event is generated in one peripheral, until the actions are triggered in one or more other peripherals.

The Event System is functional in both Active and Idle modes.

10. System Clock and Clock options

10.1 Features

- **Fast start-up time**
- **Safe run-time clock switching**
- **Internal Oscillators:**
  - **32 MHz run-time calibrated RC oscillator**
  - **2 MHz run-time calibrated RC oscillator**
  - **32.768 kHz calibrated RC oscillator**
  - **32 kHz Ultra Low Power (ULP) oscillator with 1 kHz ouput**
- **External clock options**
  - **0.4 - 16 MHz Crystal Oscillator**
  - **32 kHz Crystal Oscillator**
  - **External clock**
- **PLL with internal and external clock options with 1 to 31x multiplication**
- **Clock Prescalers with 1 to 2048x division**
- **Fast peripheral clock running at 2 and 4 times the CPU clock speed**
- **Automatic Run-Time Calibration of internal oscillators**
- **Crystal Oscillator failure detection**

10.2 Overview

XMEGA A4 has an advanced clock system, supporting a large number of clock sources. It incorporates both integrated oscillators, external crystal oscillators and resonators. A high frequency Phase Locked Loop (PLL) and clock prescalers can be controlled from software to generate a wide range of clock frequencies from the clock source input.

It is possible to switch between clock sources from software during run-time. After reset the device will always start up running from the 2 Mhz internal oscillator.

A calibration feature is available, and can be used for automatic run-time calibration of the internal 2 MHz and 32 MHz oscillators. This reduce frequency drift over voltage and temperature.

A Crystal Oscillator Failure Monitor can be enabled to issue a Non-Maskable Interrupt and switch to internal oscillator if the external oscillator fails. Figure 10-1 on page 19 shows the principal clock system in XMEGA A4.

10.3.3   32.768 kHz Crystal Oscillator

The 32.768 kHz Crystal Oscillator is a low power driver for an external watch crystal. It can be used as system clock source or as asynchronous clock source for the Real Time Counter.

10.3.4   0.4 - 16 MHz Crystal Oscillator

The 0.4 - 16 MHz Crystal Oscillator is a driver intended for driving both external resonators and crystals ranging from 400 kHz to 16 MHz.

10.3.5   2 MHz Run-time Calibrated Internal Oscillator

The 2 MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator. It is calibrated during production to provide a default frequency which is close to its nominal frequency. The oscillator can use the 32 kHz Calibrated Internal Oscillator or the 32 kHz Crystal Oscillator as a source for calibrating the frequency run-time to compensate for temperature and voltage drift hereby optimizing the accuracy of the oscillator.

10.3.6   32 MHz Run-time Calibrated Internal Oscillator

The 32 MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator. It is calibrated during production to provide a default frequency which is close to its nominal frequency. The oscillator can use the 32 kHz Calibrated Internal Oscillator or the 32 kHz Crystal Oscillator as a source for calibrating the frequency run-time to compensate for temperature and voltage drift hereby optimizing the accuracy of the oscillator.

10.3.7   External Clock input

The external clock input gives the possibility to connect a clock from an external source.

10.3.8   PLL with Multiplication factor 1 - 31x

The PLL provides the possibility of multiplying a frequency by any number from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

11.3.5 Extended Standby Mode

Extended Standby mode is identical to Power-save mode with the exception that all enabled system clock sources are kept running while the CPU and Peripheral clocks are stopped. This reduces the wake-up time when external crystals or resonators are used.

18. Hi-Res - High Resolution Extension

18.1 Features

- **Increases Waveform Generator resolution by 2-bits (4x)**
- **Supports Frequency, single- and dual-slope PWM operation**
- **Supports the AWEX when this is enabled and used for the same Timer/Counter**

18.2 Overview

The Hi-Resolution (Hi-Res) Extension is able to increase the resolution of the waveform generation output by a factor of 4. When enabled for a Timer/Counter, the Fast Peripheral clock running at four times the CPU clock speed will be as input to the Timer/Counter.

The High Resolution Extension can also be used when an AWEX is enabled and used with a Timer/Counter.

XMEGA A4 devices have three Hi-Res Extensions that each can be enabled for each Timer/Counters pair on PORTC, PORTD and PORTE. The notation of these are HIRESC, HIRESD and HIRESE, respectively.

21. SPI - Serial Peripheral Interface

21.1 Features

- **Two Identical SPI peripherals**
- **Full-duplex, Three-wire Synchronous Data Transfer**
- **Master or Slave Operation**
- **LSB First or MSB First Data Transfer**
- **Seven Programmable Bit Rates**
- **End of Transmission Interrupt Flag**
- **Write Collision Flag Protection**
- **Wake-up from Idle Mode**
- **Double Speed (CK/2) Master SPI Mode**

21.2 Overview

The Serial Peripheral Interface (SPI) allows high-speed full-duplex, synchronous data transfer between different devices. Devices can communicate using a master-slave scheme, and data is transferred both to and from the devices simultaneously.

PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID, respectively.

27. AC - Analog Comparator

27.1 Features

- **Two Analog Comparators**
- **Selectable Power vs. Speed**
- **Selectable hysteresis**
  - **0, 20 mV, 50 mV**
- **Analog Comparator output available on pin**
- **Flexible Input Selection**
  - **All pins on the port**
  - **Output from the DAC**
  - **Bandgap reference voltage.**
  - **Voltage scaler that can perform a 64-level scaling of the internal VCC voltage.**
- **Interrupt and event generation on**
  - **Rising edge**
  - **Falling edge**
  - **Toggle**
- **Window function interrupt and event generation on**
  - **Signal above window**
  - **Signal inside window**
  - **Signal below window**

27.2 Overview

XMEGA A4 features two Analog Comparators (AC). An Analog Comparator compares two voltages, and the output indicates which input is largest. The Analog Comparator may be configured to give interrupt requests and/or events upon several different combinations of input change.

Both hysteresis and propagation delays may be adjusted in order to find the optimal operation for each application.

A wide range of input selection is available, both external pins and several internal signals can be used.

The Analog Comparators are always grouped in pairs (AC0 and AC1) on each analog port. They have identical behavior but separate control registers.

Optionally, the state of the comparator is directly available on a pin.

PORTA has one AC pair. Notation of this peripheral is ACA.

27.3 Input Selection

The Analog comparators have a very flexible input selection and the two comparators grouped in a pair may be used to realize a window function. One pair of analog comparators is shown in Figure 27-1 on page 45.

- **Input selection from pin**
  - **Pin 0, 1, 2, 3, 4, 5, 6 selectable to positive input of analog comparator**
  - **Pin 0, 1, 3, 5, 7 selectable to negative input of analog comparator**
- **Internal signals available on positive analog comparator inputs**
  - **Output from 12-bit DAC**
- **Internal signals available on negative analog comparator inputs**
  - **64-level scaler of the VCC, available on negative analog comparator input**
  - **Bandgap voltage reference**
  - **Output from 12-bit DAC**

27.4 Window Function

The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 27-2.

Figure 27-2. Analog comparator window function

Not recommended for new designs - Use XMEGA A4U series
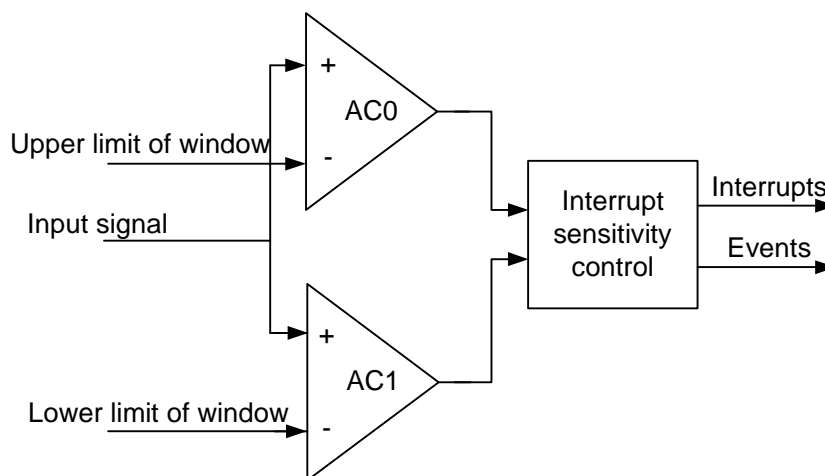
30.1.5   Communication functions

|	
SCL	Serial Clock for TWI
SDA	Serial Data for TWI
XCKn	Transfer Clock for USART n
RXDn	Receiver Data for USART n
TXDn	Transmitter Data for USART n
$\overline{SS}$	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI

30.1.6   Oscillators, Clock and Event

TOSCn	Timer Oscillator pin n
XTALn	Input/Output for inverting Oscillator pin n

30.1.7   Debug/System functions

$\overline{RESET}$	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin

33.3   49C2
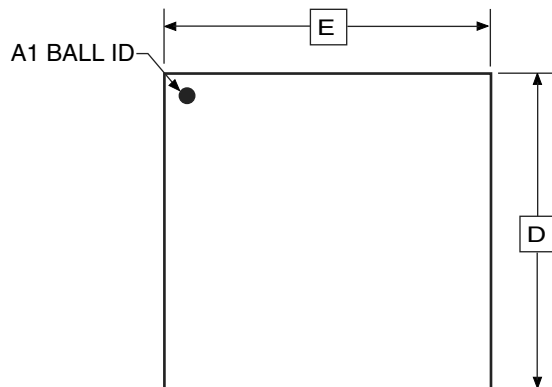
TOP VIEW

SIDE VIEW

BOTTOM VIEW

A1 BALL ID

A1 BALL CORNER

49 - Ø0.35 ±0.05

0.10
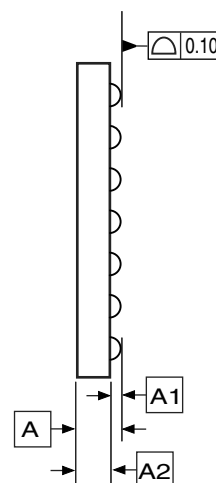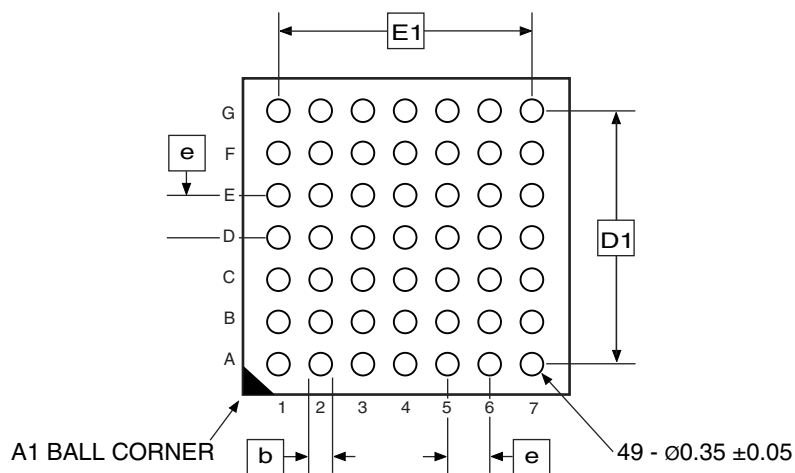
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.00	
A1	0.20	–	–	
A2	0.65	–	–	
D	4.90	5.00	5.10	
D1	3.90 BSC			
E	4.90	5.00	5.10	
E1	3.90 BSC			
b	0.30	0.35	0.40	
e	0.65 BSC			

3/14/08

| Package Drawing Contact: packagedrawings@atmel.com	**TITLE** **49C2,** 49-ball (7 x 7 array), 0.65mm pitch, 5.0 x 5.0 x 1.0mm, very thin, fine-pitch ball grid array package (VFBGA)	**GPC** CBD	**DRAWING NO.** 49C2	**REV.** A

**Not recommended for new designs -
Use XMEGA A4U series**

34.3 Speed

Table 34-2. Operating voltage and frequency

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clk_{CPU}	CPU clock frequency	$V_{CC} = 1.6V$	0		12	MHz
		$V_{CC} = 1.8V$	0		12	
		$V_{CC} = 2.7V$	0		32	
		$V_{CC} = 3.6V$	0		32	

The maximum CPU clock frequency of the XMEGA A4 devices is depending on V_{CC}. As shown in Figure 34-1 on page 63 the Frequency vs. V_{CC} curve is linear between $1.8V < V_{CC} < 2.7V$.

Figure 34-1. Operating Frequency vs.Vcc
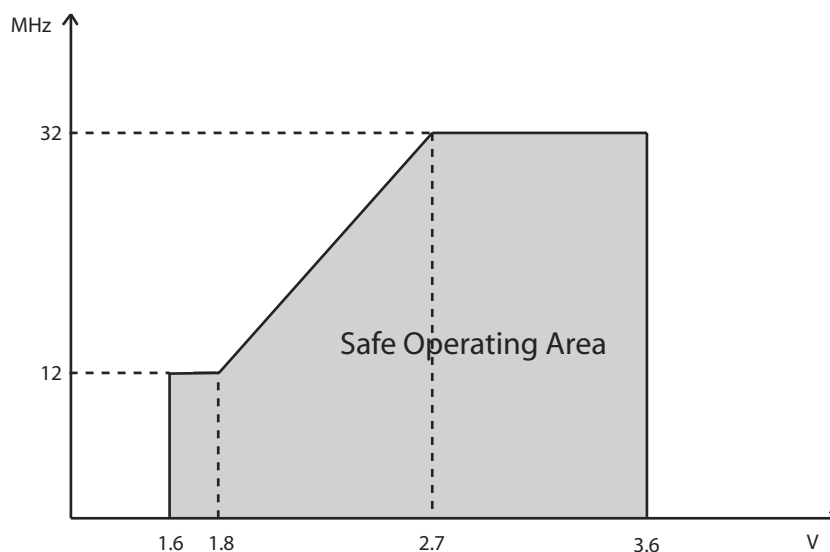
34.11 POR Characteristics

Table 34-12. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{POT-}	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	0.8		
		V_{CC} falls at 1V/ms or slower	0.8	1.3		V
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

34.12 Reset Characteristics

Table 34-13. Reset Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Minimum reset pulse width			90		ns
	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.45*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.42*V_{CC}		

34.13 Oscillator Characteristics

Table 34-14. Internal 32.768 kHz Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Accuracy	T = 85°C, V_{CC} = 3V, After production calibration	-0.5		0.5	%

Table 34-15. Internal 2 MHz Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Accuracy	T = 85°C, V_{CC} = 3V, After production calibration	-1.5		1.5	%
	DFLL Calibration step size	T = 25°C, V_{CC} = 3V		0.15		

Table 34-16. Internal 32 MHz Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Accuracy	T = 85°C, V_{CC} = 3V, After production calibration	-1.5		1.5	%
	DFLL Calibration stepsize	T = 25°C, V_{CC} = 3V		0.2		

Table 34-17. Internal 32 kHz, ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Output frequency 32 kHz ULP OSC	T = 85°C, V_{CC} = 3.0V		26		kHz

Not recommended for new designs - Use XMEGA A4U series

Figure 35-13. Idle Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC prescaled to 8 MHz.
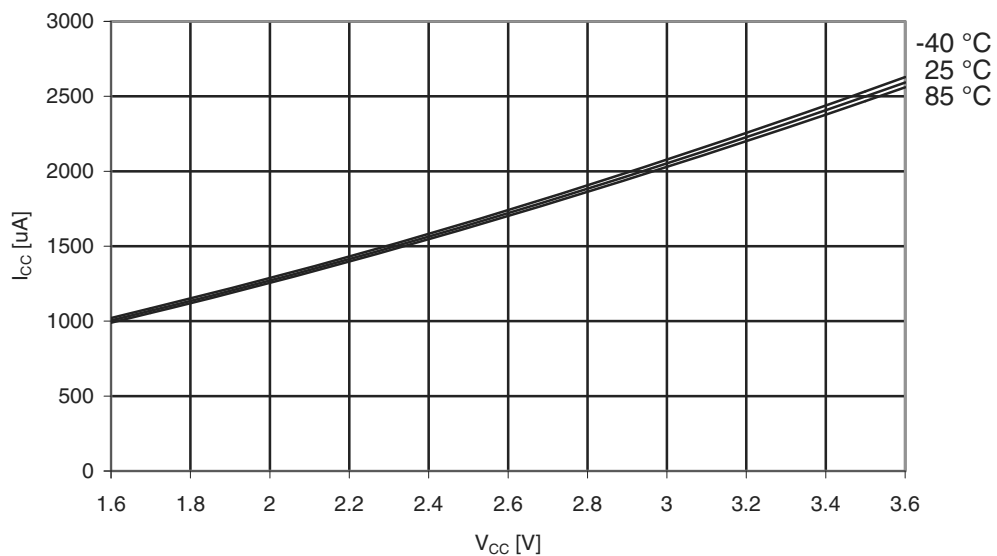
Figure 35-14. Idle Supply Current vs. Vcc
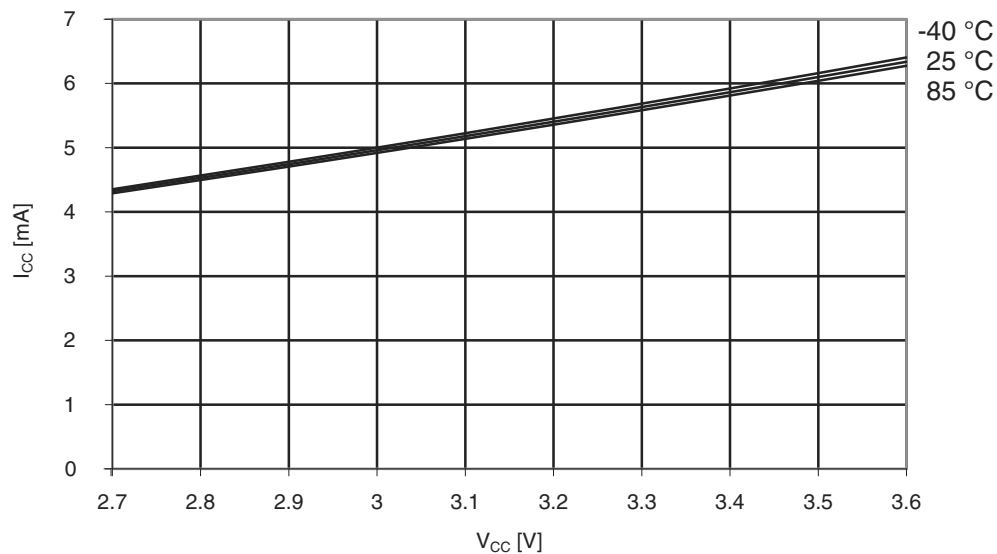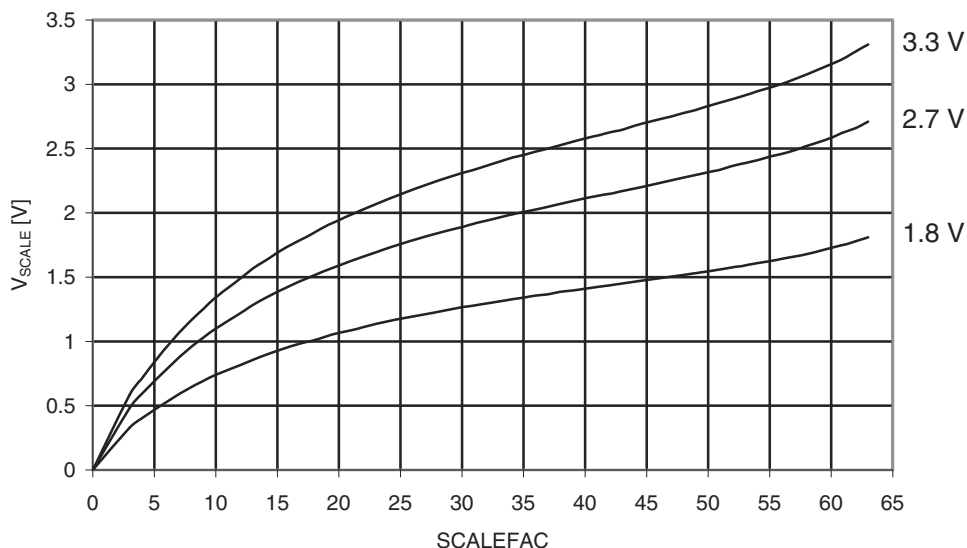
f_{SYS} = 32 MHz internal RC.

Not recommended for new designs - Use XMEGA A4U series

Figure 36-1. Analog Comparator Voltage Scaler vs. Scalefac
T = 25°C

Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. **ADC has increased INL error for some operating conditions**

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

– 6LSB for sample rates above 1Msps, and up to 8 LSB for 2Msps sample rate.

– 6LSB for reference voltage below 1.1V when VCC is above 3.0V.

– 20LSB for ambient temperature below 0 degree C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

4. **ADC gain stage output range is limited to 2.4 V**

The amplified output of the ADC gain stage will never go above 2.4 V, hence the differential input will only give correct output when below 2.4 V/gain. For the available gain settings, this gives a differential input range of:

– 1x gain: 2.4 V
– 2x gain: 1.2 V
– 4x gain: 0.6 V
– 8x gain: 300 mV
– 16x gain: 150 mV
– 32x gain: 75 mV
– 64x gain: 38 mV

Problem fix/Workaround

Keep the amplified voltage output from the ADC gain stage below 2.4 V in order to get a correct result, or keep ADC voltage reference below 2.4 V.

5. **ADC Event on compare match non-functional**

ADC signalling event will be given at every conversion complete even if Interrupt mode (INTMODE) is set to BELOW or ABOVE.

Problem fix/Workaround

Enable and use interrupt on compare match when using the compare function.

6. **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**

The ADC can not be used to do bandgap measurements when VCC is below 2.7V.

Problem fix/Workaround

None.

7. **Accuracy lost on first three samples after switching input to ADC gain stage**

Due to memory effect in the ADC gain stage, the first three samples after changing input channel must be disregarded to achieve 12-bit accuracy.

Problem fix/Workaround

Run three ADC conversions and discard these results after changing input channels to ADC gain stage.

8. **Configuration of PGM and CWCM not as described in XMEGA A Manual**

Enabling Common Waveform Channel Mode will enable Pattern generation mode (PGM), but not Common Waveform Channel Mode.

Enabling Pattern Generation Mode (PGM) and not Common Waveform Channel Mode (CWCM) will enable both Pattern Generation Mode and Common Waveform Channel Mode.

Problem fix/Workaround

Table 36-1. Configure PWM and CWCM according to this table:

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

9. **PWM is not restarted properly after a fault in cycle-by-cycle mode**

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

10. **BOD will be enabled after any reset**

If any reset source goes active, the BOD will be enabled and keep the device in reset if the VCC voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until VCC is above the programmed BOD level even if the BOD is disabled.

For inverted I/O, configure the Analog Comparator to give an inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

17. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

18. Flash Power Reduction Mode can not be enabled when entering sleep

If Flash Power Reduction Mode is enabled when entering Power-save or Extended Standby sleep mode, the device will only wake up on every fourth wake-up request. If Flash Power Reduction Mode is enabled when entering Idle sleep mode, the wake-up time will vary with up to 16 CPU clock cycles.

Problem fix/Workaround

Disable Flash Power Reduction mode before entering sleep mode.

19. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768 kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA A Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

20. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

21. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

22. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

37.5 8069N – 02/10

1. Added "PDI Speed" on page 92.

37.6 8069M – 02/10

1. Updated the device pin-out Figure 2-1 on page 3. PDI_CLK and PDI_DATA renamed only PDI.
2. Updated "Alternate Pin Functions Description" on page 49.
3. Updated "Alternate Pin Functions" on page 51.
4. Updated "Timer/Counter and AWEX functions" on page 49.
5. Added Table 34-18 on page 69.
6. Added Table 34-19 on page 69.
7. Changed Internal Oscillator Speed to "Oscillators and Wake-up Time" on page 88.
8. Updated "Errata" on page 93.

37.7 8069L – 11/09

1. Updated "Flash and EEPROM Page Size" on page 14.
2. Updated "Electrical Characteristics" on page 61 with Max/Min numbers.
3. Added "Flash and EEPROM Memory Characteristics" on page 64.
4. Updated Table 34-11 on page 67, Input hysteresis is in V and not in mV.

37.8 8069K – 06/09

1. Updated "Ordering Information" on page 2.
2. Updated "Errata" on page 93

37.9 8069J – 04/09

1. Updated "Electrical Characteristics" on page 61.
2. Updated "Typical Characteristics" on page 70.
3. Editorial updates.

100